



ON Semiconductor®

# FDMA710PZ

## Single P-Channel PowerTrench® MOSFET

-20 V, -7.8 A, 24 mΩ

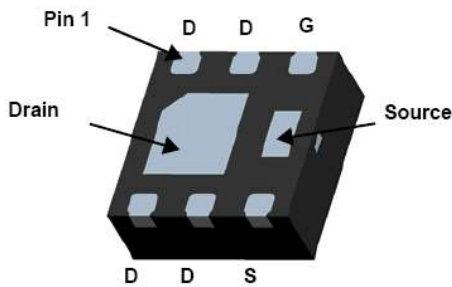
### Features

- Max  $r_{DS(on)}$  = 24 mΩ at  $V_{GS} = -5$  V,  $I_D = -7.8$  A
- Max  $r_{DS(on)}$  = 25 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -7$  A
- Max  $r_{DS(on)}$  = 35 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -5.5$  A
- Max  $r_{DS(on)}$  = 45 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -4$  A
- Low Profile - 0.8 mm maximum - in the package MicroFET 2X2 mm
- HBM ESD protection level > 3.2K V typical (Note3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

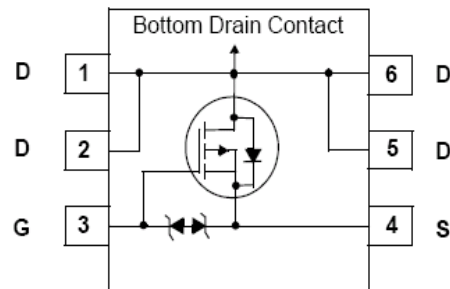
### General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated Value	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current -Continuous	$T_A = 25$ °C (Note 1a)	-7.8
	-Pulsed		-24
$P_D$	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.4
	Power Dissipation	$T_A = 25$ °C (Note 1b)	0.9
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

Symbol	Parameter	Rated Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
710	FDMA710PZ	MicroFET 2X2	7"	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -5\text{ V}$ , $I_D = -7.8\text{ A}$		19	24	m $\Omega$
		$V_{GS} = -4.5\text{ V}$ , $I_D = -7\text{ A}$		20	25	
		$V_{GS} = -2.5\text{ V}$ , $I_D = -5.5\text{ A}$		24	35	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -4\text{ A}$		29	45	
		$V_{GS} = -5\text{ V}$ , $I_D = -7.8\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		26	34	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}$ , $I_D = -7.8\text{ A}$		33		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1515	2015	pF
$C_{oss}$	Output Capacitance			265	355	pF
$C_{rss}$	Reverse Transfer Capacitance			240	360	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$ , $I_D = -7.8\text{ A}$ $V_{GS} = -5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6.4	13	ns
$t_r$	Rise Time			14	25	ns
$t_{d(off)}$	Turn-Off Delay Time			192	307	ns
$t_f$	Fall Time			96	154	ns
$Q_g(TOT)$	Total Gate Charge			30	42	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = -10\text{ V}$ , $I_D = -7.8\text{ A}$ $V_{GS} = -5\text{ V}$		2		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7.5		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -2.0\text{ A}$ (Note 2)		-0.6	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -7.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		66	106	ns
$Q_{rr}$	Reverse Recovery Charge			44	70	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $52\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.

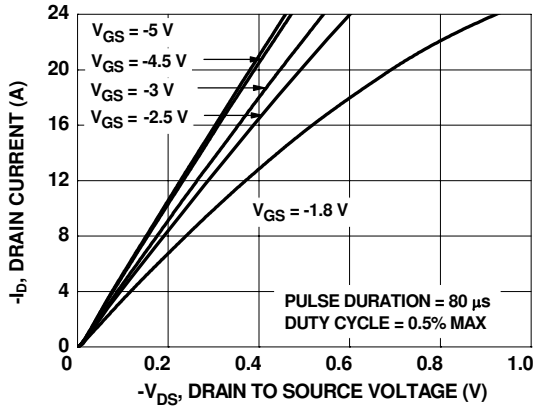


b.  $145\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

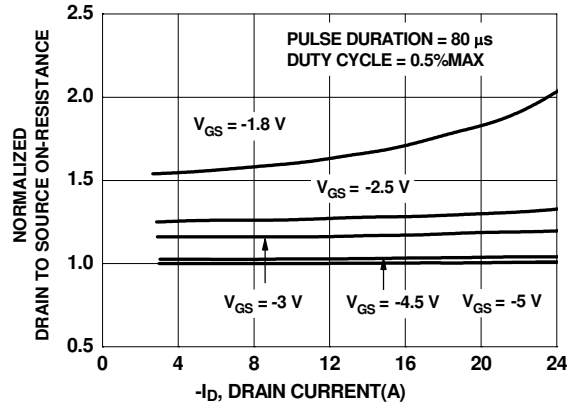
- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

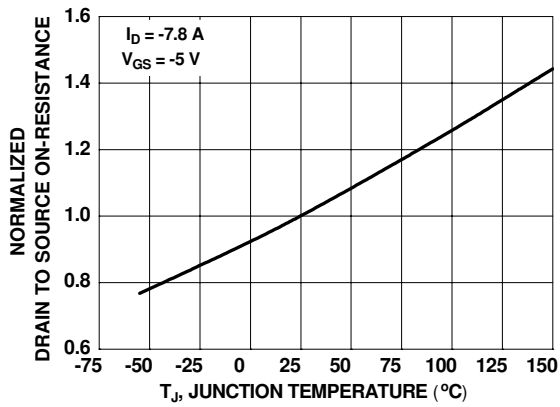
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



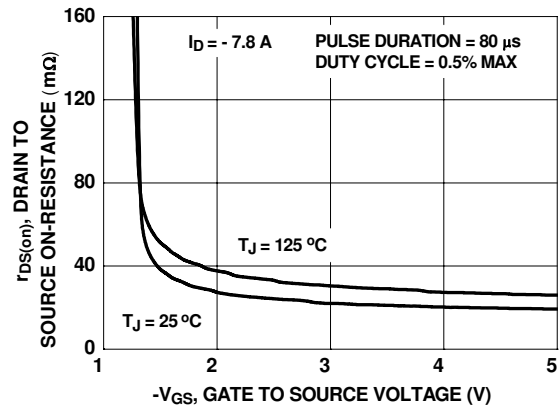
**Figure 1. On Region Characteristics**



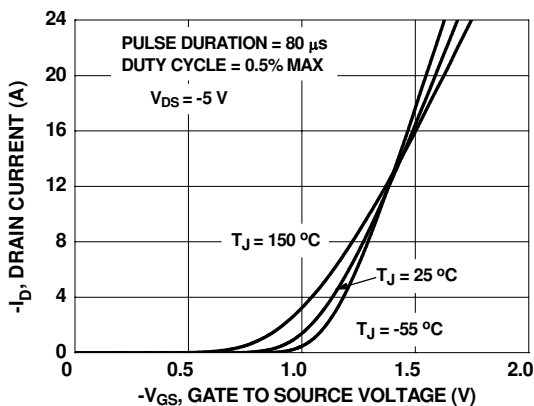
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



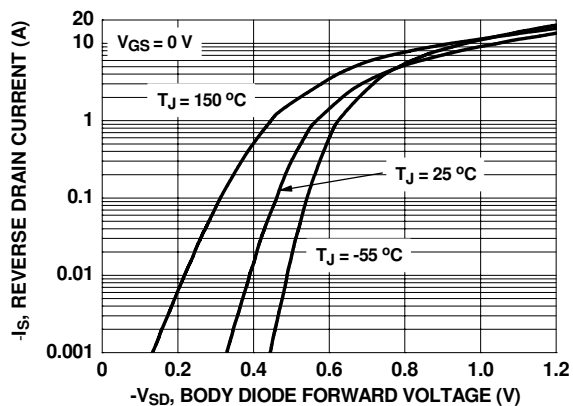
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

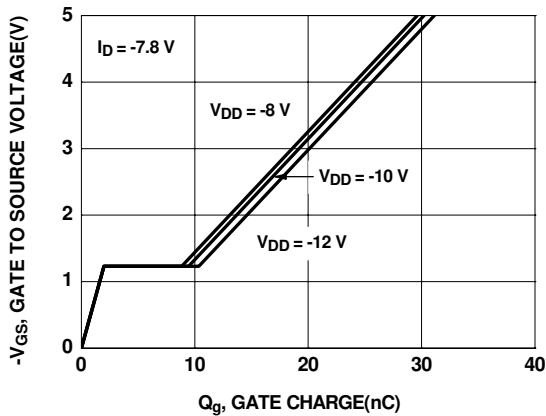


**Figure 5. Transfer Characteristics**

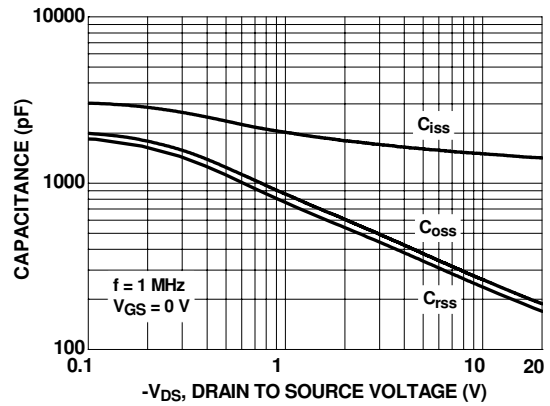


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

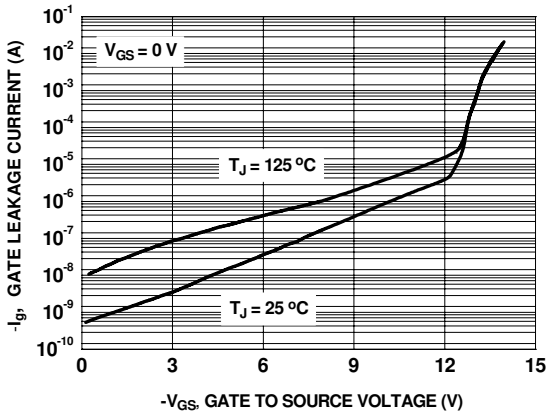
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



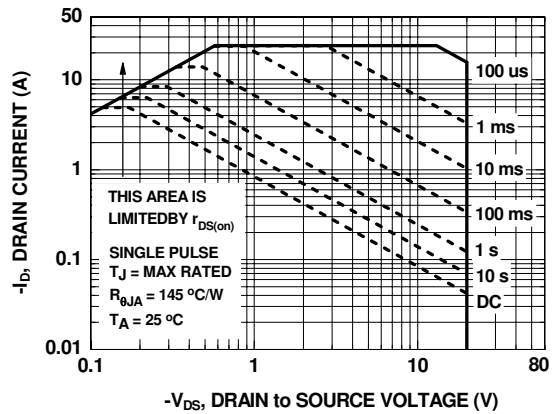
**Figure 7. Gate Charge Characteristics**



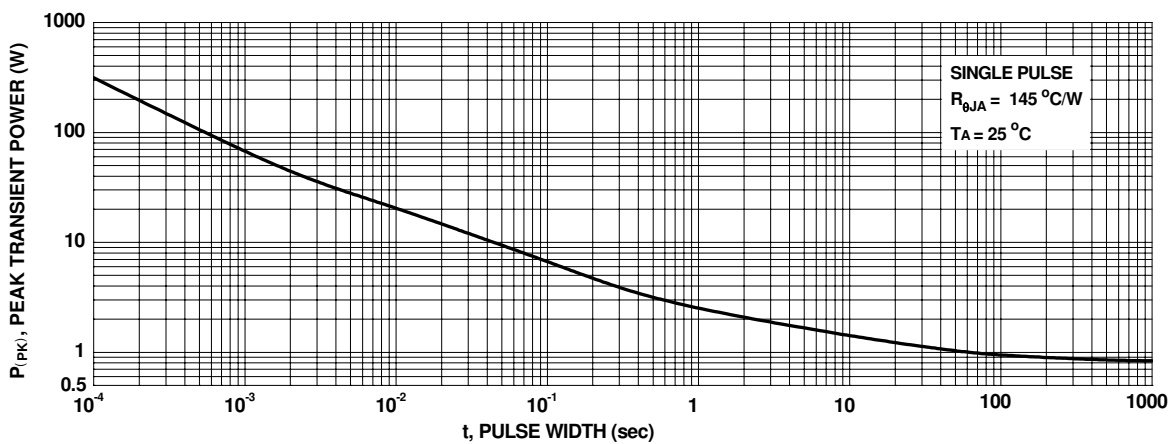
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

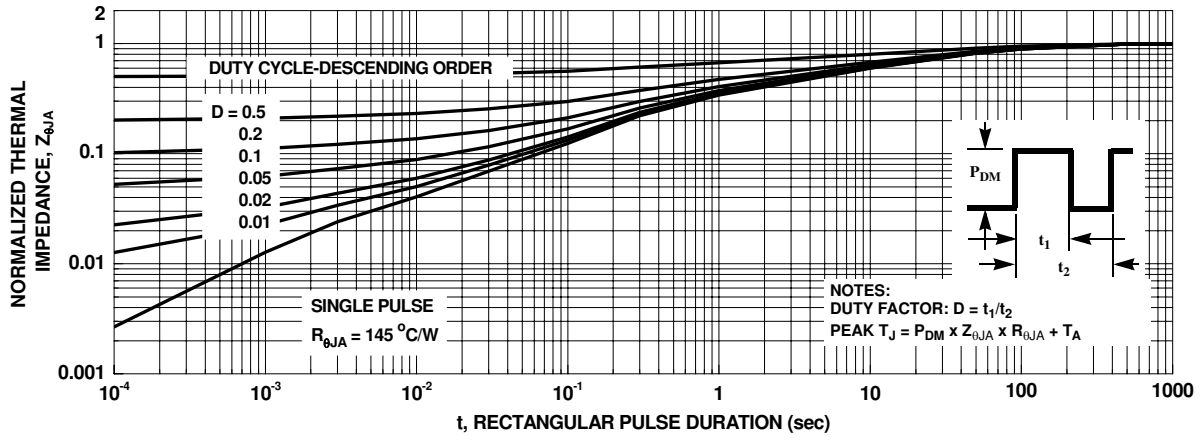


**Figure 10. Forward Bias Safe Operating Area**



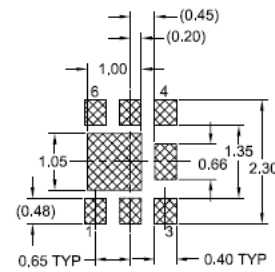
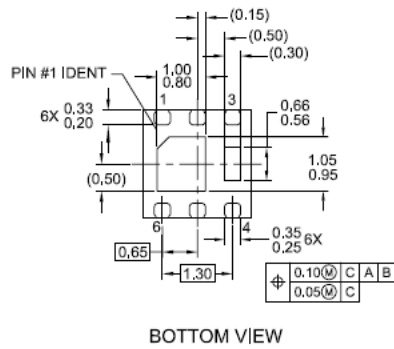
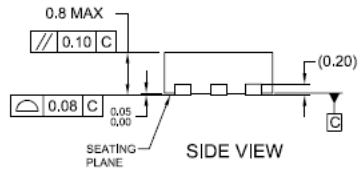
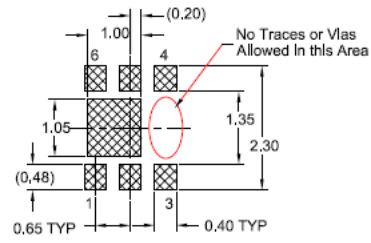
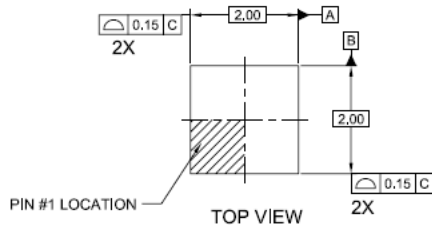
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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