FAIRCHILD SEMICONDUCTOR®

December 2012

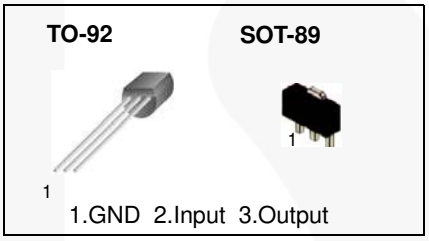
MC79L05A / LM79L05A
3-Terminal 0.1 A Negative Voltage Regulator

Features

- Output Current up to 100 mA
- No External Components
- Internal Thermal Over load Protection
- Internal Short-Circuit Current Limiting
- Output Voltage Offered in ±5% Tolerance
- Output Voltage: -5 V

Description

These regulators employ internal current limiting and thermal shutdown.



Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
MC79L05ACHX	0 ~ +125°C	9A	SOT-89	Tape and Reel
MC79L05ACP		MC79L05ACP	TO-92	Bulk
LM79L05ACZ		LM79L05ACZ	TO-92	Bulk

Block Diagram

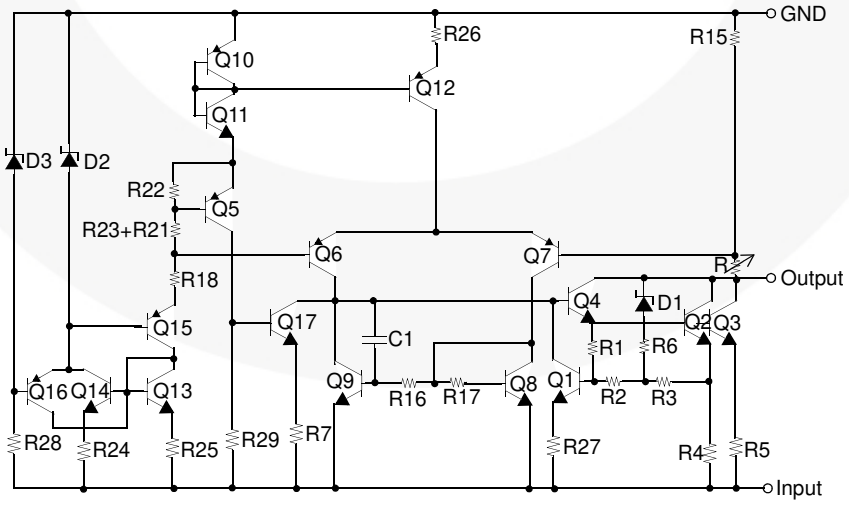


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_I	Input Voltage	-30	V
T_{OPR}	Operating Temperature Range	0 ~ +125	°C
T_{STG}	Storage Temperature Range	-65 ~ +150	°C

Electrical Characteristics

V_I = -10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C ≤ T_J ≤ +125°C, unless otherwise specified.

Symbol	Parameter		Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage		T_J = +25°C		-4.8	-5.0	-5.2	V
ΔV_O	Line Regulation (1)		T_J =+25°C	-7.0 V ≥ V_I ≥ -20 V		15	150	mV
				-8 V ≥ V_I ≥ -20 V			100	mV
ΔV_O	Load Regulation (1)		T_J =+25°C	1.0 mA ≤ I_O ≤ 100 mA		20	60	mV
				1.0 mA ≤ I_O ≤ 40 mA		10	30	mV
V_O	Output Voltage		-7.0 V ≥ V_I ≥ -20 V, 1.0 mA ≤ I_O ≤ 40 mA		-4.75		-5.25	V
			V_I = -10 V, 1.0 mA ≤ I_O ≤ 70 mA		-4.75		-5.25	V
I_Q	Quiescent Current		T_J = +25°C			2.0	5.5	mA
			T_J = +125°C				6.0	
ΔI_Q	Quiescent Current Change	With Line	-8 V ≥ V_I ≥ -20 V				1.5	mA
ΔI_Q		With Load	1.0 mA ≤ I_O ≤ 40 mA				0.1	mA
V_N	Output Noise Voltage		T_A = +25°C,10 Hz ≤ f ≤ 100 kHz			30		µV
RR	Ripple Rejection		f = 120 Hz, -8 V ≥ V_I ≥ -18 V, T_J = +25°C		41	60		dB
V_D	Dropout Voltage		T_J = +25°C			1.7		V

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Application

Design Considerations

The MC79L05A / LC79L05A fixed-voltage regulators are designed with thermal overload protection that shuts down the circuit when subjected to an excessive power overload condition. Internal short-circuit protection limits the maximum current the circuit will pass. In many low-current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to ensure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

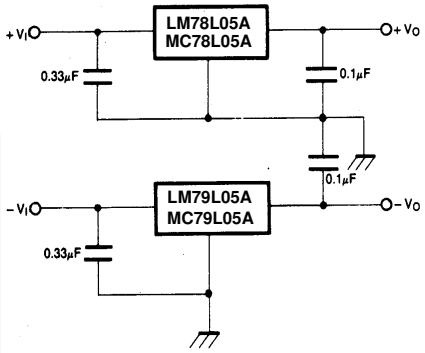


Figure 2. Positive And Negative Regulator

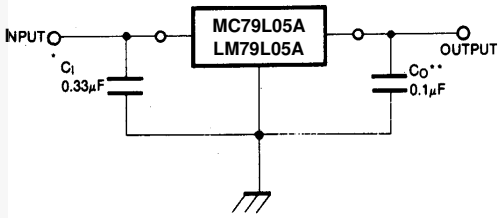


Figure 3. Typical Application

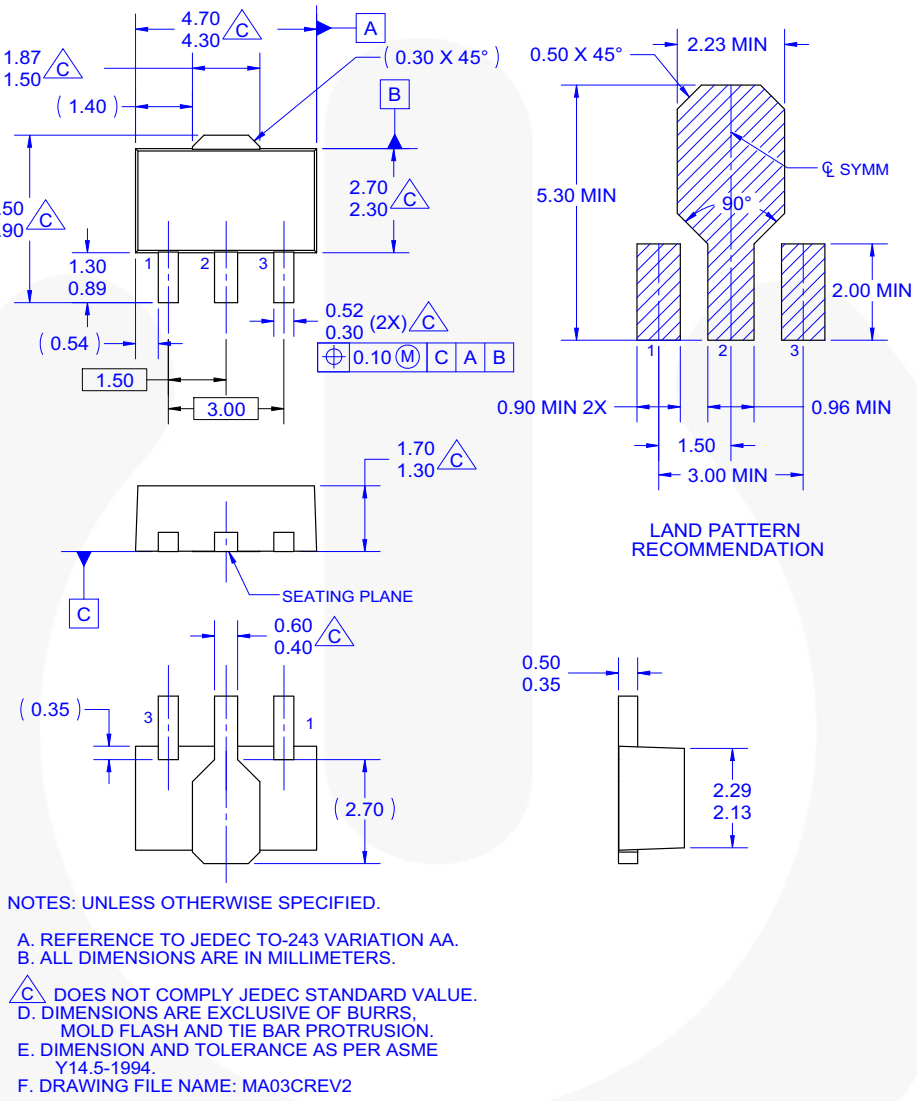
A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage, even during the low point on the input ripple voltage.

* C_I is required if regulator is located an appreciable distance from power supply filter.

** C_O improves stability and transient response.

Physical Dimensions

SOT-89



NOTES: UNLESS OTHERWISE SPECIFIED.

A. REFERENCE TO JEDEC TO-243 VARIATION AA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

C DOES NOT COMPLY JEDEC STANDARD VALUE.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. DRAWING FILE NAME: MA03CREV2

Figure 4. 3-Lead, SOT-89, JEDEC TO-243, Option AA

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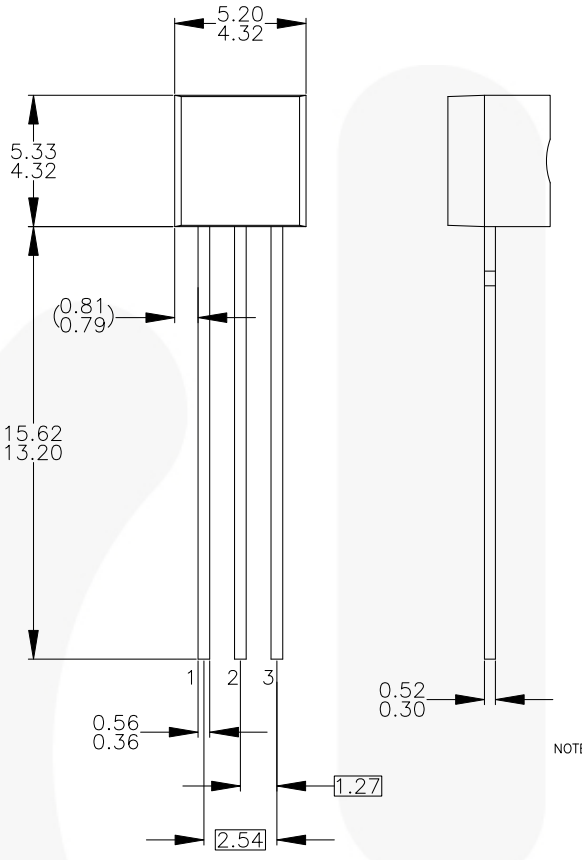
http://www.fairchildsemi.com/products/discrete/pdf/sot89_tr.pdf.

Physical Dimensions (Continued)

TO-92 Bulk Type



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P − BIPOLAR
F − JFET
M − DMOS
E − EMITTER
B − BASE
C − COLLECTOR
D − DRAIN
S − SOURCE
G − GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03DREV3.

Figure 5. 3-Lead, TO-92, Molded, Standard Straight Lead

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