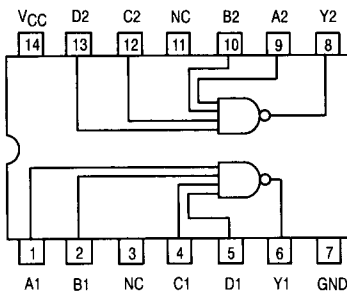




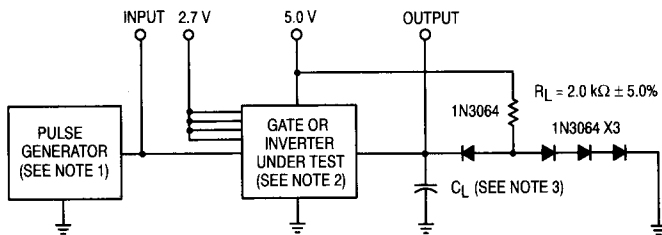
# Dual 4-Input Positive NAND Gate

ELECTRICALLY TESTED PER:  
MIL-M-38510/30007

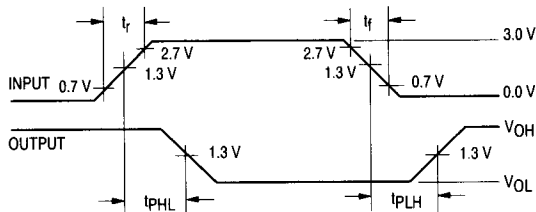
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



## Military 54LS20



AVAILABLE AS:

- 1) JAN: JM38510/30007BXA
- 2) SMD: N/A
- 3) 883: 54LS20/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	GND
NC	3	3	4	VCC
C1	4	4	6	VCC
D1	5	5	8	GND
Y1	6	6	9	VCC
GND	7	7	10	GND
Y2	8	8	12	VCC
A2	9	9	13	VCC
B2	10	10	14	GND
NC	11	11	16	VCC
C2	12	12	18	VCC
D2	13	13	19	GND
VCC	14	14	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

NOTES:

1. Pulse generator has the following characteristics:  $t_r \leq 15$  ns,  $t_f \leq 6.0$  ns,  $PRR \leq 1.0$  MHz, duty cycle = 50% and  $Z_{OUT} = 50 \Omega$ .
2. Inputs not under test are at 2.7 V.
3.  $C_L = 50$  pF  $\pm 10\%$ , including scope probe, wiring and stray capacitance.
4.  $R_L = 2.0$  k $\Omega \pm 5.0\%$ .
5. Voltage measurements are to be made with respect to network ground terminal.
6. Terminal conditions (pins not designated may be high  $\geq 2.0$  V, or low  $\leq 0.7$  V, or open).

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## 54LS20

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = - 400 μA, V <sub>IL</sub> = 0.7 V, V <sub>IN</sub> = 5.5 V on other inputs.
V <sub>OL</sub>	Logical "0" Output Voltage		0.4		0.4		0.4	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4.0 mA, V <sub>IH</sub> = 2.0 V, on all inputs.
V <sub>IC</sub>	Input Clamping Voltage		-1.5					V	V <sub>CC</sub> = 4.5 V, V <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH1</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V, other inputs = 0 V.
I <sub>IH2</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V, other inputs = 0 V.
I <sub>IL</sub>	Logical "0" Input Current	- 150	- 380	- 150	- 380	- 150	- 380	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V, other inputs = 5.5 V.
I <sub>OS</sub>	Output Short Circuit Current	- 15	- 100	- 15	- 100	- 15	- 100	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (all inputs), V <sub>OUT</sub> = 0 V.
I <sub>CCH</sub>	Power Supply Current		0.8		0.8		0.8	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V (all inputs).
I <sub>CCL</sub>	Power Supply Current		2.2		2.2		2.2	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs).
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.7		0.7		0.7	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 5.0 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL</sub> t <sub>PHL</sub>	Propagation Delay /Data-Output Output High-Low	2.0 —	17 15	2.0 —	24 19	2.0 —	24 19	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ.
t <sub>PLH</sub> t <sub>PLH</sub>	Propagation Delay /Data-Output Output Low-High	2.0 —	15 15	2.0 —	20 15	2.0 —	20 15	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 2.0 kΩ. V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2.0 kΩ.

**NOTE:**1. The limits specified for C<sub>L</sub> = 15 pF are guaranteed but not tested.