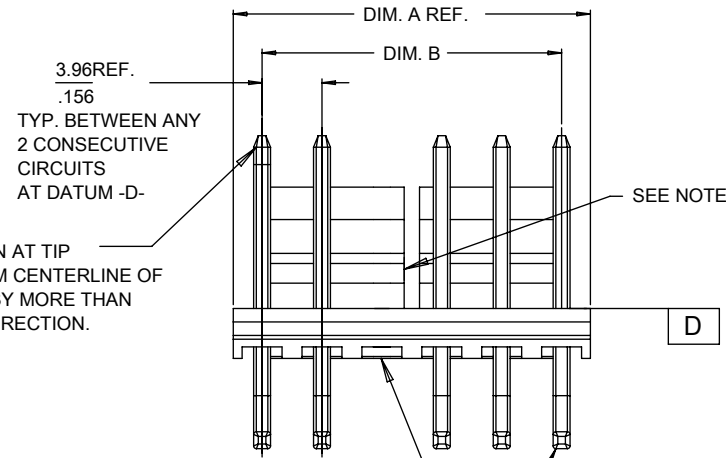


CENTERLINE OF PIN AT TIP
NOT TO VARY FROM CENTERLINE OF
PIN AT DATUM -D- BY MORE THAN
0.20 / .008 IN ANY DIRECTION.

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0.20 / .008 IN ANY DIRECTION.



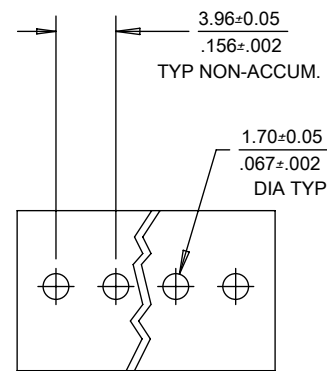
OPTIONAL VOIDED CIRCUIT
SEE CHART FOR LOCATIONS

CIRCUIT 1 REF.
SEE NOTE 10

CKT	DIM. A	DIM. B	SLOT LOC BETWEEN CKTS
2	7.77 .306	3.96±0.05 .156±.002	NONE
3	11.73 .462	7.92±0.08 .312±.003	NONE
4	15.70 .618	11.89±0.08 .468±.003	NONE
5	19.66 .774	15.85±0.10 .624±.004	NONE
6	23.62 .930	19.81±0.10 .780±.004	3 & 4
7	27.58 1.086	23.77±0.10 .936±.004	4 & 5
8	31.55 1.242	27.74±0.13 1.092±.005	4 & 5
9	35.51 1.398	31.70±0.13 1.248±.005	5 & 6
10	39.47 1.554	35.66±0.13 1.404±.005	5 & 6
11	43.43 1.710	39.62±0.15 1.560±.006	6 & 7
12	47.40 1.866	43.59±0.15 1.716±.006	4 & 5 8 & 9
13	51.36 2.022	47.55±0.15 1.872±.006	4 & 5 9 & 10
14	55.32 2.178	51.51±0.18 2.028±.007	5 & 6 9 & 10
15	59.28 2.334	55.47±0.18 2.184±.007	5 & 6 10 & 11
16	63.25 2.490	59.44±0.18 2.340±.007	5 & 6 11 & 12
17	67.21 2.646	63.40±0.20 2.496±.008	6 & 7 11 & 12
18	71.17 2.802	67.36±0.20 2.652±.008	6 & 7 12 & 13

NOTES:

- MATERIAL: HEADER-GLASS FILLED POLYESTER, 94V-0, MOLDED NATURAL (WHITE).
- FINISH: (197) OVERALL REFLOWED MATTE TIN: 0.00152/.000060 MIN. OVER 0.00127/.000050 MIN. NICKEL OVERALL. (154) OVERALL TIN: .00254/.000100 MIN OVER .00127/.000050 MIN NICKEL. (208) SELECT GOLD: .00038/.000015 MIN, SELECT TIN: .00254/.000100 MIN, OVERALL NICKEL UNDERPLATE: .00127/.000050 MIN. (228) SELECT GOLD: .00076/.000030 MIN, SELECT TIN: .00254/.000100 MIN, OVERALL NICKEL UNDERPLATE: .00127/.000050 MIN. (241) SELECT GOLD: 0.00051/.000020 MIN. SELECT TIN: 0.00254/.000100 MIN. OVERALL NICKEL UNDERPLATE: 0.00127/.000050 MIN. FOR ADDITIONAL PLATING INFO, SEE SDES-88.
- PRODUCT SPECIFICATION AND PROCESS PARAMETERS: SEE PS-08-50.
- PACKAGING INFORMATION: SEE CHART
- SOLDERABILITY: PER SMES-152.
- PIN PUSH-OUT FORCE: PRIOR TO SOLDERING, A 3 LB. MINIMUM FORCE (IN EITHER DIRECTION)
- PARTS ARE STACKABLE END TO END ON 3.96/.156 CENTERS.
- THIS PART CONFORMS TO CLASS B REQUIREMENTS OF COSMETIC SPECIFICATION PS-45499-002.
- SLOTS ON BACKWALL ARE BETWEEN CIRCUITS. SEE CHART FOR LOCATION.
- CIRCUIT 1 DESIGNATION IS USED TO DEFINE VOID LOCATION. CIRCUIT 1 MAY OR MAY NOT LINE UP WITH CIRCUIT 1 ON THE MATING HOUSING.



PCB LAYOUT: COMPONENT SIDE

QUALITY SYMBOLS	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX ELECTRONIC TECHNOLOGIES, LLC AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION										
∇ = 0	ADD 41792-0704 EC NO: 112230 DRWN: MKIPPER CHK'D: JDFOX APPR: FSMITH REV	GENERAL TOLERANCES (UNLESS SPECIFIED)		DIMENSION UNITS	SCALE						
∇ = 0		MM	INCH	MM/IN	2:1						
∇ = 0		4 PLACES ±	±	DRWN BY	DATE						
∇ = 0		DRW: MKIPPER CHK'D: JDFOX APPR: FSMITH	3 PLACES ±	± 0.01	JSCHAFFER	11-07-03	KK .156 HEADER ASSEMBLY FRICTION LOCK RIGHT ANGLE W/O PEGS				
∇ = 0			2 PLACES ±	± 0.015	CHK'D BY	DATE					
∇ = 0			1 PLACES ±	± 0.38	KSAMIEC	11-10-03	PRODUCT CUSTOMER DRAWING				
∇ = 0			0 PLACES ±	±	APPR BY	DATE					
∇ = 0		EC NO: 112230 DRWN: MKIPPER CHK'D: JDFOX APPR: FSMITH	ANGULAR TOL ± 0.5		DRAWING SIZE	THIRD ANGLE PROJECTION	SERIES	MATERIAL NUMBER	CUSTOMER		
∇ = 0			DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		B		41792	SEE CHART	GENERAL MARKET		
∇ = 0							DOCUMENT NUMBER	DOC TYPE	DOC PART	SHEET NUMBER	
						SDA-41792	PSD	000	1 OF *		

Model: EM-41792 (SD Package)

RELEASE STATUS	RELEASE DATE
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