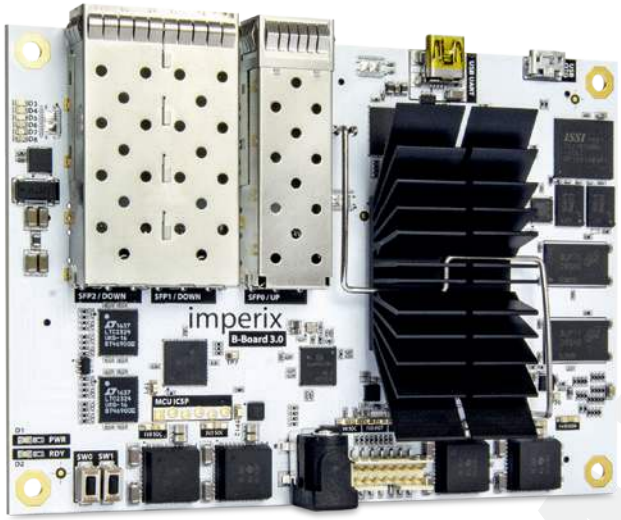
B-Board PRO

Embeddable controller

The B-Board PRO is an advanced controller designed for series-manufactured products.



GENERAL DESCRIPTION

The B-Board PRO is the core of the B-Box RCP rapid control prototyping platform, which can also be used a standalone unit, directly within series-manufactured products.
Thanks to the exact equivalence between B-Box RCP and B-Board PRO, users can benefit from the increased flexibility of the prototyping controller for research, while using a smaller and more cost-effective variant during production. In practice, code that has been developed on B-Box can be ported instantly on B-Board, hence offering a total transparency between both platforms. This approach significantly reduces the time needed for engineers to make the transition between the laboratory and the field, eventually reducing the time to market.

TYPICAL APPLICATIONS

The B-Board PRO is best used within demanding power electronic systems that require intensive R&D, as well a short development cycles. Its attractive computing performance and large flexibility also make it the perfect fit for systems that feature complex control algorithms.
Finally, its excellent PWM resolution makes it ideally suited for use with wide band gap devices such as SiC or GaN.

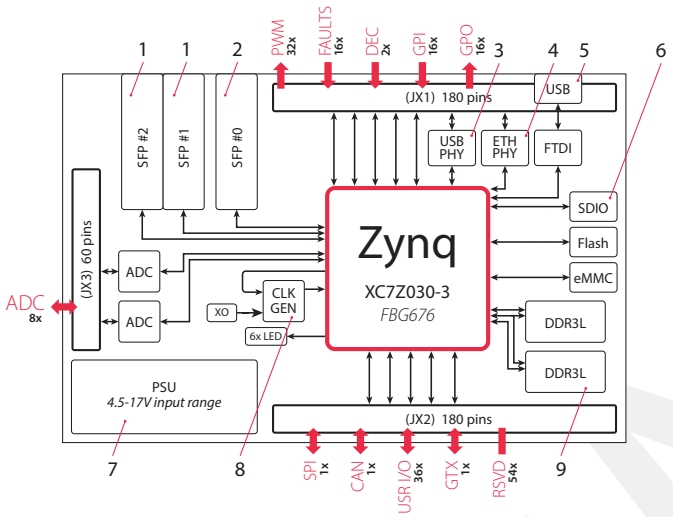
KEY FEATURES AND SPECIFICATIONS

The B-Board PRO has been designed from the start with synchronous sampling applications in mind. Indeed, it offers a large configurability of timings and guarantees a very strict management of all phase shifts, from analog inputs to PWM outputs, including in networked configurations.
Excellent computational performance are also delivered, thanks to a dual-core ARM processor and Kintex-grade FPGA, supporting closed-loop control applications up to hundreds of kHz!
Networked configurations of up to 64 controllers and hundreds of I/Os are supported by *RealSync*, a proprietary technology that guarantees sub-µs communication latency and ns-scale synchronization accuracy. The main system specifications are:

- Dual-core 1 GHz ARM processor
- Kintex-grade FPGA (user programmable)
- Advanced pulse-width modulators (PWM)
- 4 ns PWM resolution
- 140 user I/Os per unit
- 86 x 124 x 22 mm form factor

DEVICE DESCRIPTION

1) SFP Interconnect – DOWN links
2) SFP Interconnect – UP link
3) USB OTG (on bottom BSH)
4) Gigabit Ethernet (on bottom BSH)
5) Console port



6) Onboard memories:
   – SD card slot
   – 32 MB Flash (program)
   – 8 GB Flash (logging)
7) Wide input range on-board power supply
8) SFP clocks management
9) DDR memory (1 GB)

Fig. 1. Simplified structure of the B-Board processing module.

MAIN SPECIFICATIONS

Component	Specification	Component	Specification
System on chip	Xilinx Zynq XC7Z030-3FBG676E	PWM outputs	Electrical (3V3) x32 Various modulators 4 ns resolution
Processing system	ARM Cortex A9 1 GHz x2 1GB DDR3		
Programmable logic (FPGA)	Kintex 7 125K (user programmable)	Analog inputs	16 bits, simultaneous sampling x8 2 Msps (maximum speed) / 500 ksps (B-Box compatibility mode)
Storage	Flash 16MB x2 micro SD + eMMC 8GB		
Communication	USB OTG x1 Ethernet 1Gbps x1	Incremental decoder inputs	3-pins (A,B,Z) x4 Shared with GPI inputs
		Fault inputs / outputs	Digital (3.3V) x16 Electrical interlock (3.3V) x1
	USB 2.0 high speed console x1 SFP+ 5 Gbps x3	General-purpose digital inputs (GPI)	Electrical (3.3V) x16
Power supply	4.5–17 VDC (15 W)	General-purpose digital outputs (GPO)	Electrical (3.3V) x16
Operating temperature range	0 – 80 °C	User High-speed I/Os	FPGA direct (3V3) x36

Table 2. Main system specifications for B-Board PRO.

MAXIMUM I/O CAPABILITIES

Component	Characteristics	Single (1 unit)	Networkedd (64 units)
Analog inputs	Fully configurable (gain, impedance, filter, protection)	8	512
PWM outputs	Electrical, >500 Mbps	32	2048
General-purpose digital outputs (GPO)	Electrical, >100 Mbps	16	1024
General-purpose digital inputs (GPI)	Electrical, >100 Mbps	16	1024

Table 3. Maximum I/O count per B-Board PRO and in networked configuration.

ENVIRONMENTAL CONDITIONS

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
DC input voltage		4.5	12	17	V
Power consumption		5	7.5	32	W
EMC performance	Radiated IEC61000-3-2 class A / Conducted IEC61201-3 class A / Burst IEC61000-4-4 Level 4	pass			
Operating temperature	Operation above 55°C requires active cooling of the heatsink (forced air).	0		80	°C
Storage temperature		-25		85	°C
Temperature change rate		-0.5		0.5	°C/min
Relative humidity	Non-condensing	0		100	%
Absolute humidity	Non-condensing	1		29	g/m³

Table 4. Environmnental specifications for the B-Board PRO.

LOGICAL STRUCTURE

The B-Board PRO operates thanks to an association between two CPU core and dedicated peripherals implemented in programmable logic. The distribution of tasks is as follows:

- CPU0: Running on Linux, the first core is responsible for loading the application code, supervising the system execution and managing the data logging.
- CPU1: Running on BBOS (lightweight secured proprietary operating system), the second core executes the application-level control code developed by the user.
- FPGA: The programmable logic area contains all the application-specific peripherals. By default, the corresponding firmware is fixed.

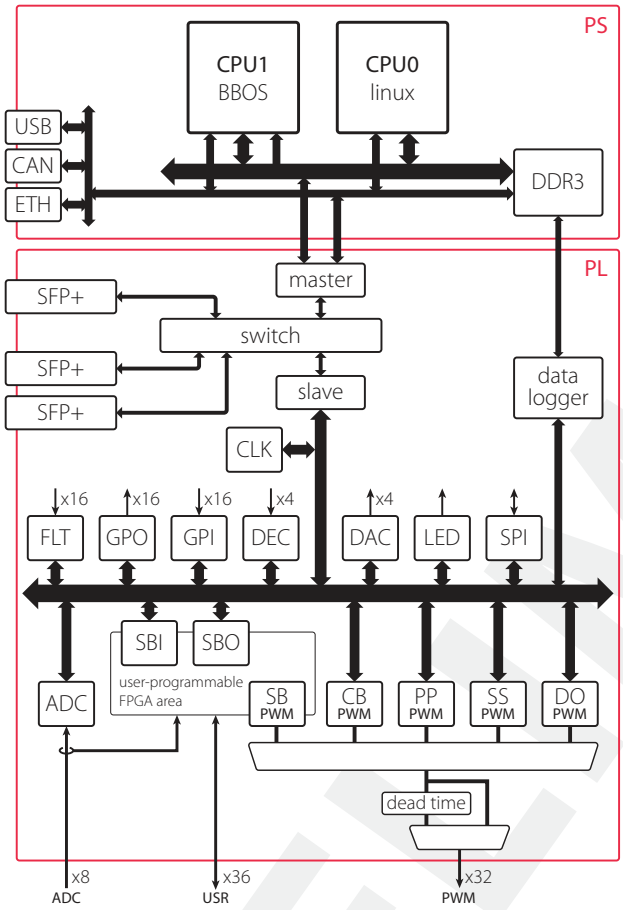


Fig. 2. Functional overview of the B-Board PRO controller.

The pre-implemented FPGA peripherals are as follows:

- CLK: Offers clock generators with up to four separate time-bases that can be used with other peripherals.
- ADC: Acquires data from the 8 analog input channels located on board.
- DAC: Updates the 4 analog output channels (SMA connectors on the front side of the device).
- SBI: Provides easy-to-use access for inbound data traffic from the user-programmable area (sandbox).
- SBO: Provides easy-to-use access for outbound data traffic from the user-programmable area (sandbox).
- DEC: Support the decoding of signals produced by up to four incremental encoders for motor drive applications.
- CB-PWM: Contains 32 fully-configurable carrier-based modulators (conventional sampled PWM).
- SS-PWM: Implements multilevel modulation for modular converters using a Sort-&-Select voltage balancing technique such as commonly used in Modular Multilevel Converters (MMC). It achieves the balancing of floating capacitors, while maximizing the ration between waveform performance and average switching frequency.
- PP-PWM: Provides hardware support for the generation of Programmed Patterns. It is useful for PWM techniques such as Selective Harmonic Elimination (SHE) or Optimized Pulse Patterns (OPP) in general.
- DO-PWM: Offers a Direct Output operation, allowing to force a specific lane state (0 or 1). This is useful for control techniques such as Model Predictive Control (MPC) or Direct Torque Control (DTC).
- SB-PWM: Provides access to the PWM outputs from the user-programmable area (sandbox).
- GPO: Offers 16 General-Purpose Outputs.
- GPI: Offers 16 General-Purpose Inputs.
- FLT: Offers 16 configurable fault inputs. These inputs can also be used as general-purpose inputs.
- LED: Drives the 3 LEDs available on the front panel.
- USR: Provides a direct access to the 36 fully-configurable high-speed I/O lanes.
- ETH: Supports data exchanges on Ethernet (TCP/UDP).
- CAN: Provides connectivity with CAN peripherals.
- SPI: Provides SPI connectivity (bidirectional).

ANALOG INPUTS

The B-Board PRO has two LTC2324-16 16 bits full-differential analog-to-digital converters from Linear Technologies, with a total of 8 channels. The devices guarantee simultaneous sampling on all channels. Overall performance specifications are given in Table 5. Timing characteristics are shown in Table 6.

Data transfer to the processing cores is achieved by FPGA and over *RealSync* in case of multi-unit operation. Transfer delays vary with the amount of data (see Fig. 3). The overall delay from sampling to cache memory is therefore the sum of the A/D conversion time plus data transfer delay.

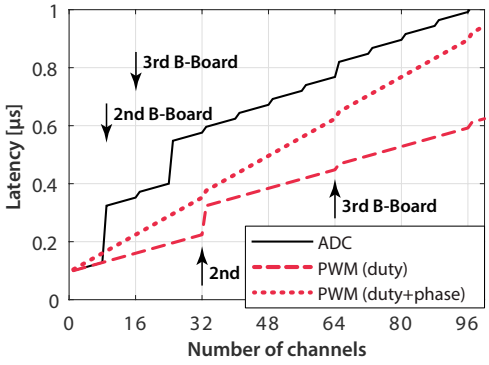


Fig. 3. Data transfer delay, as a function of the number of channels

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage range	*Differential mode*		*±5.0*		*V*
Power supply voltage		*5.15*	*5.2*	*5.3*	*V*
Max. tolerable voltage	*On any pin*	*-0.3*		*5.3*	*V*
CMRR	f_{IN} = *500 kHz*		*102*		*dB*
THD	f_{IN} = *500 kHz*		*-91*		*dB*
Signal–to–noise ratio	f_{IN} = *500 kHz*		*82.5*		*dB*
Full-scale error		*-35*	*±12*	*+35*	*LSB*
Input DC leakage current	*Each pin*	*-1*		*+1*	*µA*
Input capacitance	*Each pin*		*10*		*pF*
Power consumption	*On 5.2 V supply*		*160*	*250*	*mW*

Table 5. Performance specifications of the A/D conversion.

For proper operation, the carrier board should be designed such that the following design guidelines are followed:

- **Power supply:** A clean 5.2V power supply must be provided on the JX3 connector in order to supply the ADC chips. This power supply is entirely separated from other on-board power supplies.
- **Protection:** It is recommended to implement overvalue detection mechanisms on the carrier board in order to provide hardware-level protections for the to-be-controlled power converter.
- **ADC driver:** A low-offset wide-bandwidth operational amplifier must be present on the carrier board in order to effectively drive the ADCs. When selecting operational amplifiers, attention must be paid to the following performance characteristics:
  - Settling time (typ. 0.1% < 30 ns)
  - Slew rate (typ. > 250 V / µs)
  - Input offset (typ. < 400 µV)
  - Suitable output voltage range (typ. 0.1 – 4.9V)

  Imperix recommends considering the following components for the carrier board design:
  - THS4551 for a full-differential solution with a single +5.2V power supply. An example is given in Fig. 5.
  - AD8021 for a high-performance solution with power supplies up to ±12V. A recommended schematic with an output for protection thresholds is given in Fig. 6. The input common-mode range is 0.1–3.9V.
  - AD826 or LT1360 for solutions with ±15V power supplies. Other speed vs. precision trade-offs may also be selected.

FPGA-BASED PERIPHERAL BLOCK

Depending whether the B-Board is used inside the B-Box or in standalone mode, the ADC peripheral block switches between two precisely-matched subsystems. This guarantees that the analog input chain behaves strictly identically in both configurations.

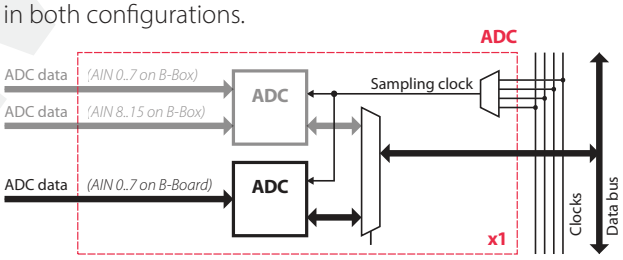


Fig. 4. Internal structure of the ADC peripheral block.

EXPANDING THE ANALOG INPUTS

Using the user-programmable area of the FPGA (see page 13), additional ADC chips may be connected to the B-Board PRO in order to increase the numper of analog channels.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Aperture delay			*500*		*ps*
Transient response	*Full-scale step*		*30*		*ns*
Sampling jitter	*Same B-Board*		*±2.1*		*ns*
	Across all B-Boards		*±3.6*		*ns*
Conversion time	*Retro-compatible mode with B-Box RCP hardware < 3.5 (commercialized 2020)*		*1.98*		*µs*
	Full-performance mode (non-transparent with B-Box HW < 3.5)		*220*		*ns*
Data transfer delay		*See Fig. 3.*			*ns*
Sampling rate	*Retro-compatible mode with B-Box RCP hardware < 3.5 (commercialized 2020)*	*0.0*		*500*	*ksps*
	Full-performance mode (non-transparent with B-Box HW < 3.5)	*1.0*		*2.0*	*Msps*

Table 6. ADC timing specifications

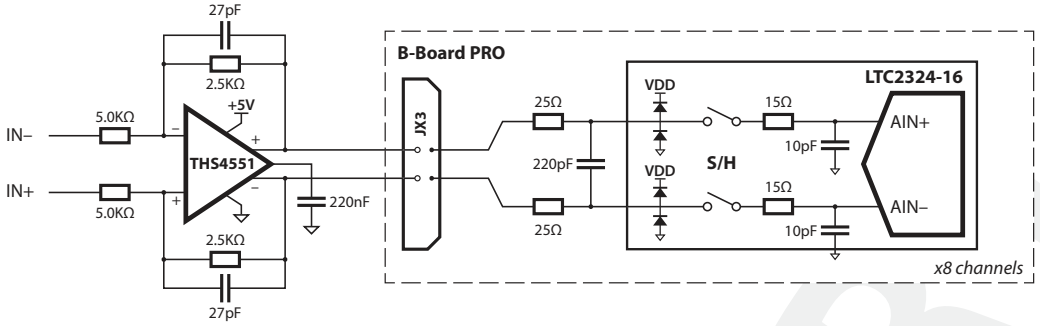


Fig. 5. Recommended carrier schematic for the ADC signals with +5.2V power supply.

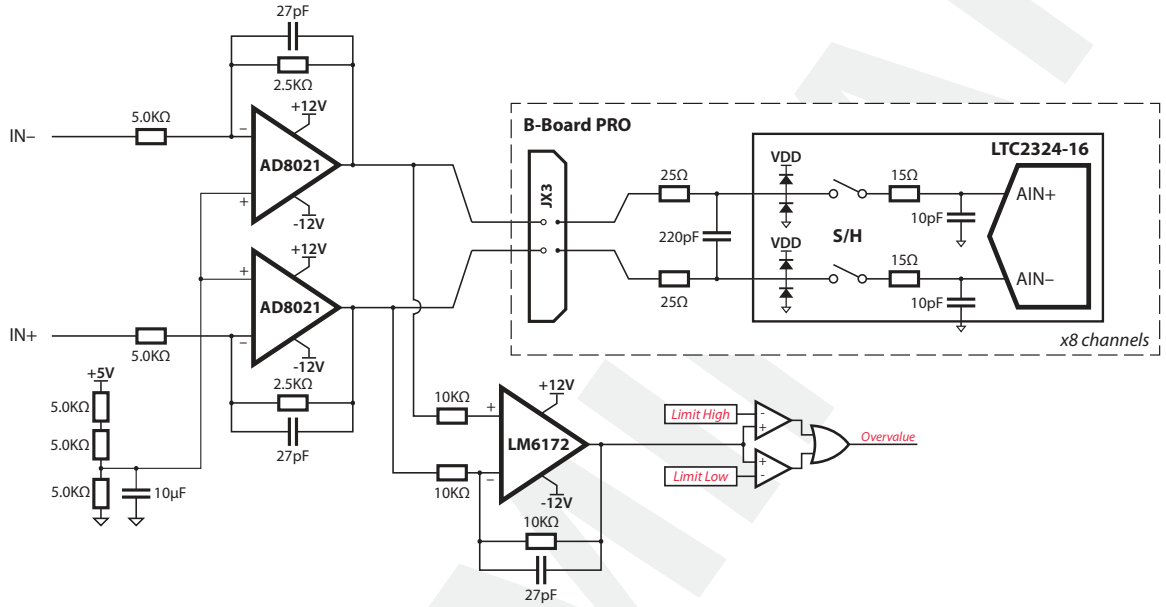


Fig. 6. Recommended carrier schematic for the ADC signals with separate ±12V power supplies.

POWER SUPPLIES

Unlike most other piggy-back control boards, the B-Board PRO already embeds numerous power suplies, so that only two supply voltages are needed:

» **Digital circuits:** A **4.5–17V** DC power supply must be provided as the main power supply. Voltages of 5V, 12V and 15V are therefore all applicable with B-Board PRO, offering a large flexibility for integration within existing equipment. This power supply is subdivided onboard to generate lower voltages such as 1.0V, 1.2V, 1.8V, 3.3V.

» **Analog circuits:** Another **5.2V** DC power supply must be provided.[1] It is exclusively used by the analog-to-digital converters. It may therefore be neglected in case the onboard ADCs are not used. Optionally, in case 5V is also used for the main power supply, a single supply voltage may be used for both inputs, provided that suitable filtering is implemented on the analog section. Please however contact support@imprix.ch to learn about the technical limitations before considering this option.

POWER SUPPLY SEQUENCING

In order to prevent excessive current flows during the power-up process (that may endager the Zynq or other components), the carrier board should be designed such that the following sequence is observed:

1) Allow the internal logic of the Zynq to power up first. Wait until the B-Board raises its **BB_RDY** flag for applying any voltage larger than 1.8V to the B-Board I/O pins.

2) In case some devices require a particular power-up sequence on the carrier board or may be endangered by voltages applied from the B-Board PRO, the **MB_RDY** flag must be held low until this particular sequence is completed. Alternatively, **MB_RDY** can be left floating as it is weakly pulled up on the B-Board.

3) When the **MB_RDY** flag is sensed high, the B-Board finishes its power up sequence by powering the previously-gated 3.3V devices as well as Zynq transceivers.

4) Independently, once he **BB_RDY** pin is held high, 3.3V circuits can be safely powered up on the carrier board without endagering the Zynq.

1 The 5.2V power supply may be used at lower voltages (e.g 4.75–5V) with limitations on the analog input voltage range. Please contact support@imperix.ch to learn about the technical limitations before considering this option.

BOOTING SEQUENCE

Once all power supplies are properly powered up, the Zync initiates its booting procedure, which takes around 20s. The overall sequence can be followed using the green LEDs D3-D5.

RDY	D3	D4	D5	Status	Duration
0	1	0	1	*Core power up in progress*	*60 ms*
0	0	1	0	*3V3 power up in progress*	*50 ms*
0	0	0	1	*Transceiver power up in progress*	*150 ms*
0	0	1	1	*Clock configuration in progress*	*60 ms*
0	1	1	1	*Zynq booting in progress*	*60 ms*
1	X	X	X	*Zynq successfully booted* *Operating system loading in progress* *Network discovery is progress*	*18-25s*

Table 7. LED indicators (green) during the power up sequence.

STATUS LEDS AT BOOT

Two onboard LEDs indicate the execution state of the overall power up and boot sequence:

» D1 / PWR turns blue when input power is available on the B-board. It should therefore be always on.

» D2 / RDY turns blue when the board has sucessfully completed the power up and booting sequence.

For debug purposes, in case anything goes wrong during the power up or booting process, a corresponding error code is displayed using the D6-D8 LEDs.

RDY	D6	D7	D8	Status
0	0	0	1	*Power failure during the powering of the core voltage*
0	0	1	0	*Power failure during the powering of the 3.3 V supply*
0	0	1	1	*Power failure during the powering of the transceivers*
0	1	0	X	*Failure during the clock configuration*
0	1	1	0	*Failure during the Zynq booting process*
0	1	1	1	*Power failure after booting (i.e. during normal operation)*
0	0	0	0	*No error*
1	X	X	X	*Control of LEDs transferred to Zynq*

Table 8. Error codes (red) applicable during the power up sequence.

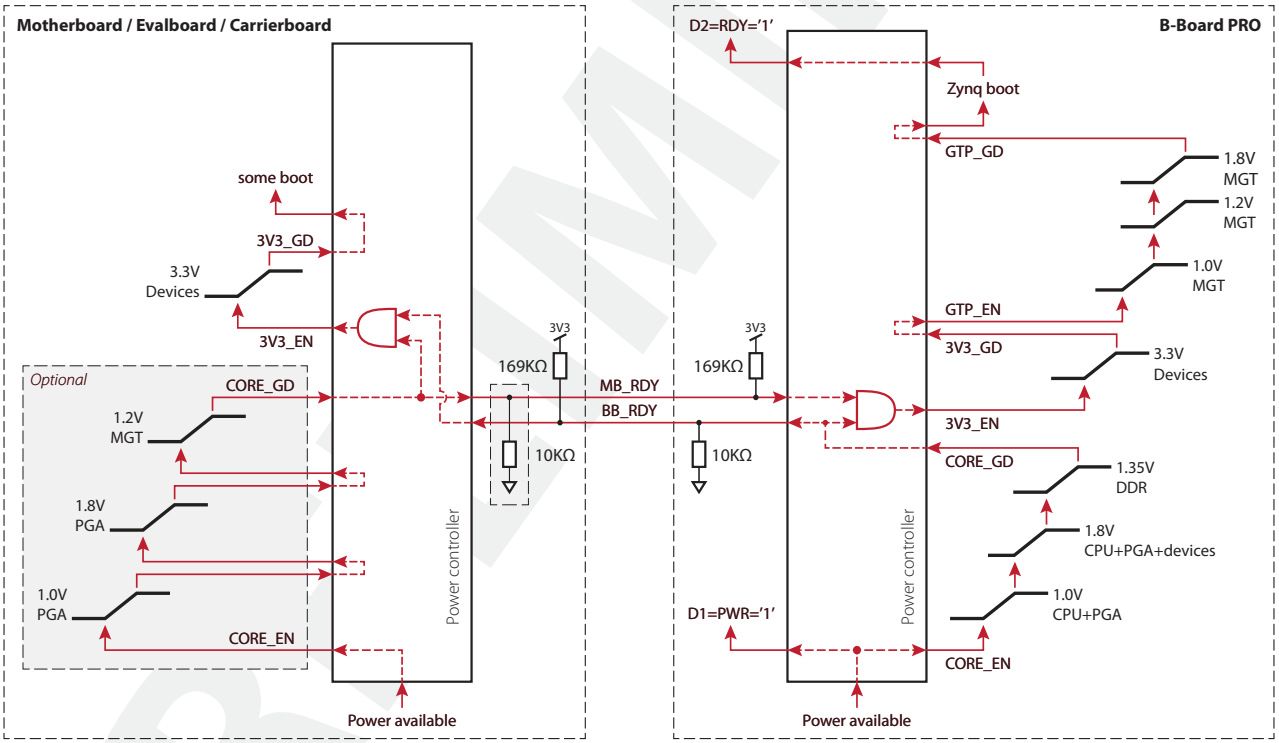


Fig. 7. Power sequencing scheme of the B-Board PRO.

DIGITAL I/O SIGNALS

All digital inputs are available on the two high-speed connectors JX1 and JX2. The following functions are available:

- PWM: Pulse-width modulated signals (32 bits)
- GPO: General purpose outputs (16 bits)
- GPI: General purpose inputs (16 bits)
- FLT: Fault feedback inputs (16 bits)
- SPI: Multi-function acquisition bus (4 bits)
- USR: Fully-configurable input / output bus (32 + 4 bits)
- CAN: Controller Area Network communication (2 bits)
- ETH: Ethernet MDI signals from onboard PHY (8 bits)

The location and voltage level of the related pins is summarized in Table 9.

> WARNING:
> Always pay attention to the **logic voltage level** of each signal. Refer to Table 9 for detailed information. Unexpected behavior or damages may occur in case inappropriate voltage is applied to the Zynq or any other circuit.

Peripheral	Bit lanes	Level	Main functions and bus width	Alternate function	Connector	Internal topology	Typ. speed
GPI	*GPI 0-7*	*3.3 V*	*General-purpose inputs (16 bits)*	*Incremental decoder*	*JX 2*	*Direct to Zynq*	*400 Mbps*
	GPI 8-15	*3.3 V*		*Incremental decoder*	*JX 1*	*Level shifted to 1.8V on B-Board*	*150 Mbps*
GPO	*GPO 0-7*	*3.3 V*	*General-purpose outputs (16 bits)*		*JX 2*	*Direct to Zynq*	*400 Mbps*
	GPO 8-15	*3.3 V*			*JX 1*	*Level shifted to 1.8V on B-Board*	*150 Mbps*
PWM	*PWM 0-15*	*3.3 V*	*Pulse-width modulated signals (32 bits)*	*High-speed DOUT*	*JX 2*	*Direct to Zynq*	*400 Mbps*
	PWM 15-31	*1.8 V*		*High-speed DOUT*	*JX 1*	*Direct to Zynq*	*500 Mbps*
FLT	*FLT 0-15*	*1.8 V*	*Fault feedback signals (16 bits)*	*High-speed DIN*	*JX 1*	*Direct to Zynq*	*500 Mbps*
SPI	*SPI 0-4*	*1.8 V*			*JX 1*	*Direct to Zynq*	*500 Mbps*
USR	*USR 0-35*	*3.3 V*			*JX 2*	*Direct to Zynq*	*400 Mbps*
CAN	*CAN TX/RX*	*3.3 V*	*Controller Area Network signals*		*JX1*	*Direct to Zynq*	*1 Mbps*
ETH	*PHY 0-4*	*N/A*	*Ethernet signals (PHY MDI)*		*JX1*	*Direct to on-board PHY*	*1 Gbps*

Table 9. General specifications of the digital signals available on the high-speed connectors.

ELECTRICAL PWM OUTPUTS (PWM)

32 PWM lanes are available. The first 16 lanes (i.e. #0–15) are available at 3.3 V, while the remaining lanes are based on 1.8 V logic. Two consecutive PWM lanes are by default associated to form a PWM channel with three possible configurations:

- PWMH + PWML: high- and low-side signals with configurable dead time between their '1' states.
- PWM + ACTIVE: PWM and switching authorization signals, i.e. one modulated switching signal and one flag for blocking / unblocking the operation.
- INDEPENDENT: each PWM lane is tied to its own PWM modulator. No dead time is enforced.

Due to the mixed logic voltage levels, the recommended carrier-board schematic includes the level shifting of 1.8 V signals to 3.3 V (or other) logic voltage.
In addition, in order to prevent any possible logic high value during the FPGA boot-up sequence, all PWM signals must be pulled-down with a relatively strong value. When desired, the output enable signal of the level shifter may also be used to gate the PWM signals, possibly by combining the nFLT_OUT signal of the B-Board with some locally-generated fault signal(s).

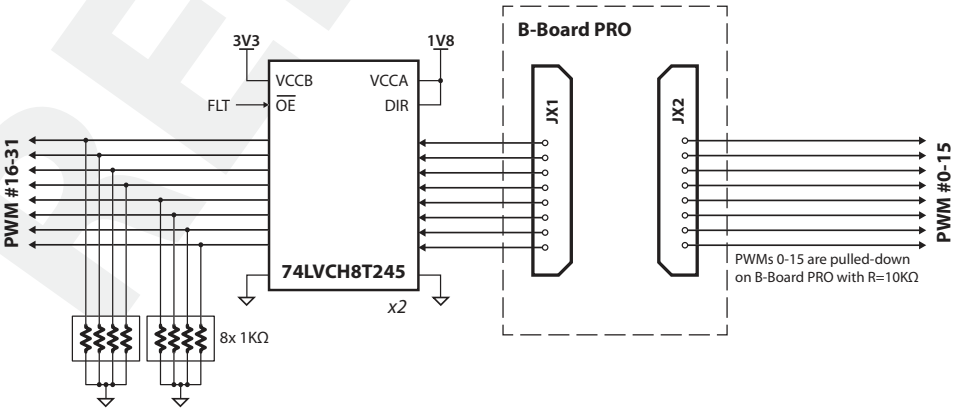


Fig. 8. Recommended carrier schematic (with level shifting) for the PWM signals.

Electrical PWM outputs are engineered to provide a very high accuracy of timings. This is valid inside a PWM channel, across the whole bus and even across all networked B-Boards. Table 10 shows the performance specifications.

Characteristic	Channels	Test conditions	Min.	Typ.	Max.	Unit
Operating voltage	*PWM 0-15 (3.3V)*		*3.0*	*3.3*	*3.6*	*V*
	PWM 16-31 (1.8V)		*1.5*	*1.8*	*2.0*	*V*
Propagation delay asymmetry	*PWM 0-15 (3.3V)*	*Any two signals on same B-Board*			*± 1.6*	*ns*
	PWM 16-31 (1.8V)				*± 2*	*ns*
	Any PWM	*Any two signals on same B-Board*			*± 2.5*	*ns*
		Any two signals across all networked B-Boards			*± 4.5*	*ns*
Relative jitter	*Any PWM*	*Any two signals on same B-Board*			*± 0.4*	*ns*
		Any two signals across all networked B-Boards			*± 0.7*	*ns*

Table 10. Performance specifications of the PWM outputs.

GENERAL-PURPOSE OUTPUTS (GPO)

16 outputs are available, spread between JX1 and JX2. They are tied to the GPO block. All GPO signals are at 3.3 V.

Characteristic	Min.	Typ.	Max.	Unit
Operating voltage		*3.3*	*3.5*	*V*
Current drive capability			*12*	*mA*
Max signal rise / fall time			*± 3*	*ns*
Propagation delay asymmetry, same B-Board			*± 2.5*	*ns*
Propagation delay asymmetry, any B-Board			*0.2*N*	*us*

Table 11. Performance specifications of the GPO outputs.

In some cases, it may be needed to shift the GPO signals to another logic voltage level and / or to improve the current drive capability of each bit. In that case, a similar circuit as shown in Fig. 8 may be considered. Furthermore, the same pull-down resistors may be useful as well.

GENERAL-PURPOSE INPUTS (GPI) AND INCREMENTAL DECODER INPUTS (DEC)

16 outputs are available, spread between JX1 and JX2. They are statically tied to the GPI block as well as the DEC block. All GPI signals are at 3.3 V.

Characteristic	Test conditions	Value	Unit
Maximum tolerable input voltage	*3.3 V*	*3.6*	*V*

Table 12. Performance specifications of the GPI/DEC inputs.

Pin	GPI signal	DEC signal	Pin	GPI signal	DEC signal
JX2 / 105	*GPI 0*	*A0*	*JX1 / 79*	*GPI 8*	*A1*
JX2 / 106	*GPI 1*	*B0*	*JX1 / 80*	*GPI 9*	*B1*
JX2 / 107	*GPI 2*	*Z0*	*JX1 / 81*	*GPI 10*	*Z1*
JX2 / 108	*GPI 3*	*A2 or $\overline{A0}$*	*JX1 / 82*	*GPI 11*	*A3 or $\overline{A1}$*
JX2 / 110	*GPI 4*	*B2 or $\overline{B0}$*	*JX1 / 84*	*GPI 12*	*B3 or $\overline{B1}$*
JX2 / 111	*GPI 5*	*Z2 or $\overline{Z0}$*	*JX1 / 85*	*GPI 13*	*Z3 or $\overline{Z1}$*
JX2 / 112	*GPI 6*	*N/A*	*JX1 / 86*	*GPI 14*	*N/A*
JX2 / 113	*GPI 7*	*N/A*	*JX1 / 87*	*GPI 15*	*N/A*

Table 13. Signal assignment for the GPI / DEC inputs.

FAULT FEEDBACK INPUTS (FLT)

16 digital input lanes are available as fault feedback signals (e.g. for gate drivers). These signals are tied to the fault manager block (FLT), but can also be used as digital inputs from the application software. An additional pre-implemented fault inter-locking also exists. Further details are presented in section "Fault Interlocking signals" on page 10.

Characteristic	Min.	Typ.	Max.	Unit
Response delay to blocking of PWM signals		*50*	*60*	*ns*
Operating voltage	*1.5*	*1.8*	*2.0*	*V*

Table 14. Performance specifications of the fault feedback inputs.

The FLT input lanes are pulled down inside the Zync chip. As such, faults are by default inactive, unless the polarity of the signals is changed to active low by software.

MULTI-FUNCTION ACQUISITION BUS (SPI)

A multi-purpose Serial Peripheral Interface (SPI) bus is available on connector JX1. It is statically tied to the SPI block.

Characteristic	Min.	Typ.	Max.	Unit
Configurable clock frequency			*20*	*MHz*
Current drive capability			*12*	*mA*
Operating voltage	*1.5*	*1.8*	*2.0*	*V*

Table 15. Performance specifications of the SPI bus.

Pins	Name	Direction	Function description
JX1 / 57	*SCLK*	*Output*	*Data sampling clock*
JX1 / 56	*CS*	*Output*	*Chip select strobe*
JX1 / 55	*MISO*	*Input*	*Master In Slave Out data*
JX1 / 54	*MOSI*	*Output*	*Master Out Slave In data*

Table 16. Signal assignment of the SPI bus.

USER-CONFIGURABLE I/O BUS (USR)

The B-Board PRO features a high-speed bus of 36x bidirectional I/Os that is directly accessible from the user-programmable area (inside the Zynq chip). This area, also designated as sandbox offers easy-to-use access from / to the processing cores through the dedicated SBI and SBO blocks.

Characteristic	Min.	Typ.	Max.	Unit
Operating data bitrate (all lanes)			*400*	*Mbps*
Operating voltage	*3.0*	*3.3*	*3.6*	*V*
Current drive capability			*12*	*mA*

Table 17. Performance specifications of the USR bus.

Pins	Name	Dir	Function description
JX2 / 34-37, 39-42	*USR 0-7*	*I/O*	*Any (e.g. data / address)*
JX2 / 9-42, 44-47	*USR 8-15*	*I/O*	*Any (e.g. data / address)*
JX2 / 147-144, 143-139	*USR 16-23*	*I/O*	*Any (e.g. data / address)*
JX2 / 137-134, 132-129	*USR 24-31*	*I/O*	*Any (e.g. data / address)*
JX2 / 153-152, 150-149	*USR 32-35*	*I/O*	*Any (e.g. data / address / strobes)*

Table 18. Signal assignment of the USR bus.

CONTROLLER AREA NETWORK (CAN)

TX and RX signals for CAN communication are available on B-Board PRO. A suitable transceiver is necessary on the carrier board (e.g. TJA1041). In particular cases, it may be interesting to consider galvanically isolate the CAN TX and RX signals for the processing board.

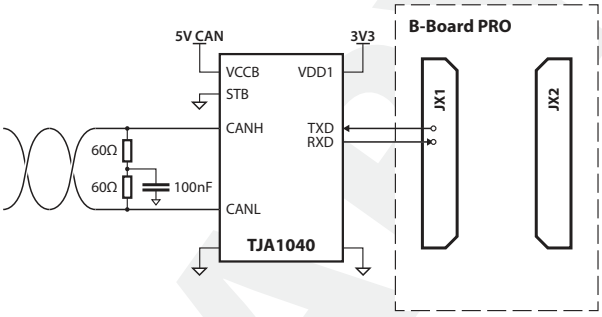


Fig. 9. Recommended carrier schematic for the CAN signals.

Pins	Name	Direction	Function description
JX1 / 176	*CAN TX*	*Output*	*CAN data output*
JX1 / 177	*CAN RX*	*Input*	*CAN data input*

Table 19. Signal assignment of the CAN bus.

ETHERNET COMMUNICATION SIGNALS (PHY)

The utilized PHY is Marvell 88E1512-A0-NNP2I000, which directly provides Ethernet signals on connector JX1, such that only an Ethernet filter is required on the carrier board. Fig. 10 shows the recommended schematic.
Usual high-speed routing techniques used for Gigabit Ethernet connections should preferably be applied. Furthermore, ESD protection measures may be required as well.

Pins	Name	Dir	Function description
JX1 / 20-19	*PHY MDI 0 P/N*	*I/O*	*MDI 0 signals pair*
JX1 / 17-16	*PHY MDI 1 P/N*	*I/O*	*MDI 1 signals pair*
JX1 / 14-13	*PHY MDI 2 P/N*	*I/O*	*MDI 2 signals pair*
JX1 / 12-11	*PHY MDI 3 P/N*	*I/O*	*MDI 3 signals pair*
JX1 / 167	*PHY LED0*	*OUT*	*Status LED 0*
JX1 / 168	*PHY LED1*	*OUT*	*Status LED 1*

Table 20. Signal assignment of the PHY bus.

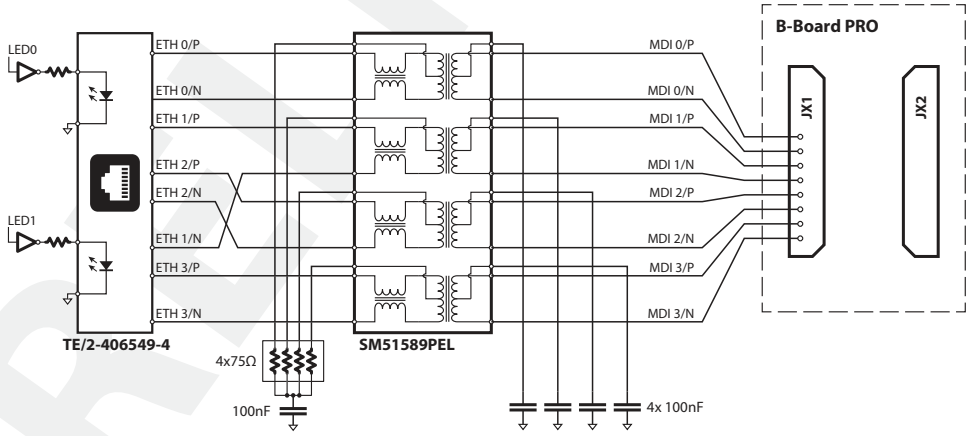


Fig. 10. Recommended carrier schematic for the ETH signals.

FAULT INTERLOCKING SIGNALS

Fault inter-locking allows to coordinate emergency mechanisms between several B-Boards or with other systems. These mechanisms are bi-directional in the sense that they can inform other devices about an internal fault condition or, reciprocally, receive external trigger signals.
In networked configurations, fault inter-locking is intrinsically available thanks to the *RealSync* protocol (SFP links). The interlock involves one fault input and one fault output (see Table 22).

Characteristic	Trigger	Min.	Typ.	Max.	Unit
Response delay to blocking of PWM signals	*nFLT IN*		*40*	*50*	*ns*
	RealSync		*0.2*N*		*µs*

Table 21. Performance specifications of the inter-locking.

Pins	Name	Direction	Level	Function description
JX2 / 31	*nFLT IN*	*Input*	*3.3V*	*Critical fault input flag*
JX2 / 32	*nFLT OUT*	*Output*	*3.3V*	*Critical fault output flag*

Table 22. Signal assignment for the fault inter-locking signals.

FAULT MANAGER

At the firmware level, all fault signals are grouped inside the fault manager, which manages the overall system execution state and controls the activation of the PWM outputs. The collected fault signals include:

» Dedicated fault input lines FLT 0..15 (JX1)
» Interlock (electrical)

BBOS allows to configure the enabling/disabling of each digital fault input line individually through a configuration mask. All signal values (fault flags) can be read from the corresponding VALUES register.

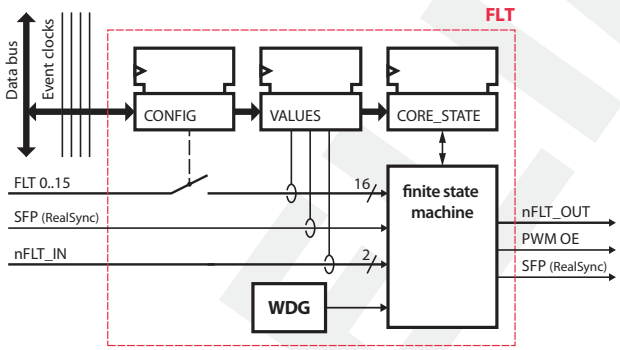


Fig. 11. Internal structure of the FLT peripheral block.

CLOCK AND INTERRUPT GENERATORS

Four independent clock generators are available on B-Board PRO. They allow to configure independent time bases that can be allocated to various FPGA peripherals. This guarantees a very strict management of frequencies and phase-shifts between blocks. Clock generators support glitch-less re-configuration during run-time (variable-frequency). Outputs of clock generators are either interrupt signals or reference clocks for pulse-width modulators. Typical configurations include:

» **Basic example**: Control, modulation and sampling are at the same frequency. All resources are mapped onto the same clock generator. Measurements are made in the middle of the current ripple.
» **Multi-frequency example**: Two distinct converters are switching at different frequencies (e.g. 4 kHz and 5 kHz). Sampling is done at a common multiple (e.g. 20 kHz).
» **Variable-frequency**: One variable-frequency generator is used for modulation. Another frequency generator is used at a constant frequency for sampling and control.

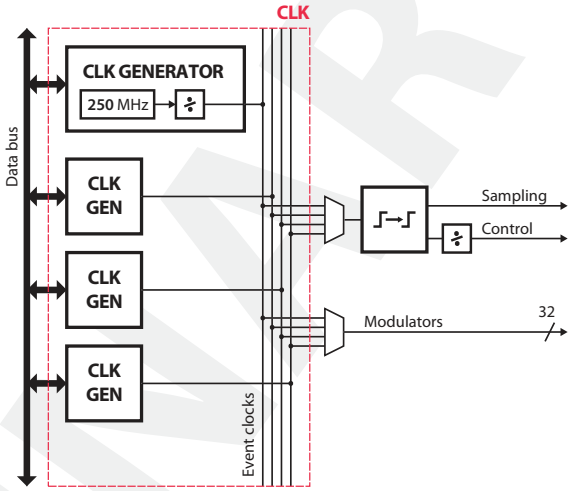


Fig. 12. Internal structure of the CLK peripheral block.

Characteristic	Value
Counter resolution	*4.0 ns*
Counter depth (carrier, prescaler)	*16 bits*
Postscaler value (IRQ subsystem)	*0 – 4095*
Achievable frequency range	*58.2 mHz – 250 MHz*

Table 23. Performance specifications of the CLK peripheral block.

In a multi-device configuration (with networked B-Boards), all clock generators are intrinsically syntonized and automatically synchronized. This way, all phase-dependent operations such as sampling (ADC) or modulation (PWM) are guaranteed to have extremely accurate timings. Achievable performance is shown in Table 24 and illustrated in Fig. 13.

Characteristic	Min.	Typ.	Max.	Unit
Mean deviation, any slave B-Board vs. master	*-2.0*	*0*	*2.0*	*ns*
Phase noise (jitter), any B-Board, 3σ		*± 230*		*ps*

Table 24. Synchronization performance of CLK peripheral blocks across multiple B-Boards using *RealSync*.

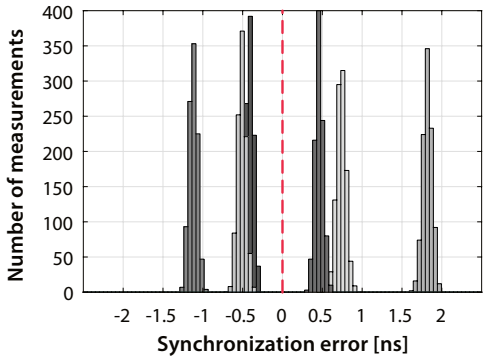


Fig. 13. Relative phase error performance with several B-Boards in a stacked configuration (example with 6 slaves units).

PULSE WIDTH MODULATORS

The B-Board PRO embeds a full PWM signal generation system, featuring five sub-systems. Each of them generates 32 PWM signals. Fig. 14 depicts the corresponding structure:

- CB-PWM: Carrier-based modulators (32 channels). Various types of carriers are available, with single or double update rate. The CB-PWM block also provide hardware support for space-vector modulation (SV-PWM).
- PP-PWM: Programmed patterns modulators (2x three-phase, Xx angles, up to Yx levels). They allow the implementation of Selective Harmonic Elimination (SHE) or other types of Optimized Pulse Patterns (OPP).
- DO-PWM: Direct outputs. The direct access to the output state ('1' or '0') typically enables the implementation of software-modulated techniques such as Model Predictive Control (MPC). This also allows to use PWM outputs as standard digital outputs (possibly with dead time).
- SS-PWM: Sort-and-Select modulation and balancing (2 arms of up to 8 modules). This sub-system offers hardware-level support for the operation of Modular Multilevel Converters or similar topologies.
- SB-PWM: Sandbox. This FPGA area is left available for the implementation of fully-customized modulation techniques, while providing drivers for an easy-to-use access from the software level.

At the output, each of the 32 PWM signals can be directly propagated to the physical outputs (electrical or optical), or to go through a dead time generator.
This results in 32 PWM lanes. By default, lanes are also arranged into 16 pairs of adjacent lanes designated as channels. Within a channel, odd lanes are always low-side signals, while even lanes are always high-side. PWM lanes #0-31 are available from the electrical connectors, while only PWM lanes #0-15 are produced on the optical outputs.
Dead time is obtained by delaying the rising edge of each PWM signal within a given pair. This results in an equivalent propagation delay of half the dead time.

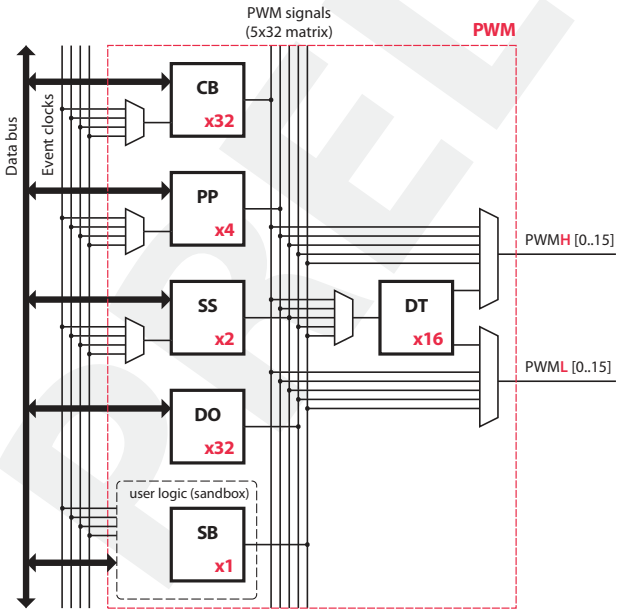


Fig. 14. Internal structure of the PWM signals generation block.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 25. Performance specifications of the dead time generation.

Channel	0	1	2	...	7	8	9	10	...	15
Lane	*0*	*2*	*4*	*...*	*14*	*16*	*18*	*20*	*...*	*30*
	1	*3*	*5*	*...*	*15*	*17*	*19*	*21*	*...*	*31*

Table 26. Designation of the PWM lanes and channels.

CB-PWM: CARRIER-BASED MODULATION

Carrier-based modulators offer the simplest way to generate pulse-width modulated signals. The corresponding subsystem features 32 independent modulators, which offer independent duty-cycle and phase parameters as well as four different types of carriers. With triangular carriers, modulators can be configured with single or double update rates (once or twice per PWM period).

Characteristic	Value
Counter depth	*16 bits*
Edge resolution (counter resolution)	*4 ns*

Table 27. Performance specifications of the CB-PWM block.

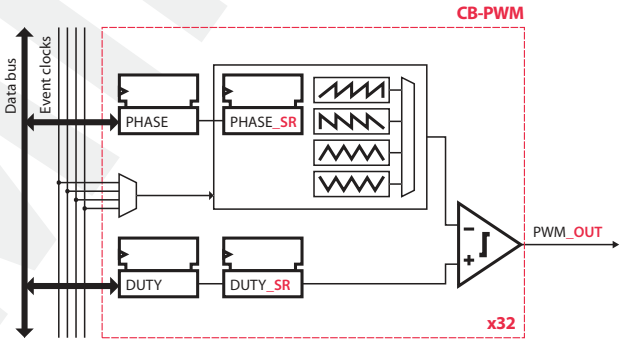


Fig. 15. Internal structure of the CB-PWM peripheral block.

SV-PWM: SPACE VECTOR MODULATION

Space vector modulation (sometimes referred to as SVM) is supported through dedicated software drivers, making use of the same resources as the CB-PWM subsystem. Indeed, once the closed vectors have been identified and the suitable sequence determined, the switching events can be easily produced by suitably-programmed modulators. SV-PWM automatically configures adjacent lanes or channels and supports single or double update rates.

SS-PWM: SORT-AND-SELECT MODULATION FOR MODULAR MULTILEVEL CONVERTERS (MMC)

Modulation with integrated voltage balancing for multilevel converters is supported at the firmware level thanks to the SS-PWM block. It applies to Modular Multilevel Converters as well as similar topologies with floating submodules.
This subsystem accesses the voltages acquired on the analog inputs in order to sort the submodule voltages and allocate the switching events to the suitable submodule as a function of the current polarity.
The SS-PWM block is compatible with half- and full-bridge

submodule topologies and hence with both positive and negative arm voltages. The pre-implemented solution also guarantees that only one submodule switches at a given time in order to minimize switching losses and optimize the ratio between apparent and actual switching frequencies. Finally, the firmware also supports the exclusion of one or several submodules from the modulation process, as required by most fault-tolerant operation mechanisms.

Characteristic	Symbol	Value
Number or submodule per converter arm	*N*	*4, 8, 16 (–bypass)*
Number of output voltage levels	*L*	*N+1 or 2N+1*
Switching frequency range	f_{sw}	*3.72 Hz – 1 MHz*
PWM edge resolution		*20 ns*

Table 28. Performance specifications of the SS-PWM block.

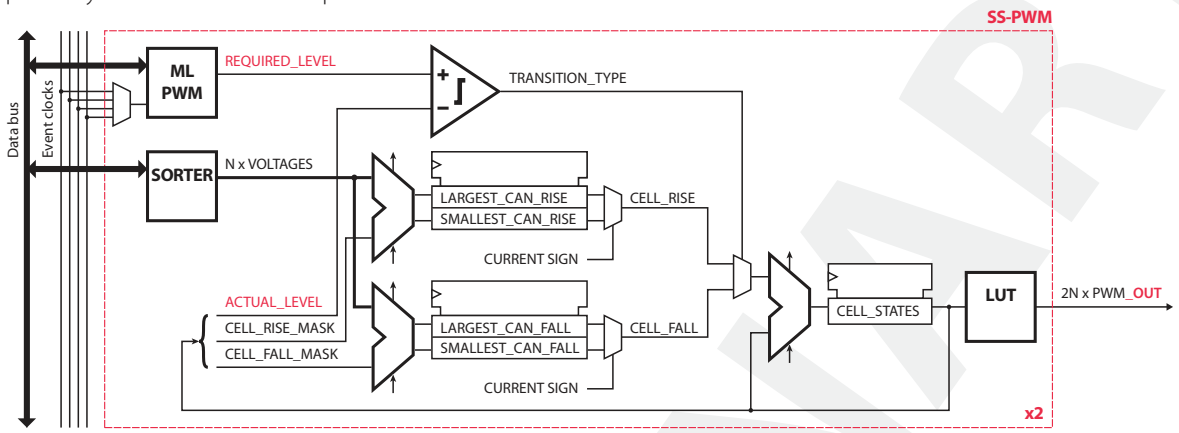


Fig. 23. Internal structure of the SS-PWM peripheral block.

SB-PWM : SANDBOX FOR OTHER TECHNIQUES

In addition to existing modulators, the B-Board also features a user-programmable area inside the FPGA . This notably allows to implement special own modulation techniques.
In this sandbox, data read and write access from / to the CPU is provides from the the SBI and SBO blocks, respectively (see "User-programmable area (Sandbox)" on page 16).
The SB-PWM subsystem itself allows to connect to the PWM lanes through the dead-time generator block (see Fig. 13) as well as the B-Box's hardware protection mechanisms.

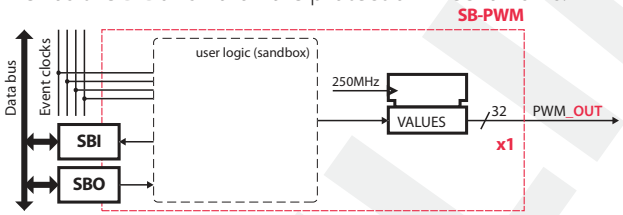


Fig. 16. Internal structure of the SB-PWM block.

DO-PWM : DIRECT OUTPUT ACCESS

Direct access to the PWM outputs is supported by the DO-PWM subsystem. It distinguishes from the SB-PWM in the sense that it is pre-implemented and requires no HDL editing. PWM state values (0 or 1) can be written directly from the CPU cores. This may typically be useful for model-predictive control (MPC) or sliding mode control techniques such as direct torque control (DTC).
Similarly to all PWM subsystems, when used as a channel, output lanes benefit from the dead-time generator block as well as protective mechanisms.

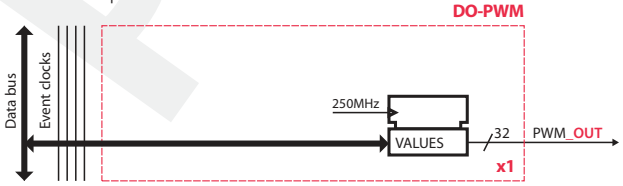


Fig. 17. Internal structure of the DO-PWM block.

PP-PWM : PROGRAMMED PATTERNS MODULATION

The programmed pattern blocks support modulation techniques that rely on pre-defined switching instants such as the generation of firing angles on a thyristor-based converter, the implementation of Selective Harmonic Elimination (SHE) or any Optimized Pulse Pattern (OPP). Three-phase system up to X levels are supported.
PP-PWM have a fixed counter period (hence angular resolution), but can nevertheless be fed by variable-frequency clocks (see CLK peripheral block), typically aiming to be integrated withing a software PLL.
Each PP-PWM block contains several look up tables (LUT) for switching angles, registers for indicating the direction (up or down) of each switching event, as well as an additional truth table for decoding the output state.
Obviously, the PP-PWM blocks are meant for accelerating the run time execution of OPP-based modulation and not for supporting the computation of the associated optimization algorithms.

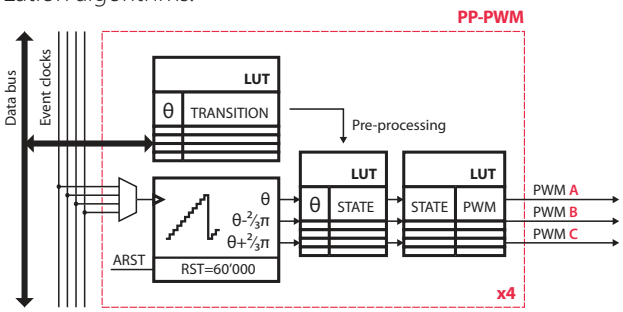


Fig. 18. Internal structure of the SS-PWM block.

Characteristic	Value
Number of angle registers (values 0 – 60'000)	*3x 16 angles x 16 bits*
Number of transition direction bits registers (up or down)	*3x 16 bits*
Edge resolution (respectively to signal period)	*0.017 ‰*

Table 29. Performance specifications of the PP-PWM block.

DEAD TIME GENERATION SUBSYSTEM

As depicted by Fig. 14, the PWM block features a dead time generator at its output. This subsystem can be either used or bypassed by picking-up the signals from the PWM signals matrix directly (outputs of the modulators). As such, signals from all five PWM subsystems can be routed to the physical outputs (electrical only on B-Board).

The dead time generation relies on a finite state machine operating as depicted in Fig. 19. Essentially, rising edges of the high-side and low-side signals are delayed by a programmable amount of time. This results in an equivalent propagation delay of half the dead time.

Intrinsically, this implementation guarantees that a signal pulse shorter than the dead time value is not produced.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 30. Performance specifications of the dead time generation.

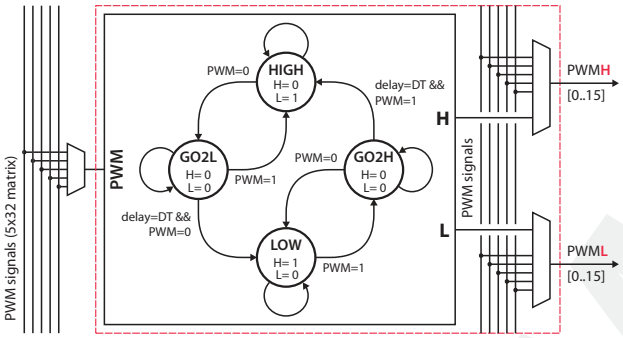


Fig. 19. Internal structure of the dead time generation block.

DATA TRANSFER PERFORMANCE

The transfer of continuously-updated modulation parameters from the processing core to the distributed modulators causes delays, which depend on the amount of data to be transferred. Fig. 20 shows the achieved performance with respect to the update of the CB-PWM block. Other modulators perform similarly.

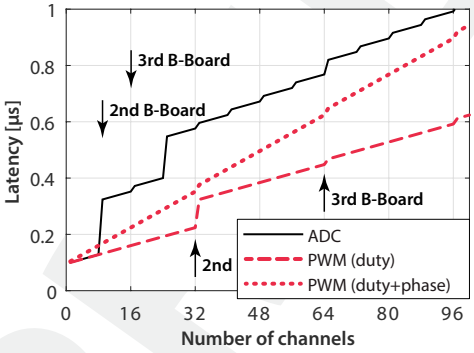


Fig. 20. Data transfer delay, as a function of the number of channels and number of B-Boards.

USER-PROGRAMMABLE AREA (SANDBOX)

The B-Board is designed such that its FPGA area (PL) can embed user-defined logic. This allows for the implementation of special modulation techniques, proprietary communication mechanisms, or interfacing with external hardware. Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from / to the CPU cores:

- SBI: Input from the sandbox
- SBO: Output to the sandbox

Also, the sandbox offers connectivity to the following I/O:

- ADC values (16x 16 bits signed integers)
- SB-PWM signals (32 bits register)
- Internal clocks
- Physical I/Os (FLT, USR, GPI, GPO)

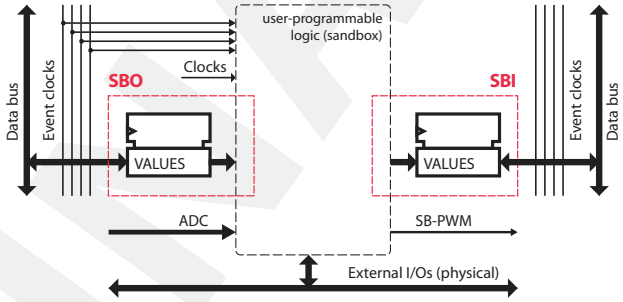


Fig. 21. Internal structure of the SBI and SBO blocks.

Thanks to the *RealSync* communication and synchronization protocol, the sandbox can be used indistinctively on the master or a slave B-Box within a control network. The data transfers (read or write) from the CPU core is handled by the SBI or SBO blocks using either the write-through (configuration) or write-back (real-time) data traffic, as with any other peripheral block.

C/C++ drivers (as well as their blockset counterparts) are readily available within the software development kits (SDKs). On the programmable logic side, development templates are provided upon request. In the provided HDL source code, other peripheral blocks are obfuscated.

INCREMENTAL DECODERS

The B-Board features decoder inputs for quadrature-encoder speed / position sensor signals (usually called A and B), with or without a reset line (usually called Z). These inputs are either configurable as four independent sensor inputs or two differential inputs.

The decoder module counts all 4 edges of the A and B inputs, leading to an angular resolution 4 times better than the PPR value usually specified for a given encoder. Additionally, the position can be latched with a sampling, similar to the sample and hold feature of the ADC inputs.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input signals	• *Single-ended signalling : A, B and Z (Z is optional)* • *Differential signalling : A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$ ($\overline{Z}$ are optional)*				
Sampling options	*Either synchronized with ADC, or independent*				
PPR frequency	*Quadruple rate.*	*0*		*5*	*MHz*

Table 31. Performance specifications of the DEC block.

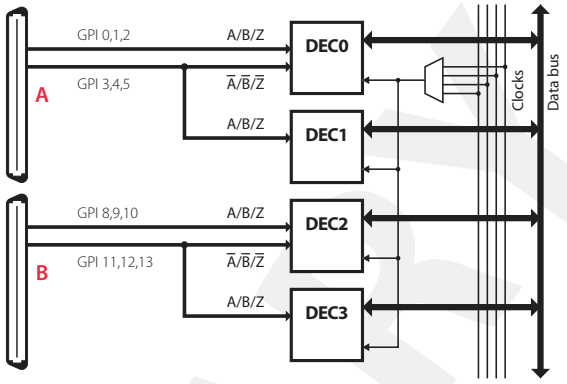


Fig. 22. Device mapping and configuration of the four incremental speed / position sensors decoders.

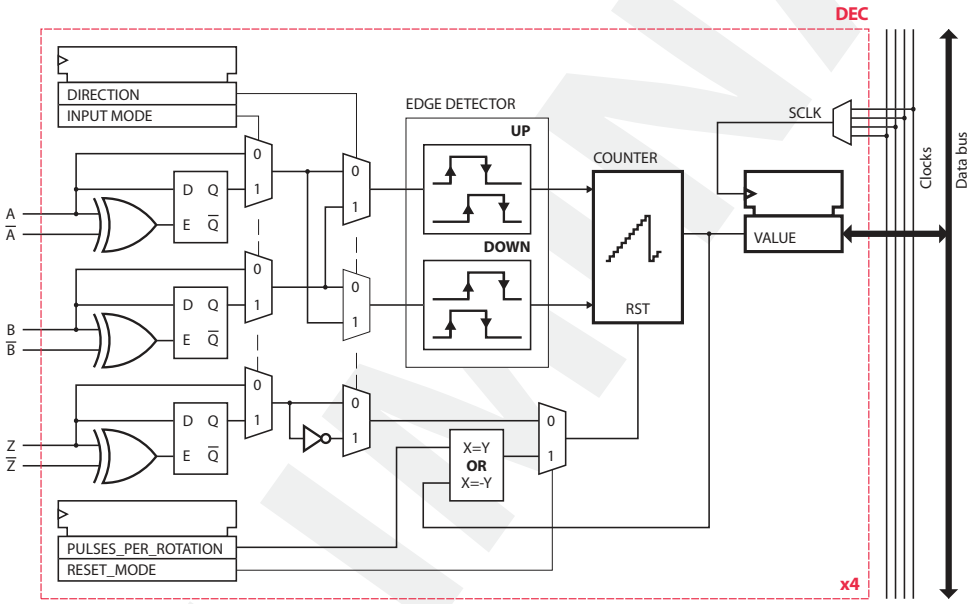
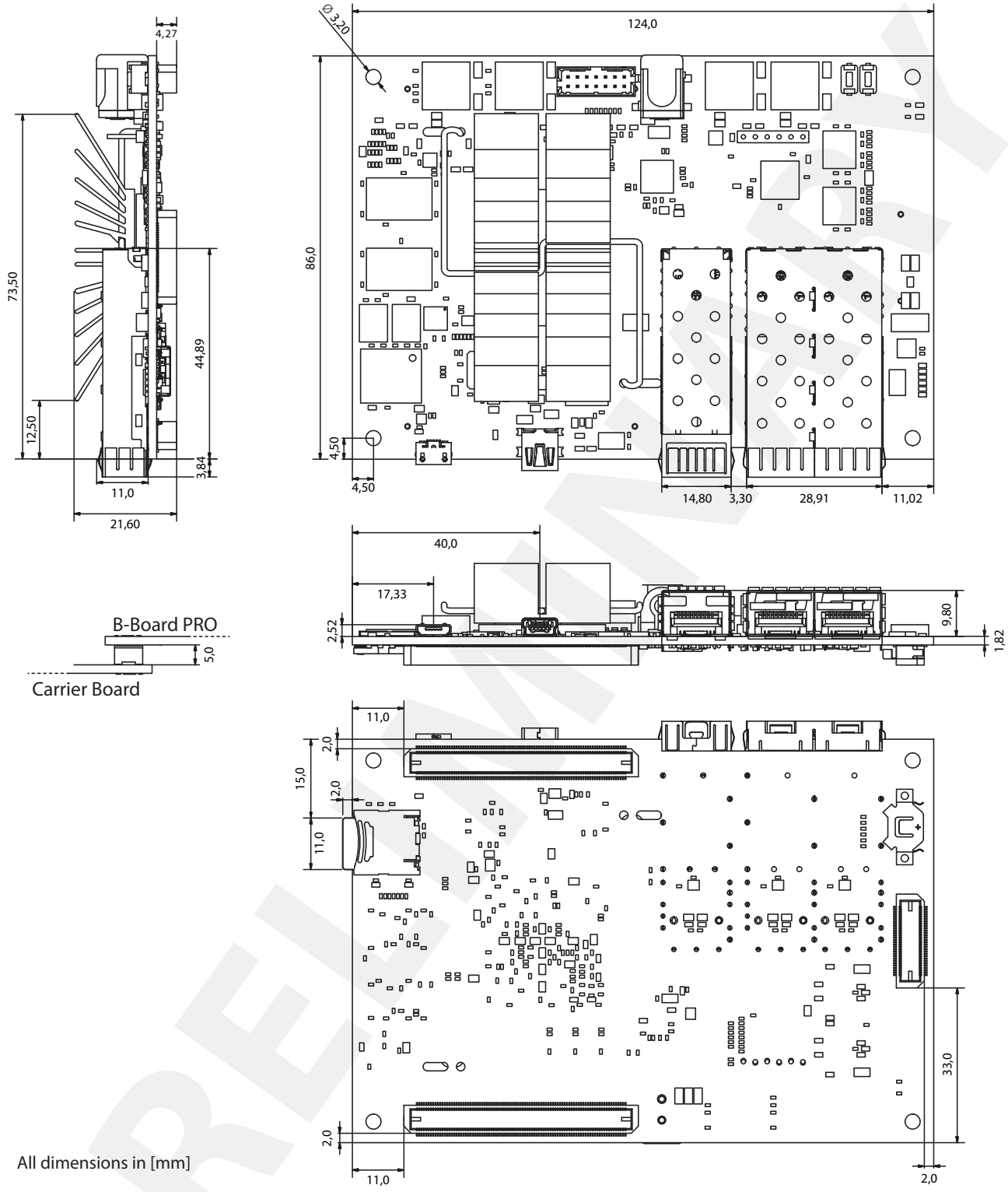


Fig. 24. Internal structure of the DEC block.

MECHANICAL DATA



All dimensions in [mm]

Fig. 25. Mechanical dimensions of B-Board PRO

CONNECTOR JX1

Dir.	Level	Function	Pins	Pins	Function	Level	Dir.
GND			90-88	91-93	GND		
IN	3,3V	GPI 15	87	94	GPO 15	3,3V	OUT
IN	3,3V	GPI 14	86	95	GPO 14	3,3V	OUT
IN	3,3V	GPI 13	85	96	GPO 13	3,3V	OUT
IN	3,3V	GPI 12	84	97	GPO 12	3,3V	OUT
GND			83	98	GND		
IN	3,3V	GPI 11	82	99	GPO 11	3,3V	OUT
IN	3,3V	GPI 10	81	100	GPO 10	3,3V	OUT
IN	3,3V	GPI 9	80	101	GPO 9	3,3V	OUT
IN	3,3V	GPI 8	79	102	GPO 8	3,3V	OUT
GND			78	103	GND		
IN	1,8V	FLT 0	77	104	PWM 16	1,8V	OUT
IN	1,8V	FLT 1	76	105	PWM 17	1,8V	OUT
IN	1,8V	FLT 2	75	106	PWM 18	1,8V	OUT
IN	1,8V	FLT 3	74	107	PWM 19	1,8V	OUT
GND			73	108	GND		
IN	1,8V	FLT 4	72	109	PWM 20	1,8V	OUT
IN	1,8V	FLT 5	71	110	PWM 21	1,8V	OUT
IN	1,8V	FLT 6	70	111	PWM 22	1,8V	OUT
IN	1,8V	FLT 7	69	112	PWM 23	1,8V	OUT
GND			68	113	GND		
IN	1,8V	FLT 8	67	114	PWM 24	1,8V	OUT
IN	1,8V	FLT 9	66	115	PWM 25	1,8V	OUT
IN	1,8V	FLT 10	65	116	PWM 26	1,8V	OUT
IN	1,8V	FLT 11	64	117	PWM 27	1,8V	OUT
GND			63	118	GND		
IN	1,8V	FLT 12	62	119	PWM 28	1,8V	OUT
IN	1,8V	FLT 13	61	120	PWM 29	1,8V	OUT
IN	1,8V	FLT 14	60	121	PWM 30	1,8V	OUT
IN	1,8V	FLT 15	59	122	PWM 31	1,8V	OUT
GND			58	123	GND		
OUT	1,8V	SPI SCLK	57	124	RSVD	1,8V	IN
OUT	1,8V	SPI CS	56	125	RSVD	1,8V	IN
IN	1,8V	SPI MISO	55	126	RSVD	1,8V	IN
OUT	1,8V	SPI MOSI	54	127	RSVD	1,8V	IN
GND			53	128	GND		
OUT	1,8V	RSVD	52-51	129-130	RSVD	1,8V	OUT
GND			50	131	GND		
I/O	1,8V	RSVD	49-48	132-133	RSVD	1,8V	I/O
GND			47	134	GND		
I/O	1,8V	RSVD	46-45	135-136	RSVD	1,8V	I/O
GND			44	137	GND		
I/O	1,8V	RSVD	43-42	138-139	RSVD	1,8V	I/O
GND			41	140	GND		
IN	1,8V	RSVD	40-38	141-144	RSVD	1,8V	IN
GND			36	145	GND		
IN	1,8V	RSVD	35-32	146-147	RSVD	1,8V	IN
GND			31	150	GND		
IN	1,8V	RSVD	30-27	151-154	RSVD	1,8V	IN
GND			26	155	GND		
IN	1,8V	RSVD	25-22	156-159	RSVD	1,8V	IN

Dir.	Level	Function	Pins	Pins	Function	Level	Dir.
GND			21	160	GND		
I/O	N/A	PHY 0P	20	161	RSVD		
I/O	N/A	PHY 0N	19	162	RSVD		
GND			18	163	GND		
I/O	N/A	PHY 1P	17	164	RSVD		
I/O	N/A	PHY 1N	16	165	RSVD		
GND			15	166	GND		
I/O	N/A	PHY 2P	14	167	PHY LED 0	N/A	I/O
I/O	N/A	PHY 2N	13	168	PHY LED 1	N/A	I/O
GND			12	169	GND		
I/O	N/A	PHY 3P	11	170	OTG VBUS	N/A	I/O
I/O	N/A	PHY 3N	10	171	OTG VBUS	N/A	I/O
GND			9	172	GND		
	3,3V	OTG DN	8	173	RSVD		
	3,3V	OTG DP	7	174	RSVD		
GND			6	175	GND		
	3,3V	OTG ID	5	176	CAN TX	3,3V	OUT
	3,3V	OTG CPEN	4	177	CAN RX	3,3V	IN
GND			3-1	178-180	GND		

Table 32. Detailed pinout specification for connector JX1

CONNECTOR JX2

Dir.	Level	Function	Pins	Pins	Function	Level	Dir.
GND			1-3	180-178	GND		
GND			4	177	CID 0	3,3V	IN
OUT	CML	GTX TX3N	5	176	CID 1	3,3V	IN
OUT	CML	GTX TX3P	6	175	CID 2	3,3V	IN
GND			7	174	GND		
GND			8	173	5 – 17 VDC		PWR
IN	CML	GTX RX3N	9	172	5 – 17 VDC		PWR
IN	CML	GTX RX3P	10	171	5 – 17 VDC		PWR
GND			11	170	5 – 17 VDC		PWR
GND			12	169	GND		
PWR	5 – 17 VDC		13-16	168-165	5 – 17 VDC		PWR
GND			17	164	GND		
PWR	5 – 17 VDC		18-21	163-160	5 – 17 VDC		PWR
GND			22	159	GND		
PWR	5 – 17 VDC		23-26	158-155	5 – 17 VDC		PWR
GND			27	154	GND		
OUT	3,3V	BB RDY	28	153	USR 32	3,3V	I/O
IN	3,3V	MB RDY	29	152	USR 33	3,3V	I/O
GND			30	151	GND		
IN	3,3V	nFLT IN	31	150	USR3 4	3,3V	I/O
OUT	3,3V	nFLT OUT	32	149	USR 35	3,3V	I/O
GND			33	148	GND		
I/O	3,3V	USR 0	34	147	USR 16	3,3V	I/O
I/O	3,3V	USR 1	35	146	USR 17	3,3V	I/O
I/O	3,3V	USR 2	36	145	USR 18	3,3V	I/O
I/O	3,3V	USR 3	37	144	USR 19	3,3V	I/O
GND			38	143	GND		

Dir.	Level	Function	Pins	Pins	Function	Level	Dir.
I/O	3,3V	USR 4	39	142	USR 20	3,3V	I/O
I/O	3,3V	USR 5	40	141	USR 21	3,3V	I/O
I/O	3,3V	USR 6	41	140	USR 22	3,3V	I/O
I/O	3,3V	USR 7	42	139	USR 23	3,3V	I/O
GND			43	138	GND		
I/O	3,3V	USR 8	44	137	USR 24	3,3V	I/O
I/O	3,3V	USR 9	45	136	USR 25	3,3V	I/O
I/O	3,3V	USR 10	46	135	USR 26	3,3V	I/O
I/O	3,3V	USR 11	47	134	USR 27	3,3V	I/O
GND			48	133	GND		
I/O	3,3V	USR 12	49	132	USR 28	3,3V	I/O
I/O	3,3V	USR 13	50	131	USR 29	3,3V	I/O
I/O	3,3V	USR 14	51	130	USR 30	3,3V	I/O
I/O	3,3V	USR 15	52	129	USR 31	3,3V	I/O
GND			53	128	GND		
I/O	3,3V	RSVD	54-58	127-123	RSVD	N/A	I/O
GND			59	122	GND		
I/O	3,3V	RSVD	60-62	121-119	RSVD	3,3V	I/O
GND			63	118	GND		
I/O	3,3V	RSVD	64-66	117-115	RSVD	3,3V	I/O
GND			67	114	GND		
OUT	3,3V	GPO 7	68	113	GPI 7	3,3V	IN
OUT	3,3V	GPO 6	69	112	GPI 6	3,3V	IN
OUT	3,3V	GPO 5	70	111	GPI 5	3,3V	IN
OUT	3,3V	GPO 4	71	110	GPI 4	3,3V	IN
GND			72	109	GND		
OUT	3,3V	GPO 3	73	108	GPI 3	3,3V	IN
OUT	3,3V	GPO 2	74	107	GPI2	3,3V	IN
OUT	3,3V	GPO 1	75	106	GPI 1	3,3V	IN
OUT	3,3V	GPO 0	76	105	GPI 0	3,3V	IN
GND			77	104	GND		
OUT	3,3V	PWM 0	78	103	PWM 8	3,3V	OUT
OUT	3,3V	PWM 1	79	102	PWM 9	3,3V	OUT
OUT	3,3V	PWM 2	80	101	PWM 10	3,3V	OUT
OUT	3,3V	PWM 3	81	100	PWM 11	3,3V	OUT
GND			82	99	GND		
OUT	3,3V	PWM 4	83	98	PWM 12	3,3V	OUT
OUT	3,3V	PWM 5	84	97	PWM 13	3,3V	OUT
OUT	3,3V	PWM 6	85	96	PWM 14	3,3V	OUT
OUT	3,3V	PWM 7	86	95	PWM 15	3,3V	OUT
GND			87-90	94-91	GND		

Table 33. Detailed pinout specification for connector JX2

CONNECTOR JX3

Dir.	Function	Pins	Pins	Function	Dir.
GND		1	60	GND	
	N/A	2-3	59-58	N/A	
GND		4	57	GND	
	N/A	5-8	56-53	N/A	
GND		9	52	GND	
IN	5.0 V	10-11	51-50	5.0 V	IN
GND		12	49	GND	
IN	5.0 V	13-14	48-47	5.0 V	IN
GND		15	46	GND	
IN	5.0 V	16-17	45-44	5.0 V	IN
GND		18	43	GND	
IN	AIN 3P	19	42	AIN 7P	IN
IN	AIN 3N	20	41	AIN 7N	IN
GND		21	40	GND	
IN	AIN 2P	22	39	AIN 6P	IN
IN	AIN 2N	23	38	AIN 6N	IN
GND		24	37	GND	
IN	AIN 1P	25	36	AIN 5P	IN
IN	AIN 1N	26	35	AIN 5N	IN
	GND	27	34	GND	
IN	AIN 0P	28	33	AIN 4P	IN
IN	AIN 0N	29	32	AIN 4N	IN
GND		30	31	GND	

Table 34. Detailed pinout specification for connector JX3

REVISION HISTORY

- 14.01.20: Initial release
- 10.02.20: Additional details regarding the SBI, SBO and SB-PWM blocks.
- 20.04.20: Clarification on ADC inputs.

This product must be used in electric / electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.
Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and / or cause serious damage. All conducting parts must be inaccessible after installation.

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ABOUT US

Imperix Ltd is a company established in Sion, Switzerland. Its name is derived form the Latin verb imperare, which stands for controlling and refers to the company's core business: the control of power electronic systems. Imperix commercializes hardware and software solutions related to the fast and secure implementation of pilot systems and plants in the field of power conversion, energy storage and smart grids.

NOTE

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