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November 2013



FQB5N50C

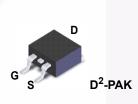
N-Channel QFET[®] MOSFET 500 V, 5 A, 1.4 Ω

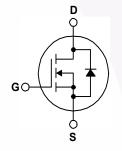
Features

- + 5 A, 500 V, $R_{DS(on)}$ = 1.4 Ω (Max.) @ V_{GS} = 10 V, I_D = 2.5 A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 15 pF)
- 100% Avalanche Tested
- RoHS Compliant

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQB5N50CTM	Unit
V _{DSS}	Drain-Source Voltage		500	V
	Drain Current - Continuous ($T_c = 25^{\circ}C$)		5	A
ID	- Continuous (T _C = 100°C)		2.9	А
I _{DM}	Drain Current - Pulsed	(Note 1)	20	A
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		300	mJ
I _{AR}	Avalanche Current	(Note 1)	5	A
E _{AR}	Repetitive Avalanche Energy (No		7.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
D	Power Dissipation (T _C = 25°C)		73	W
PD	- Derate above 25°C		0.58	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
TL	Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds		300	°C
۱L			500	

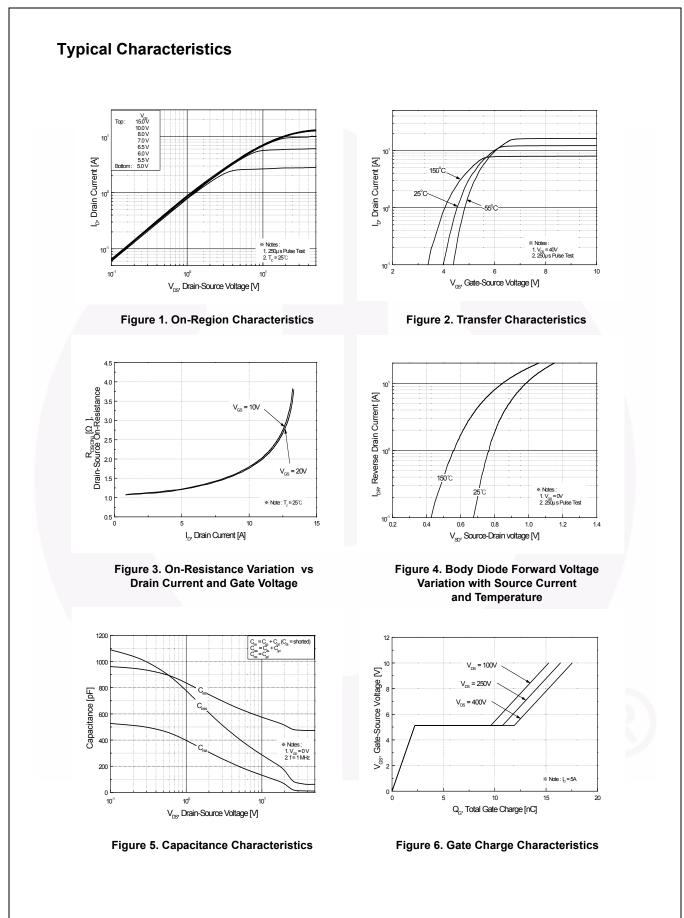
Thermal Characteristics

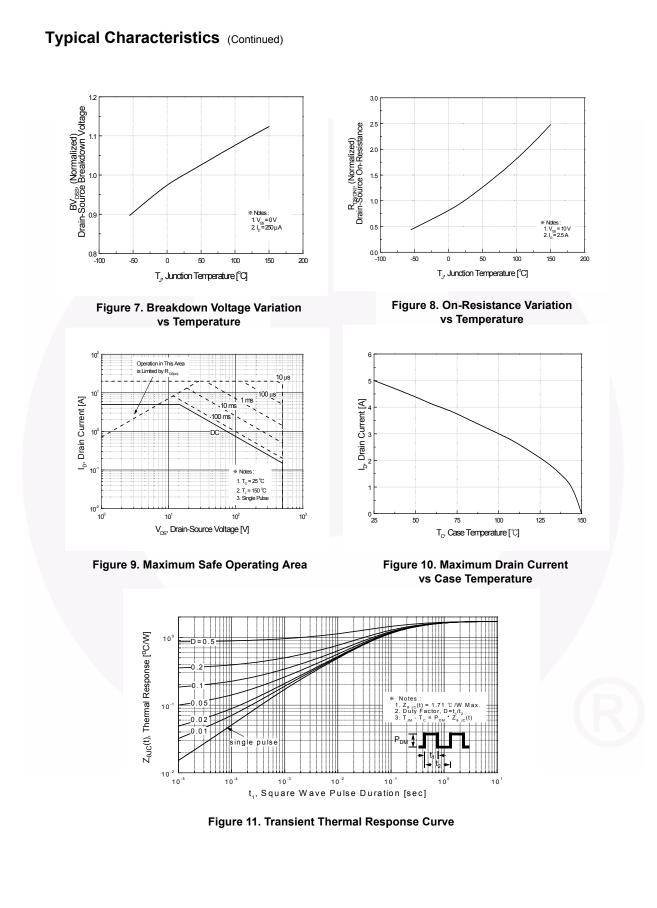
Symbol	Parameter	FQB5N50CTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max. 1.71		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	C/W

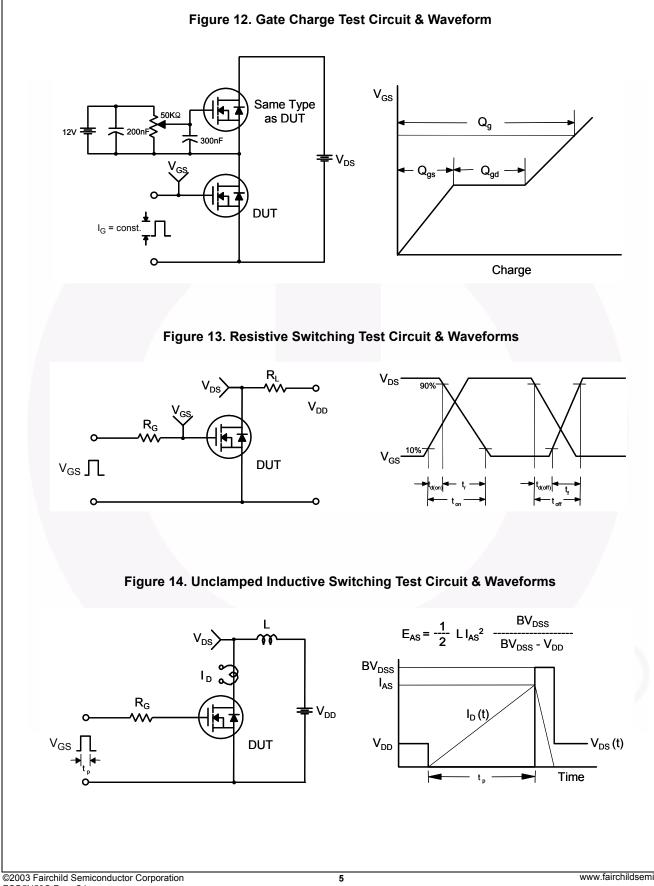
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Device MarkingDeviceFQB5N50CFQB5N50CTM		PackageReel SizeD2-PAK330 mm		Tape Width 24 mm		Quantity 800 units		
								lectri
Symbol		Parameter		Conditions	Min	Тур	Max	Unit
Off Cha	aracteristic	`e						
BV _{DSS}		ce Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		500			V
∆BV _{DSS}		Voltage Temperature	$I_D = 250 \ \mu\text{A}$, Referenced to 25°C					
ΔT_{J}	Coefficient	volage temperature				0.5		V/°C
I _{DSS}	Zero Gate Voltage Drain Current		V_{DS} = 500 V, V_{G}				1	μA
000			V _{DS} = 400 V, T _C = 125°C			1	10	μA
GSSF		Leakage Current, Forward	V_{GS} = 30 V, V_{DS}				100	nA
GSSR	Gate-Body	Leakage Current, Reverse	V_{GS} = -30 V, V_{DS}	_S = 0 V			-100	nA
On Cha	racteristic	s						
V _{GS(th)}	Gate Thres	hold Voltage	$V_{DS} = V_{GS}, I_D =$	250 μA	2.0		4.0	V
R _{DS(on)}	Static Drain On-Resista		V _{GS} = 10 V, I _D =	2.5A		1.14	1.4	Ω
JFS		ansconductance	V _{DS} = 40 V, I _D =	2.5A		5.2		S
Dynam C _{iss} C _{oss} C _{rss}	ic Charact	citance	V _{DS} = 25 V, V _{GS} f = 1.0 MHz	= 0 V,		480 80 15	625 105 20	pF pF
						15	20	рг
Switch	ing Charac				1		I	
d(on)	Turn-On De		V _{DD} = 250 V, I _D	= 5A,		12	35	ns
r	Turn-On Ris		R _G = 25 Ω			46	100	ns
d(off)	Turn-Off De	•	-	(Note 4)		50	110	ns
f	Turn-Off Fa					48	105	ns
כ ^ק	Total Gate ($V_{DS} = 400 V, I_{D}$	= 5A,		18	24	nC
ב _{gs} ב	Gate-Sourc		V _{GS} = 10 V	(Note 4)		2.2 9.7		nC nC
2 _{gd}	Gate-Drain	Charge		(Note 4)		9.7		nc
Drain-S	ource Dio	de Characteristics a	nd Maximum I	Ratings				
S		Im Continuous Drain-Source Diode Forward Current				5	Α	
SM		Pulsed Drain-Source Diode F					20	A
/ _{SD}		e Diode Forward Voltage	V _{GS} = 0 V, I _S = 5 A				1.4	V
rr		covery Time	$V_{GS} = 0 V, I_{S} = 5$			263		ns
ג _{יי}	Reverse Re	covery Charge	dI _F / dt = 100 A/µ	us		1.9		μC
DTES:		n limited by maximum junction tempe						

FQB5N50C — N-Channel QFET[®] MOSFET







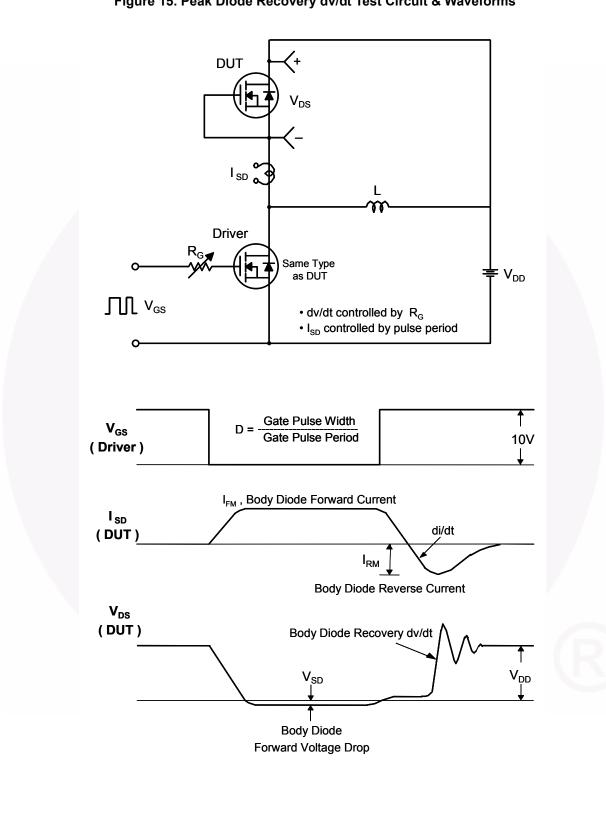


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

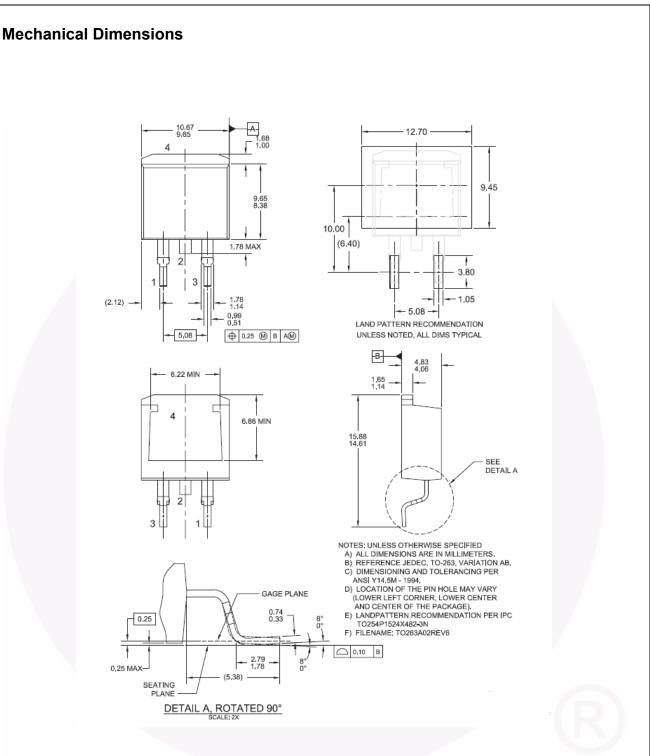


Figure 16. TO263 (D²PAK), Molded, 2-Lead, Surface Mount

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FQB5N50C — N-Channel QFET[®] MOSFET



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FPS™		SyncFET™	VoltagePlus™ XS™
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