Product Specification

PE42540

UltraCMOS® SP4T RF Switch
10 Hz–8 GHz

Product Description

The PE42540 is a HaRP™ technology-enhanced absorptive SP4T RF switch developed on UltraCMOS® process technology. This switch is designed specifically to support the requirements of the test equipment and ATE market. It comprises four symmetric RF ports and has very high isolation. An on-chip CMOS decode logic facilitates a two-pin low voltage CMOS control interface and an optional external V_{SS} feature. High ESD tolerance and no blocking capacitor requirements make this the ultimate in integration and ruggedness.

The PE42540 is manufactured on PSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™ technology enhanced
  - Fast settling time
  - Eliminates gate and phase lag
  - No drift in insertion loss and phase
- High linearity: 58 dBm IIP3
- Low insertion loss: 0.8 dB @ 3 GHz, 1.0 dB @ 6 GHz and 1.2 dB @ 8 GHz
- High isolation: 45 dB @ 3 GHz, 39 dB @ 6 GHz and 31 dB @ 8 GHz
- Maximum power handling: 30 dBm @ 8 GHz
- High ESD tolerance of 2 kV HBM on RFC and 1 kV HBM on all other pins

Figure 1. Functional Diagram

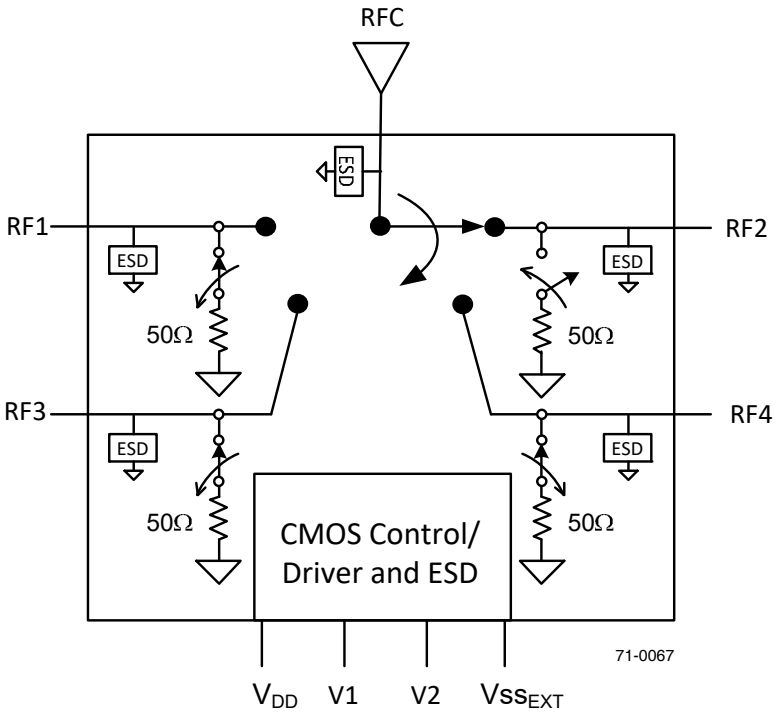


Figure 2. Package Type

32-lead 5 × 5 mm LGA

Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.3V, V_{SS_EXT} = 0V (Z_S = Z_L = 50Ω)

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		10 Hz[1]		8 GHz	
RFC–RFX insertion loss	10 Hz–9 kHz		0.7	1.0	dB
	3000 MHz		0.8	1.1	dB
	6000 MHz		1.0	1.3	dB
	7500 MHz		1.1	1.5	dB
	8000 MHz		1.2	1.6	dB
RFX–RFX isolation	10 Hz–9 kHz	70	80		dB
	3000 MHz	40	45		dB
	6000 MHz	34	39		dB
	7500 MHz	27	32		dB
	8000 MHz	25	31		dB
RFC–RFX isolation	10 Hz–9 kHz	74	84		dB
	3000 MHz	40	45		dB
	6000 MHz	28	33		dB
	7500 MHz	24	29		dB
	8000 MHz	21	27		dB
Return loss (RFC to active port)	10 Hz–9 kHz		24		dB
	3000 MHz		23		dB
	6000 MHz		18		dB
	7500 MHz		14		dB
	8000 MHz		13		dB
Return loss (terminated port)	10 Hz–9 kHz		35		dB
	3000 MHz		18		dB
	6000 MHz		13		dB
	7500 MHz		11		dB
	8000 MHz		10		dB
Settling time	50% CTRL to 0.05 dB final value (–40 to +85 °C) *rising edge*		14	18	µs
	50% CTRL to 0.05 dB final value (–40 to +85 °C) *falling edge*		15	45	µs
Switching time (T_{SW})	50% CTRL to 90% or 10% RF		5	8	µs
P1dB[1] input 1 dB compression point RFX–RFC	All bands @ 1:1 VSWR, 100% duty cycle	31	33		dBm
Input IP3	8000 MHz		58		dBm
Input IP2	8000 MHz		100		dBm

Note 1: Maximum operating P_{IN} (50Ω) is shown in *Table 3.* Please refer to *Figure 4, Figure 5* and Figure *6* when operating the part at low frequency.

Figure 3. Pin Configuration (Top View)

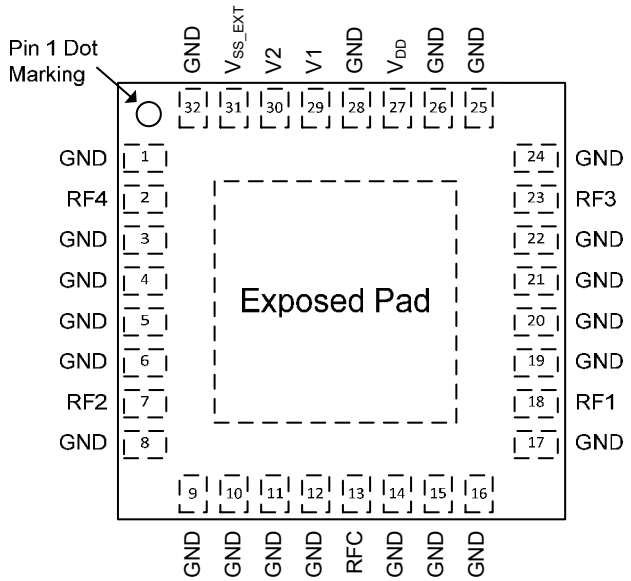


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 3-6, 8, 9-12, 14-17, 19-22, 24-26, 28, 32	GND	Ground
2	RF4[2]	RF I/O
7	RF2[2]	RF I/O
13	RFC[2]	RF common
18	RF1[2]	RF I/O
23	RF3[2]	RF I/O
27	V_{DD}	Supply
29	V1	Switch control input, CMOS logic level
30	V2	Switch control input, CMOS logic level
31	V_{SS_EXT}[1]	External V_{SS} negative voltage control
Paddle	GND	Exposed solder pad: Ground for proper operation

Notes: 1. Use V_{SS_EXT} (pin 31, $V_{SS\_EXT} = -V_{DD}$) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 31) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2. All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	3.0	3.3	3.55	V
Negative power supply voltage[1], V_{SS_EXT}	–3.6	–3.3	–3.0	V
Negative supply current, I_{ss}		–10	–40	µA
Power supply current, I_{DD} V_{DD} = 3.3V, V_{SS_EXT} = 0V, Temp = +85 °C		90	160	µA
Power supply current, I_{DD} V_{DD} = 3.6V, V_{SS_EXT} used			50	µA
Control voltage high (V1, V2)	1.2	1.5	V_{DD}	V
Control voltage low (V1, V2)	0	0	0.4	V
Control current, I_{CTRL}			1	µA
P_{IN} thru path[2] (50Ω, RF power in) 9 kHz – 1 GHz 1 GHz – 8 GHz (85 °C, V_{SS_EXT} = –3.0V) (85 °C, V_{SS_EXT} = 0.0V) (85 °C, V_{SS_EXT} = –3.5V)			*Fig. 4–6* 30 30 28 27.5	dBm
Max power into termination (50Ω) 9 kHz ≤ 6 MHz[2,3] 6 MHz–8 GHz[2,3]			*Fig. 4–6* 20	dBm
Max power, hot switching (50Ω) 9 kHz ≤ 6 MHz[2,3] 6 MHz–8 GHz[2,3]			*Fig. 4–6* 20	dBm
Operating temperature range, T_{OP}	–40		+85	°C

Notes: 1. Applies only when external V_{SS} power supply is used. Otherwise, V_{SS_EXT} = 0.
2. 100% duty cycle (–40 to +85 °C, 1:1 VSWR).
3. Do not exceed 20 dBm.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Maximum junction temperature		+150	°C
Storage temperature range, T_{ST}	–60	+150	°C
Supply voltage, V_{DD}	–0.3	4	V
Control voltage (V1, V2)		4	V
P_{IN} thru path[2] (50Ω, RF power in) 9 kHz – 1 GHz 1 GHz – 8 GHz (85 °C, V_{SS_EXT} = –3.0V) (85 °C, V_{SS_EXT} = 0.0V) (85 °C, V_{SS_EXT} = –3.5V)		 *Fig. 4–6* 30 30 28 27.5	dBm
Max power into termination (50Ω) 9 kHz ≤ 6 MHz[1] 6 MHz–8 GHz		 *Fig. 4–6* 20	dBm
ESD voltage HBM[2] RFC All pins		 2000 1000	 V V
ESD voltage CDM[3], all pins		450	V
ESD voltage MM[4], all pins		100	V

Notes: 1. Do not exceed 20 dBm.
2. Human body model (MIL-STD 883 Method 3015).
3. Charged device model (JEDEC JESD22–C101).
4. Machine model (JEDEC JESD22-A115-A).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42540 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 31 = GND). The rate at which the PE42540 can be switched is only limited to the switching time (*Table 1*) if an external negative

Optional External Vss

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the Vss voltage specified in *Table 3*. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage

Spurious Performance

The typical spurious performance of the PE42540 is –159 dBm/Hz dBm when V_{SS_EXT} = 0V (pin 31 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting $V_{SS\_EXT} = -V_{DD}$.

Table 5. Truth Table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42540 in the 32-lead 5 × 5 mm LGA package is MSL3.

Low Frequency Operation

Table 6 shows the minimum and maximum voltage limits when operating the device under various V_{DD} and V_{SS_EXT} voltage conditions below 9 kHz. Refer to *Figures 4, 5* and *6* to determine the maximum operating power over the frequency

Table 6. Instantaneous RF Voltage Limits for Operation Below 9 kHz

V_{DD}	V_{SS_EXT}	Minimum Peak Voltage at RF Port	Maximum Peak Voltage at RF Port
≥ 3.0	0.0	–0.2	1.2
3.0	–3.0	–0.6	1.6
3.3	–3.3	–0.3	1.3
3.5	–3.5	–0.1	1.1
3.6	–3.6	0.0	1.0

Maximum Operating Power vs Frequency

Figures 4, *5* and *6* show the power limit of the device will increase with frequency. As the frequency increases, the contours and maximum

Thermal Data

Psi-JT (ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51–2).

$\psi_{JT} = (T_J - T_T)/P$

where

ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 7. Thermal Data for PE42540

Parameter	Typ	Unit
ψ_{JT}	79	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	128	°C/W

Figure 4. Maximum Operating Power vs Frequency ($T_{ambient}$ = +25 °C)

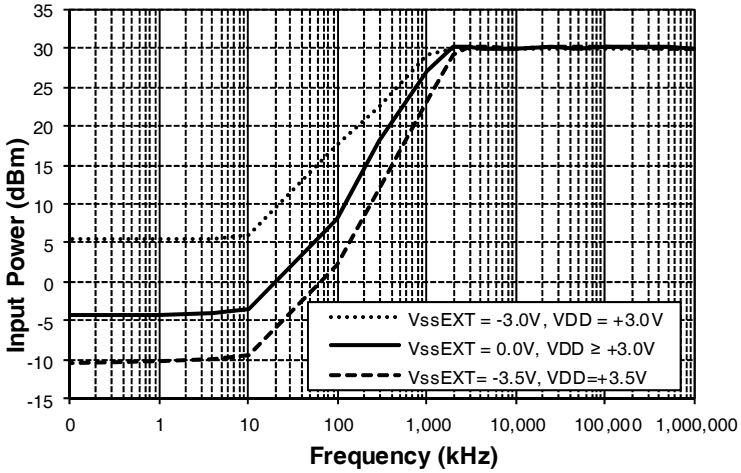


Figure 5. Maximum Operating Power vs Frequency ($T_{ambient}$ = +50 °C)

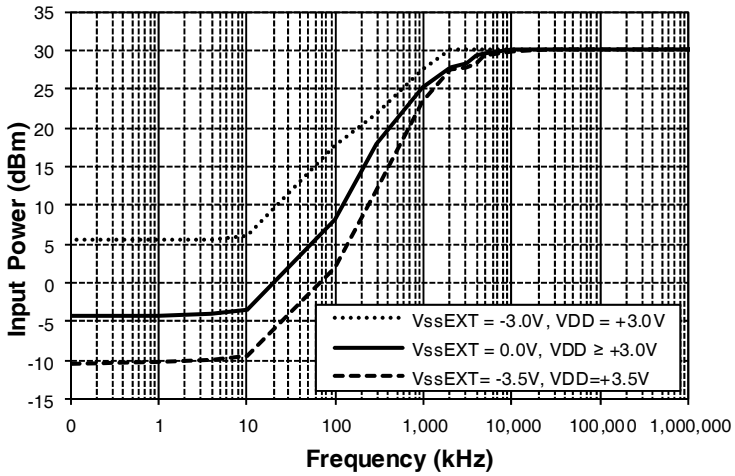


Figure 6. Maximum Operating Power vs Frequency ($T_{ambient}$ = +85 °C)

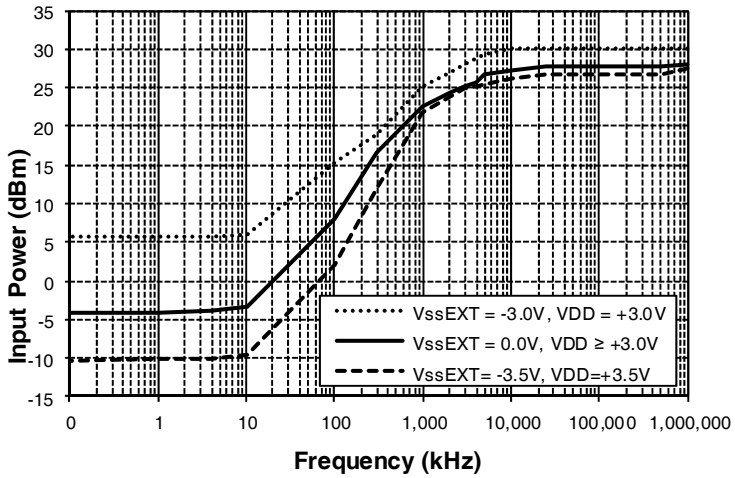


Figure 7. Insertion Loss vs V_{DD} (Temp = +25°C, V_{SS_EXT} = 0)

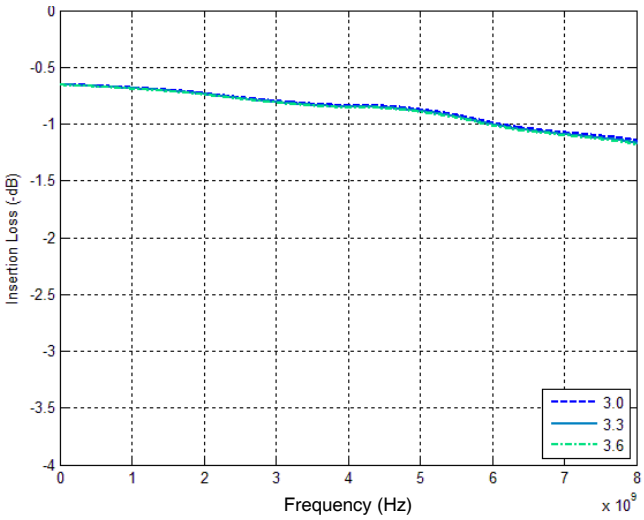


Figure 8. Insertion Loss vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

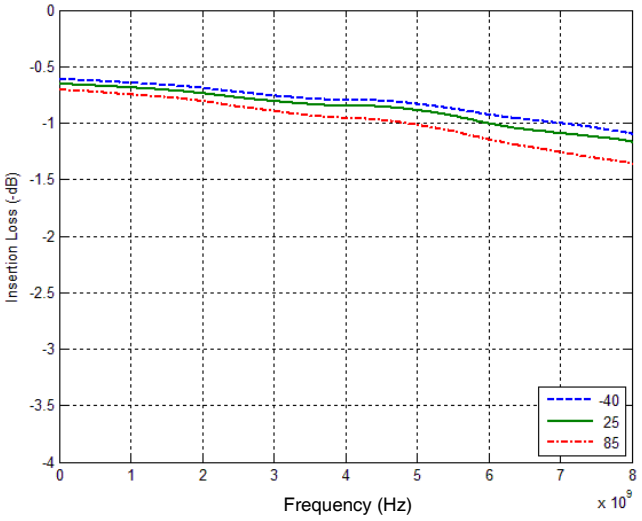


Figure 9. Insertion Loss (Temp = +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0)

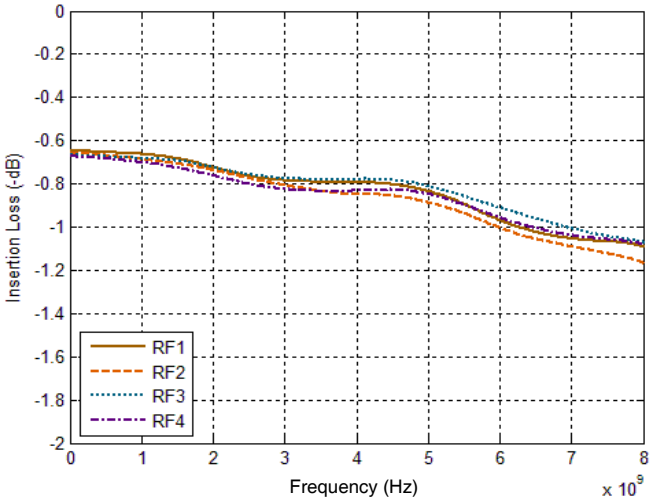


Figure 10. Isolation: RFX–RFX vs V_{DD} (Temp = +25 °C, V_{SS_EXT} = 0)

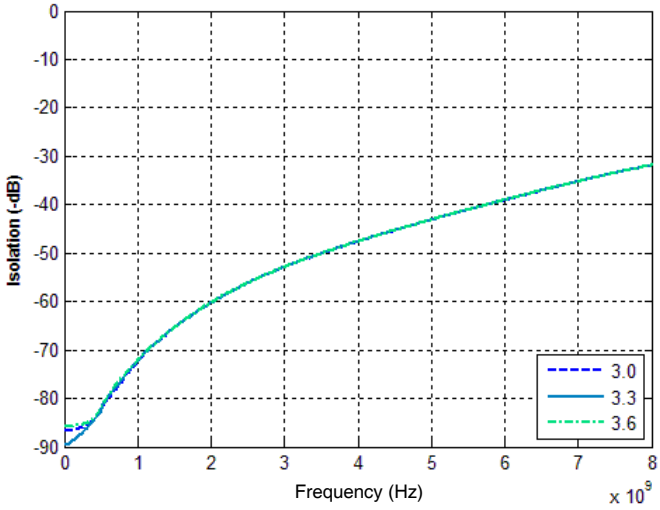


Figure 11. Isolation: RFX–RFX vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

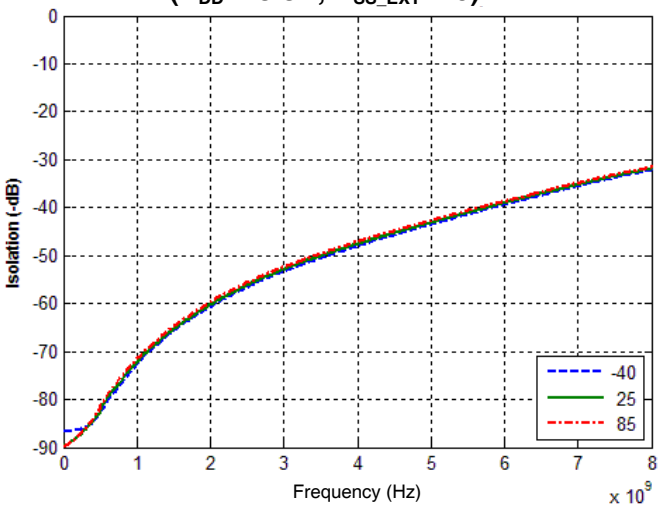


Figure 12. Isolation: RFX–RFC vs V_{DD} (Temp = +25 °C, V_{SS_EXT} = 0)

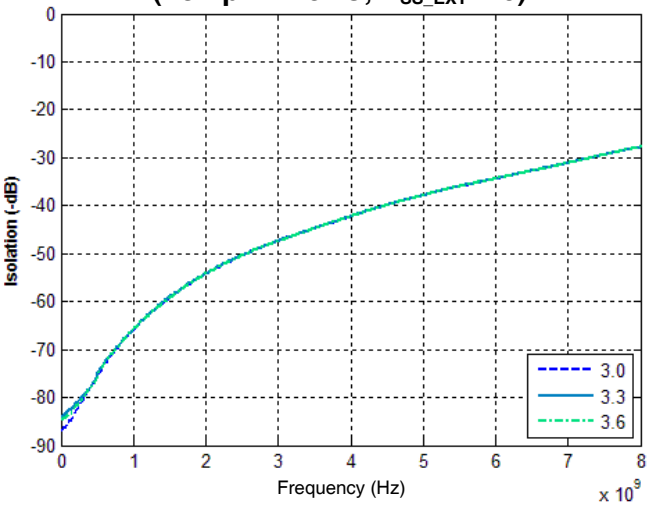


Figure 13. Isolation: RFX–RFC vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

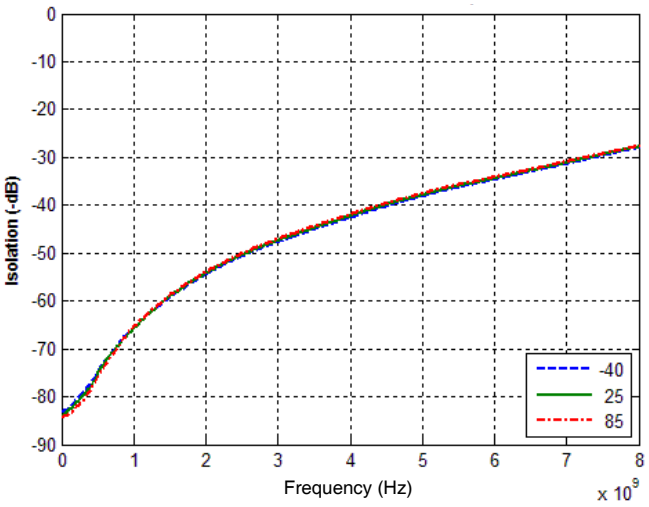


Figure 14. Active Port Return Loss vs V_{DD} (Temp = +25 °C, V_{SS_EXT} = 0)

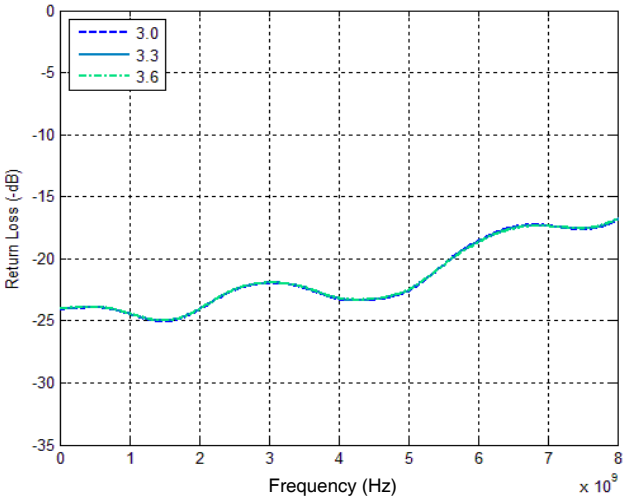


Figure 15. Active Port Return Loss vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

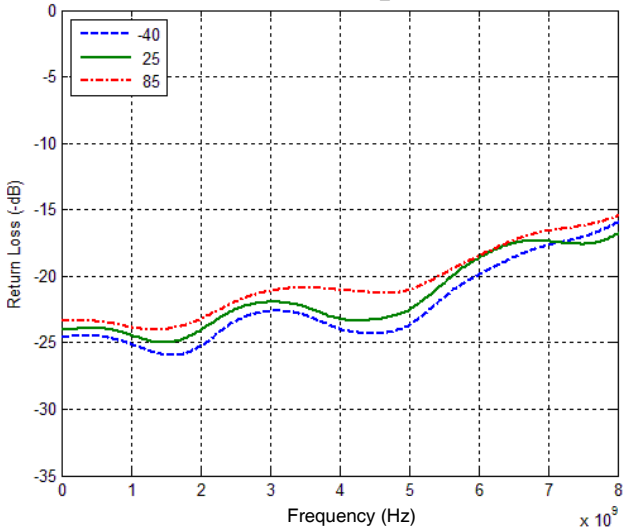


Figure 16. Terminated Port Return Loss vs V_{DD} (Temp = +25 °C, V_{SS_EXT} = 0)

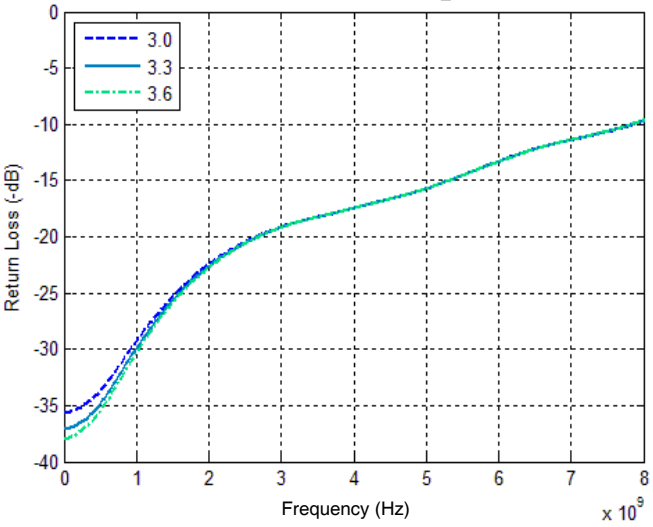


Figure 17. Terminated Port Return Loss vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

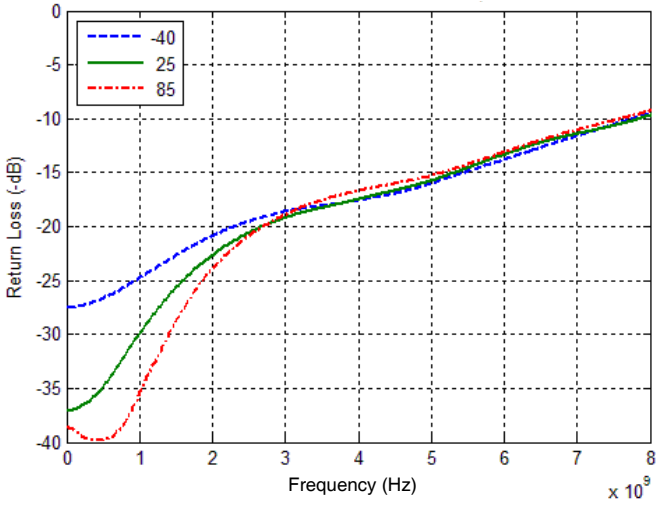


Figure 18. RFC Port Return Loss vs V_{DD} (Temp = +25 °C, V_{SS_EXT} = 0)

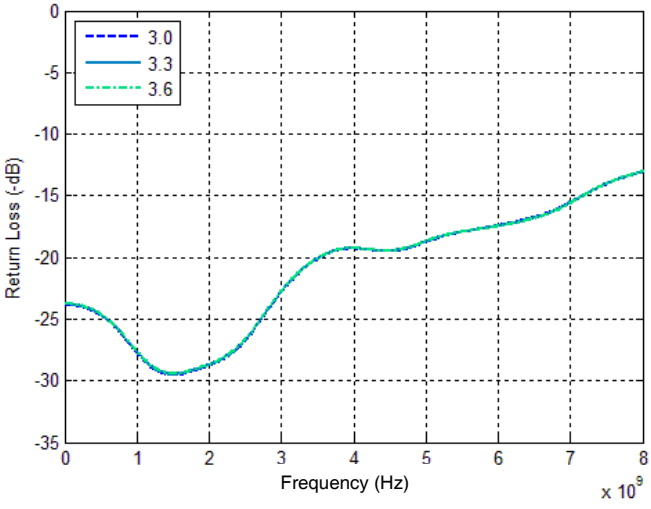


Figure 19. RFC Port Return Loss vs Temp (V_{DD} = 3.3V, V_{SS_EXT} = 0)

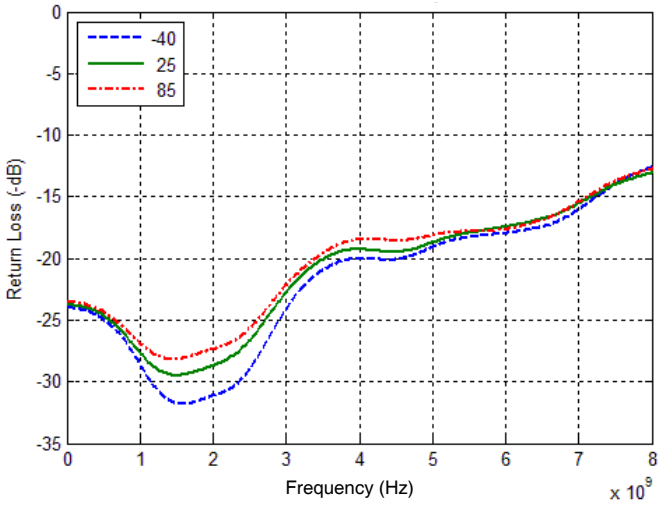
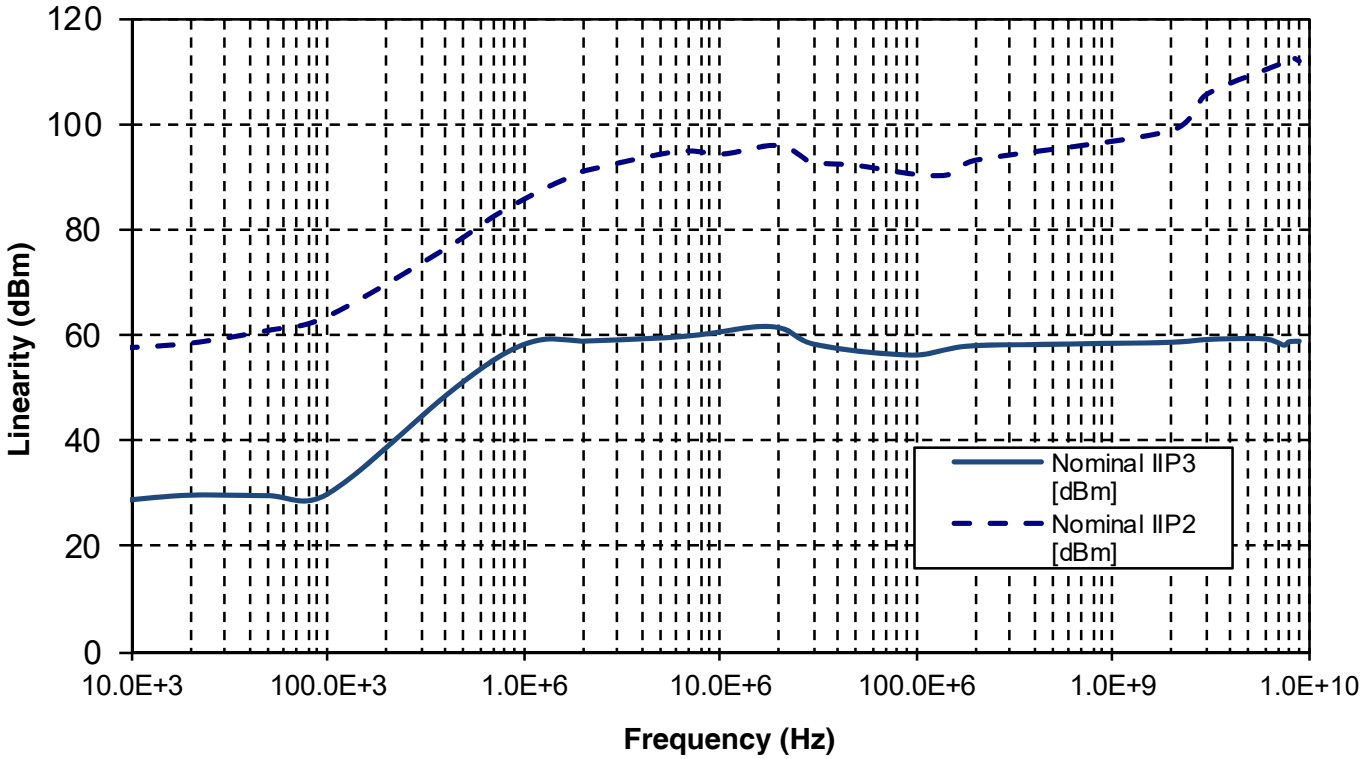


Figure 20. Linearity Performance (Temp = +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0)



Evaluation Kit

The SP4T switch evaluation board was designed to ease customer evaluation of PSemi's PE42540. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via SMA connectors J2, J4, J3 and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

Figure 21. Evaluation Board Layout

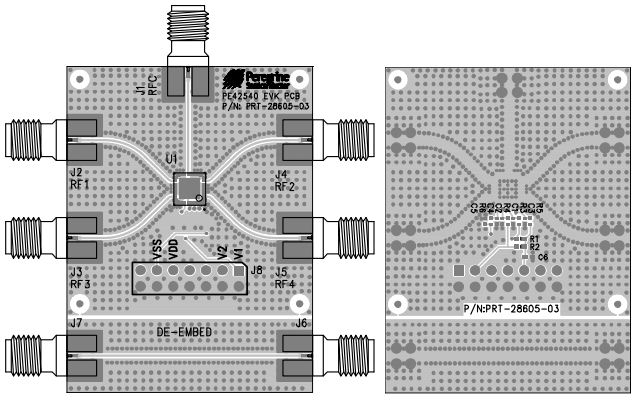


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Figure 22. Evaluation Board Schematic

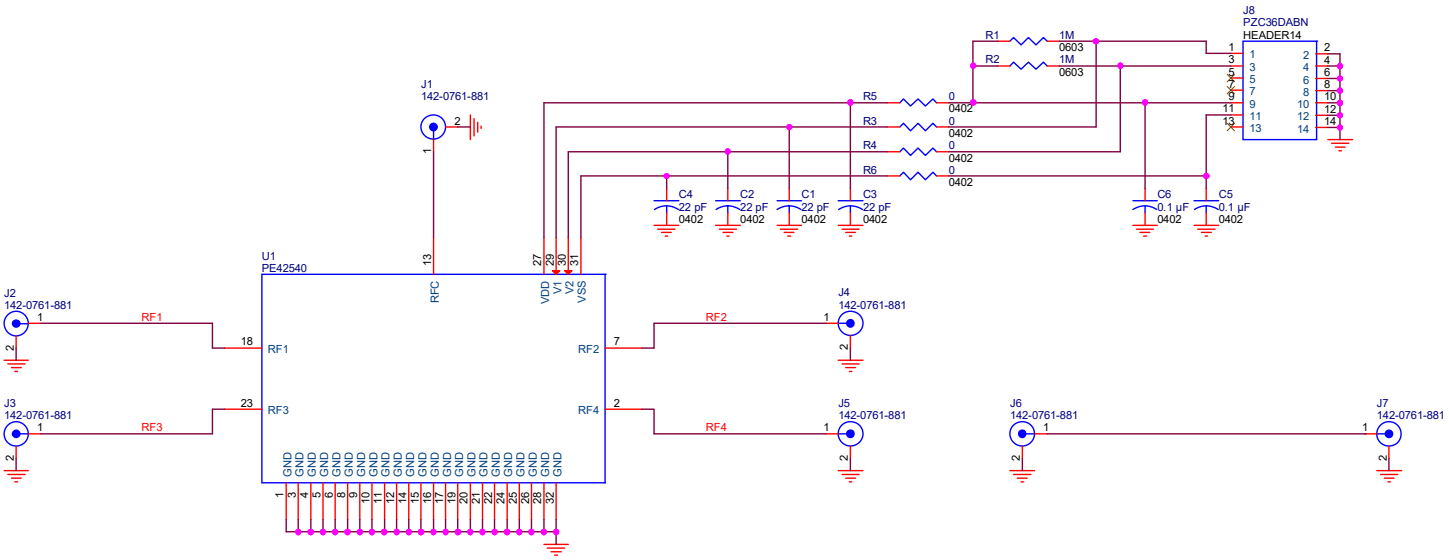

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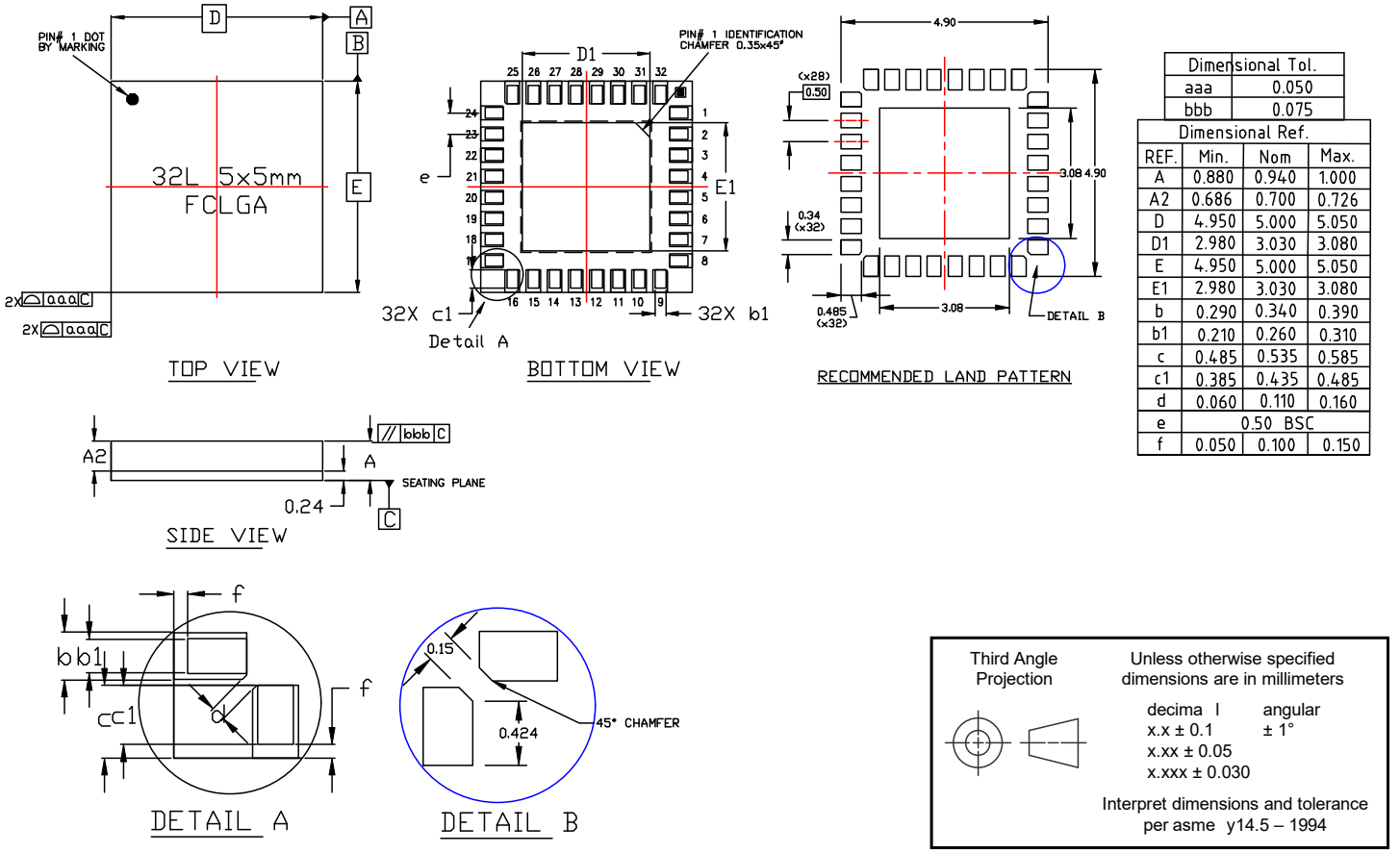
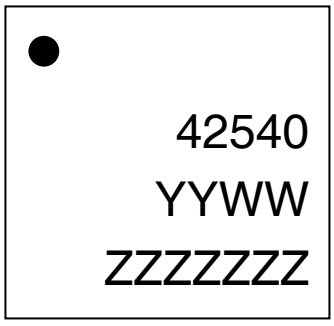
Figure 23. Package Drawing



Dimensional Tol.	
aaa	0.050
bbb	0.075

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.880	0.940	1.000
A2	0.686	0.700	0.726
D	4.950	5.000	5.050
D1	2.980	3.030	3.080
E	4.950	5.000	5.050
E1	2.980	3.030	3.080
b	0.290	0.340	0.390
b1	0.210	0.260	0.310
c	0.485	0.535	0.585
c1	0.385	0.435	0.485
d	0.060	0.110	0.160
e		0.50 BSC	
f	0.050	0.100	0.150

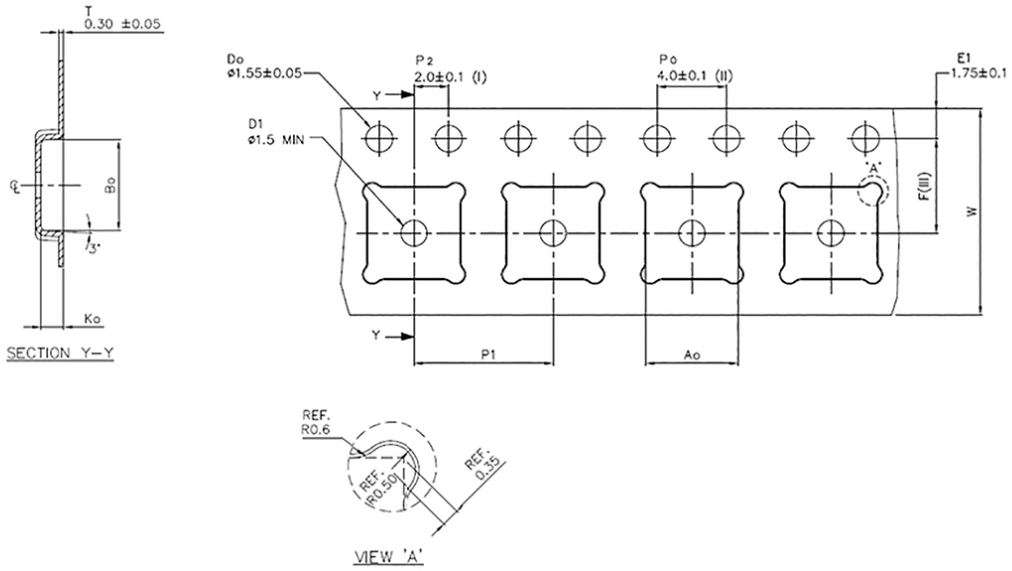
Figure 24. Marking Specifications



YYWW = Date Code

DOC-65743

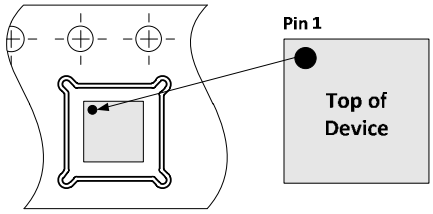
Figure 25. Tape and Reel Drawing



Notes:
(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centerline of sprocket hole to centerline of pocket.

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Ao = 5.30 ± 0.1 mm
Bo = 5.30 ± 0.1 mm
Ko = 1.30 ± 0.1 mm
F = 5.50 ± 0.1 mm
P_1 = 8.00 ± 0.1 mm
W = 12.00 ± 0.3 mm



Device Orientation in Tape

Table 8. Ordering Codes for PE42540

Order Code	Description	Package	Shipping Method
PE42540G-Z	PE42540 SP4T RF switch	Green 32-lead 5 × 5 mm LGA	3000 units/T&R
EK42540-08	PE42540 Evaluation kit	Evaluation kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
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