DS92CK16 3V BLVDS 1 to 6 Clock Buffer/Bus Transceiver

Check for Samples: DS92CK16

FEATURES

- **Master/Slave Clock Selection in a Backplane Application**
- **125 MHz Operation (Typical)**
- **100 ps Duty Cycle Distortion (Typical)**
- **50 ps Channel to Channel Skew (Typical)**
- **3.3V Power Supply Design**
- **Glitch-free Power on at CLKI/O Pins**
- **Low Power Design (20 mA @ 3.3V Static)**
- **Accepts Small Swing (300 mV Typical) Differential Signal Levels**
- **Industrial Temperature Operating Range (-40°C to +85°C)**
- **Available in 24-pin TSSOP Packaging**

DESCRIPTION

The DS92CK16 1 to 6 Clock Buffer/Bus Transceiver is a one to six CMOS differential clock distribution device utilizing Bus Low Voltage Differential Signaling (BLVDS) technology. This clock distribution device is designed for applications requiring ultra low power dissipation, low noise, and high data rates. The BLVDS side is a transceiver with a separate channel acting as a return/source clock.

The DS92CK16 accepts LVDS (300 mV typical) differential input levels, and translates them to 3V CMOS output levels. An output enable pin $\overline{OE}$, when high, forces all CLK_{OUT} pins high.

The device can be used as a source synchronous driver. The selection of the source driving is controlled by the $CrdCLK_{IN}$ and $\overline{DE}$ pins. This device can be the master clock, driving the inputs of other clock I/O pins in a multipoint environment. Easy master/slave clock selection is achieved along a backplane.

Function Diagram and Truth Table

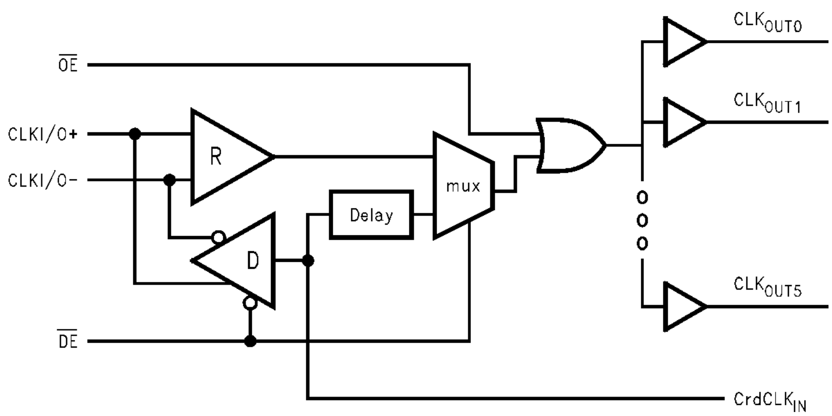


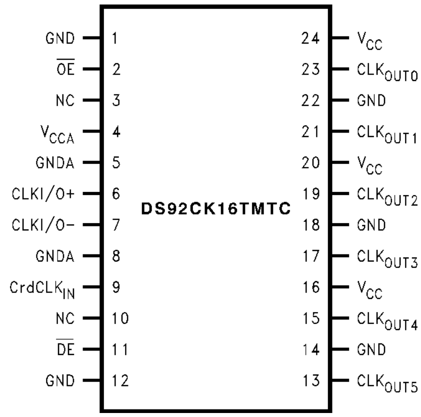
Table 1. Receive Mode Truth Table

INPUT				OUTPUT
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	(CLKI/O+)–(CLKI/O−)	CLK_{OUT}
H	H	X	X	H
L	H	X	VID≥ 0.07V	H
L	H	X	VID≤ −0.07V	L

Table 2. Driver Mode Truth Table

INPUT			OUTPUT		
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	CLK/I/O+	CLKI/O−	CLK_{OUT}
L	L	L	L	H	L
L	L	H	H	L	H
H	L	L	L	H	H
H	L	H	H	L	H
H	H	X	Z	Z	H

Connection Diagram



TSSOP Package
See Package Number PW (R-PDSO-G24)

TSSOP PACKAGE PIN DESCRIPTIONS

Pin Name	Pin #	Type	Description
CLKI/O+	6	I/O	True (Positive) side of the differential clock input.
CLKI/O−	7	I/O	Complementary (Negative) side of the differential clock input.
OE	2	I	$\overline{OE}$; this pin is active Low. When High, this pin forces all CLK_{OUT} pins High. When Low, CLK_{OUT} pins logic state is determined by either the $CrdCLK_{IN}$ or the VID at the CLK/I/O pins with respect to the logic level at the $\overline{DE}$ pin. This pin has a weak pullup device to V_{CC}. If $\overline{OE}$ is floating, then all CLK_{OUT} pins will be High.
DE	11	I	$\overline{DE}$; this pin is active LOW. When Low, this pin enables the $CardCLK_{IN}$ signal to the CLKI/O pins and CLK_{OUT} pins. When High, the Driver is TRI-STATE, the CLKI/O pins are inputs and determine the state of the CLK_{OUT} pins. This pin has a weak pullup device to V_{CC}. If $\overline{DE}$ is floating, then CLKI/O pins are TRI-STATE.
CLK_{OUT}	13, 15, 17, 19, 21, 23	O	6 Buffered clock (CMOS) outputs.
$CrdCLK_{IN}$	9	I	Input clock from Card (CMOS level or TTL level).
V_{CC}	16, 20, 24	Power	V_{CC}; Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GND	1, 12, 14, 18, 22	Ground	GND
V_{CCA}	4	Power	Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GNDA	5, 8	Ground	Analog Ground (Internally separate from Ground must be connected externally).
NC	3, 10		No Connects

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

Supply Voltage (V_{CC})	−0.3V to +4V
Enable Input Voltage ($\overline{DE}$, $\overline{OE}$, $CrdCLK_{IN}$)	−0.3V to +4V
Voltage (CLK_{OUT})	−0.3V to (V_{CC} + 0.3V)
Voltage (CLKI/O±)	−0.3V to +4V
Driver Short Circuit Current	momentary
Receiver Short Circuit Current	momentary
Maximum Package Power Dissipation at +25°C	
PW Package	1500 mW
Derate PW Package	8.2 mW/°C above +25°C
θ_{JA}	95°C/W
θ_{JC}	30°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
(Soldering, 4 sec.)	260°C
ESD Ratings: HBM [3]	>3000V
CDM [3]	>1000V
Machine Model [3]	>200V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be verified. These ratings are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) ESD Rating: ESD qualification is performed per the following: HBM (1.5 kΩ, 100 pF), Machine Model (250V, 0Ω), IEC 1000-4-2. All VCC pins connected together, all ground pins connected together.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
$CrdCLK_{IN}$, $\overline{DE}$, $\overline{OE}$ Input Voltage	0		V_{CC}	V
Operating Free Air Temperature (T_A)	−40	25	+85	°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified [1] [2].

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{TH}	Input Threshold High		CLKI/O+, CLKI/O−		25	+70	mV
V_{TL}	Input Threshold Low			−70	-35		mV
VCMR	Common Mode Voltage Range [3]	VID = 250 mV pk to pk		|VID|/2		2.4 - |VID|/2	V
I_{IN}	Input Current	V_{IN} = 0V to V_{CC}, $\overline{DE}$ = V_{CC}, $\overline{OE}$ = V_{CC}, Other Input = 1.2V ± 50 mV		−20	±5	+20	µA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except VID, VOD, VTH, and VTL.
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) The VCMR range is reduced for larger VID. Example: If VID=400 mV, then VCMR is 0.2V to 2.2V A VID up to |V_{CC}–0V| may be applied between the CLKI/O+ and CLKI/O− inputs, with the Common Mode set to V_{CC}/2.

DC Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1) (2).

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OH1R}	Output High Voltage	VID = 250 mV, I_{OH} = −1.0 mA	CLK_{OUT}	V_{CC}−0.4	2.9		V
V_{OH2R}	Output High Voltage	VID = 250 mV, I_{OH} = −6 mA		V_{CC}−0.8	2.5		V
V_{OL1R}	Output Low Voltage	I_{OL} = 1.0 mA, VID = −250 mV			0.06	0.3	V
V_{OL2R}	Output Low Voltage	I_{OL} = 6 mA, VID = −250 mV		0		0.4	V
I_{ODHR}	CLK_{OUT} Dynamic Output Current (4)	VID = +250 mV, V_{OUT} = V_{CC}−1V		−8	-16	-30	mA
I_{ODLR}	CLK_{OUT} Dynamic Output Current (4)	VID = −250 mV, V_{OUT} = 1V		10	21	35	mA
V_{IH}	Input High Voltage		$\overline{DE}$, $\overline{OE}$, $CrdCLK_{IN}$	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V	$\overline{OE}$, $\overline{DE}$	−10	−2	+10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V		−20	−5	+20	µA
I_{INCRD}	Input Current	V_{IN} = 0V to V_{CC}, $\overline{OE}$ = V_{CC}	$CrdCLK_{IN}$	−5		+5	µA
V_{CL}	Input Voltage Clamp	I_{OUT} = −1.5 mA	$\overline{OE}$, $\overline{DE}$, $CrdCLK_{IN}$	−0.8			V
I_{CC}	No Load Supply Current Outputs Enabled, No VID Applied	$\overline{OE}$ = $\overline{DE}$ = 0V, $CrdCLK_{IN}$ = V_{CC} or GND, CLKI/O (±) = Open CLK_{OUT} (0:5) = Open Circuit	V_{CC}			13	mA
I_{CC1}	No Load Supply Current Outputs Enabled, VID over Common Mode Voltage Range	$\overline{OE}$ = GND $\overline{DE}$ = V_{CC} $CrdCLK_{IN}$ = V_{CC} or GND, VID = 250 mV (0.125V VCM 2.275V), CLK_{OUT} (0:5) = Open Circuit				10	mA
I_{CCD}	Driver Loaded Supply Current	$\overline{DE}$ = $\overline{OE}$ = 0V, $CrdCLK_{IN}$ = V_{CC} or GND, R_L = 37.5Ω between CLKI/O+ and CLKI/O−, CLK_{OUT} (0:5) = Open Circuit			20	25	mA
V_{OD}	Driver Output Differential Voltage	R_L = 37.5Ω, Figure 5 $\overline{DE}$ = 0V	CLKI/O+, CLKI/O−	250	350	450	mV
ΔV_{OD}	Driver V_{OD} Magnitude Change				10	20	mV
V_{OS}	Driver Offset Voltage			1.1	1.29	1.5	V
ΔV_{OS}	Driver Offset Voltage Magnitude Change				5	20	mV
V_{OHD}	Driver Output High				1.35	1.8	V
V_{OLD}	Driver Output Low			0.80	1.05		V
I_{OS1D}	Driver Differential Short Circuit Current (5)	$CrdCLK_{IN}$ = V_{CC} or GND, VOD = 0V, (outputs shorted together) $\overline{DE}$ = 0V			|30|	|50|	mA
I_{OS2D}	Driver Output Short Circuit Current to V_{CC} (5)	$CrdCLK_{IN}$ = GND, $\overline{DE}$ = 0V, CLKI/O+ = V_{CC}			36	70	mA
I_{OS3D}	Driver Output Short Circuit Current to V_{CC} (5)	$CrdCLK_{IN}$ = V_{CC}, $\overline{DE}$ = 0V, CLKI/O− = V_{CC}			34	70	mA
I_{OS4D}	Driver Output Short Circuit Current to GND (5)	$CrdCLK_{IN}$ = V_{CC}, $\overline{DE}$ = 0V, CLKI/O+ = 0V			−47	−70	mA
I_{OS5D}	Driver Output Short Circuit Current to GND (5)	$CrdCLK_{IN}$ = GND, $\overline{DE}$ = 0V, CLKI/O− = 0V			−50	−70	mA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or Open, $V_{APPLIED}$ = 3.6V				±20	µA

(4) Only one output should be momentarily shorted at a time. Do not exceed package power dissipation rating.
(5) Only one output should be momentarily shorted at a time. Do not exceed package power dissipation rating.

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified [1] [2].

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL RECEIVER CHARACTERISTICS						
t_{PHLDR}	Differential Propagation Delay High to Low. CLKI/O to CLK_{OUT}	C_L = 15 pF VID = 250 mV Figure 1 Figure 2	1.3	2.8	3.8	ns
t_{PLHDR}	Differential Propagation Delay Low to High. CLKI/O to CLK_{OUT}		1.3	2.9	3.8	ns
t_{SK1R}	Duty Cycle Distortion [3] (pulse skew) $\|t_{PLH}–t_{PHL}\|$			100	400	ps
t_{SK2R}	Channel to Channel Skew; Same Edge [4]			30	80	ps
t_{SK3R}	Part to Part Skew [5]				2.5	ns
t_{TLHR}	Transition Time Low to High [6] (20% to 80%)		0.4	1.4	2.4	ns
t_{THLR}	Transition Time High to Low [6] (80% to 20%)		0.4	1.3	2.2	ns
t_{PLHOER}	Propagation Delay Low to High ($\overline{OE}$to CLK_{OUT})	C_L = 15 pF Figure 3 Figure 4	1.0	3	4.5	ns
t_{PHLOER}	Propagation Delay High to Low ($\overline{OE}$ to CLK_{OUT})		1.0	3	4.5	ns
f_{MAX}	Maximum Operating Frequency [7]		100	125		MHz
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLDD}	Differential Propagation Delay High to Low. $CrdCLK_{IN}$ to CLKI/O	C_L = 15 pF R_L = 37.5Ω Figure 6 Figure 7	0.5	1.8	2.5	ns
t_{PLHDD}	Differential Propagation Delay Low to High. $CrdCLK_{IN}$ to CLKI/O		0.5	1.8	2.5	ns
t_{PHLCrd}	$CrdCLK_{IN}$ to CLK_{OUT} Propagation Delay High to Low	C_L = 15 pF Figure 8 Figure 9	2.0	4.5	6.0	ns
t_{PLHCrd}	$CrdCLK_{IN}$ to CLK_{OUT} Propagation Delay Low to High		2.0	4.5	6.0	ns
t_{SK1D}	Duty Cycle Distortion (pulse skew) $\|t_{PLH}–t_{PHL}\|$ [8]				600	ps
t_{SK2D}	Differential Part-to-Part Skew [9]				2.0	ns
t_{TLHD}	Differential Transition Time [6] (20% to 80%)		0.4	0.75	1.4	ns
t_{THLD}	Differential Transition Time [6] (80% to 20%)		0.4	0.75	1.4	ns
t_{PHZD}	Transition Time High to TRI-STATE. $\overline{DE}$ to CLKI/O				10	ns
t_{PLZD}	Transition Time Low to TRI-STATE. $\overline{DE}$ to CLKI/O	V_{IN} = 0V to V_{CC} C_L = 15 pF, R_L = 37.5Ω Figure 10 Figure 11			10	ns
t_{PZHD}	Transition Time TRI-STATE to High. $\overline{DE}$ to CLKI/O				32	ns
t_{PZLD}	Transition Time TRI-STATE to Low. $\overline{DE}$ to CLKI/O				32	ns
f_{MAX}	Maximum Operating Frequency [7]		100	125		MHz

(1) C_L includes probe and fixture capacitance.
(2) Generator waveform for all tests unless otherwise specified: f = 25 MHz, Zo = 50Ω, t_r = 1 ns, t_f = 1 ns (10%–90%). To ensure fastest propagation delay and minimum skew, clock input edge rates should not be slower than 1 ns/V; control signals not slower than 3 ns/V. In general, the faster the input edge rate, the better the AC performance.
(3) t_{SK1R} is the difference in receiver propagation delay ($|t_{PLH}–t_{PHL}|$) of one device, and is the duty cycle distortion of the output at any given temperature and V_{CC}. The propagation delay specification is a device to device worst case over process, voltage and temperature.
(4) t_{SK2R} is the difference in receiver propagation delay between channels in the same device of any outputs switching in the same direction. This parameter is specified by design and characterization.
(5) $t_{SK3R,}$ part-to-part skew, is the difference in receiver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. T_{SK3R} is defined as Max–Min differential propagation delay.This parameter is specified by design and characterization.
(6) All device output transition times are based on characterization measurements and are specified by design.
(7) Generator input conditions: t_r/t_f < 1 ns, 50% duty cycle, differential (1.10V to 1.35V pk-pk). Output Criteria: 60%/40% duty cycle, V_{OL}(max) 0.4V, V_{OH}(min) 2.7V, Load = 7 pF (stray plus probes).
(8) t_{SK1D} is the difference in driver propagation delay ($|t_{PLH}–t_{PHL}|$) and is the duty cycle distortion of the CLKI/O outputs.
(9) t_{SK2D} part-to-part skew, is the difference in driver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SK2D} is defined as Max–Min differential propagation delay.

PARAMETER MEASUREMENT INFORMATION

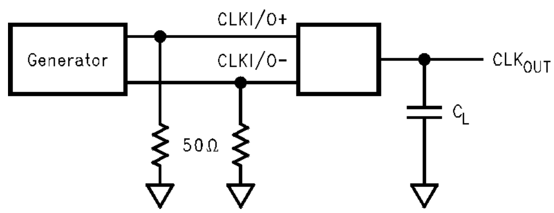
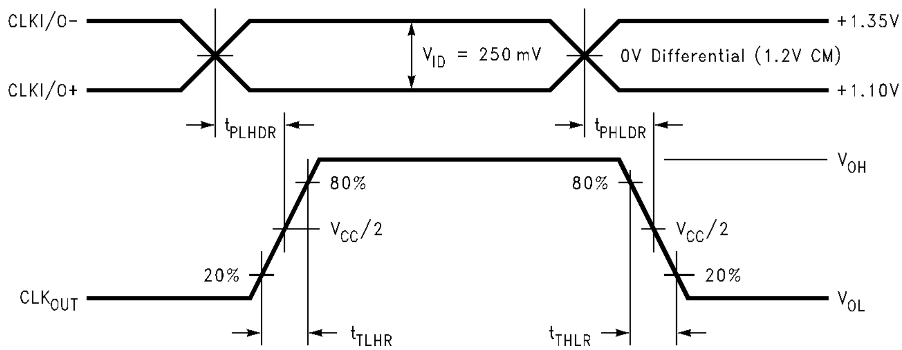


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit



Generator waveform for all test unless otherwise specified: f = 25 MHz, 50% Duty Cycle, Zo = 50Ω, t_{TLH} = 1 ns, t_{THL} = 1 ns.

Figure 2. Receiver Propagation Delay and Transition Time Waveforms

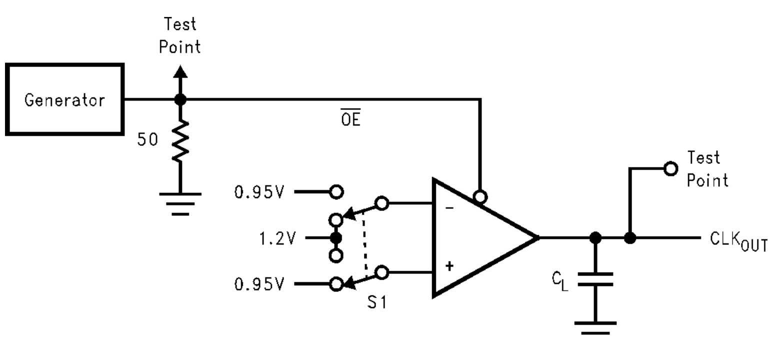


Figure 3. Output Enable ($\overline{OE}$) Delay Test Circuit

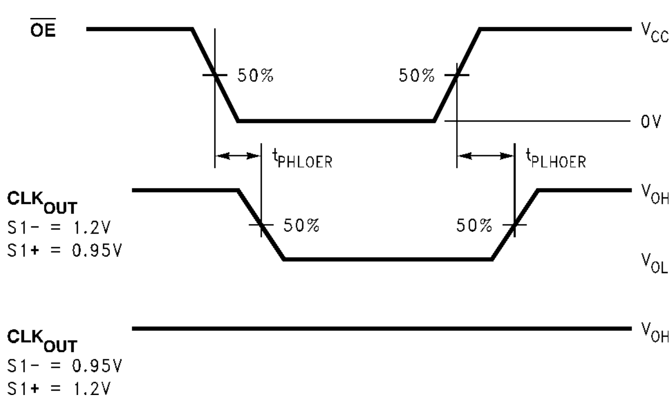


Figure 4. Output Enable ($\overline{OE}$) Delay Waveforms

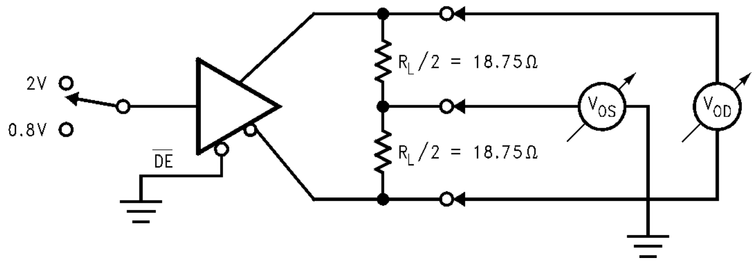


Figure 5. Differential Driver DC Test

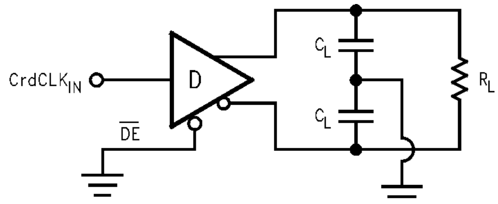


Figure 6. Driver Propagation Delay Test Circuit

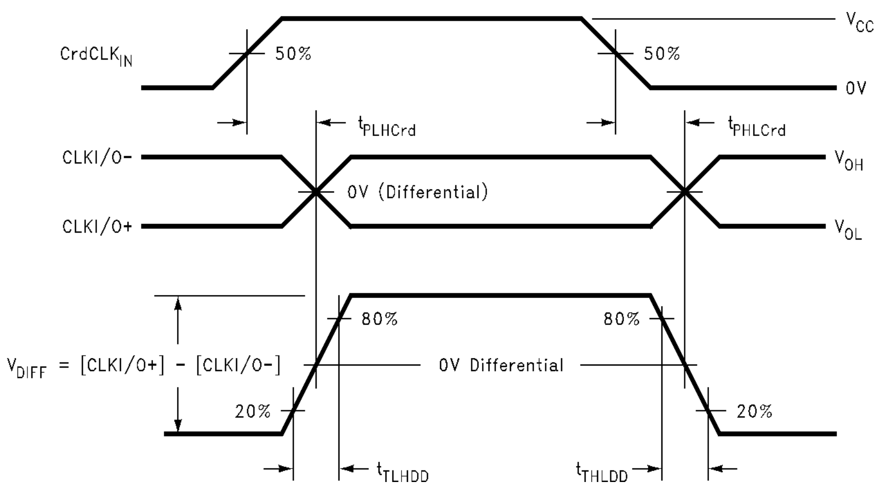


Figure 7. Driver Propagation Delay and Transition Time Waveforms

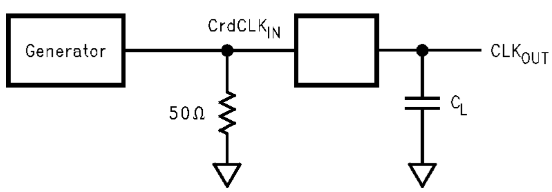


Figure 8. $CrdCLK_{IN}$ Propagation Delay Time Test Circuit

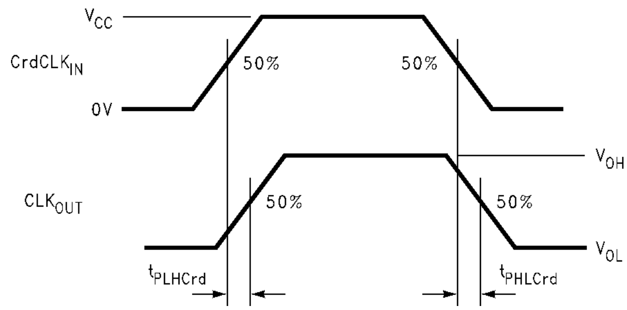


Figure 9. CrdCLK$_{IN}$ Propagation Delay Time Waveforms

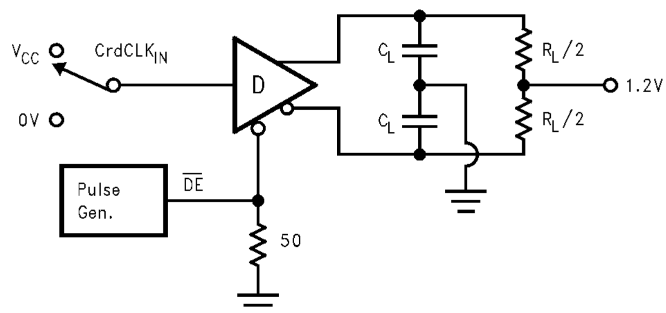


Figure 10. Driver TRI-STATE Test Circuit

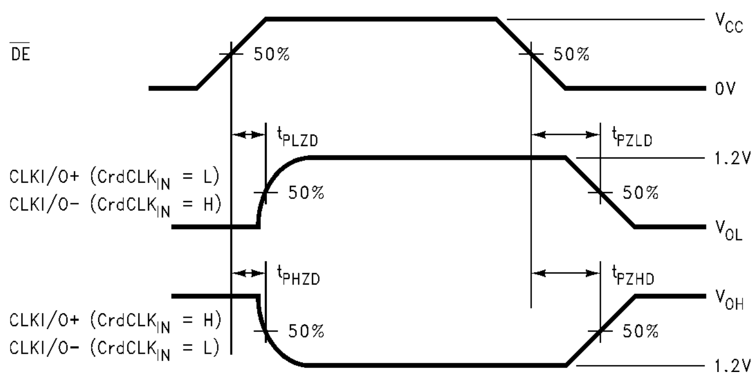


Figure 11. Driver TRI-STATE Waveforms

APPLICATIONS INFORMATION

General application guidelines and hints for BLVDS/LVDS transceivers, drivers and receivers may be found in the following application notes: LVDS Owner's Manual, AN805(SNOA233), AN807(SNLA027), AN808(SNLA028), AN903(SNLA034), AN905(SNLA035), AN916(SNLA219), AN971(SNLA165), AN977(SNLA166) .

BLVDS drivers and receivers are intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Zo) is in the range of 50Ω to100Ω. Two termination resistors of ZoΩ each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS92CK16 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance (100 ohms) and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 9.330 mA. The current changes as a function of load resistor. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop. Unterminated configurations are not allowed. The 9.33 mA loop current will develop a differential voltage of about 350mV across 37.5Ω (double terminated 75Ω differential transmission backplane) effective resistance, which the receiver detects with a 280 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 70 mV = 280 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 4.7µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC BOARD CONSIDERATIONS

Use at least 4 PCB layers (top to bottom); BLVDS signals, ground, power, TTL signals.

Isolate TTL signals from BLVDS signals, otherwise the TTL may couple onto the BLVDS lines. It is best to put TTL and BLVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (BLVDS port side) connectors as possible to create short stub lengths.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. backplane or cable) and termination resistor(s). Run the differential pair trace lines as close together as possible as soon as they leave the IC . This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

STUB LENGTH

Stub lengths should be kept to a minimum. The typical transition time of the DS92CK16 BLVDS output is 0.75ns (20% to 80%). The 100 percent time is 0.75/0.6 or 1.25ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 1.25ns/5 is 250 picoseconds. Let velocity equal 160ps per inch for a typical loaded backplane. Then maximum stub length is 250ps/160ps/in or 1.56 inches. To determine the maximum stub for your backplane, you need to know the propagation velocity for the actual conditions (refer to application notes AN– 905(SNLA035) and AN–808(SNLA028)).

TERMINATION

Use a resistor which best matches the differential impedance of your loaded transmission line. Remember that the current mode outputs need the termination resistor to generate the differential voltage. BLVDS will not work without resistor termination.

Surface mount 1% to 2% resistors are best.

PROBING BLVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

Use controlled impedance media. The connectors you use should have a matched differential impedance of about Zo Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92CK16TMTC	ACTIVE	TSSOP	PW	24	61	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	DS92CK16T MTC	Samples
DS92CK16TMTC/NOPB	ACTIVE	TSSOP	PW	24	61	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS92CK16T MTC	Samples
DS92CK16TMTCX/NOPB	ACTIVE	TSSOP	PW	24	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS92CK16T MTC	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

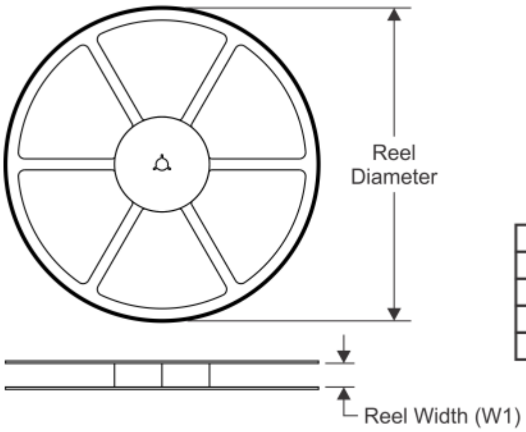
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

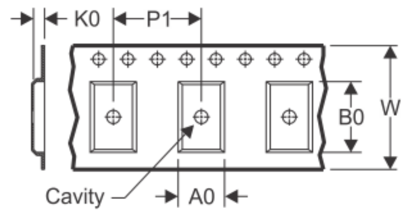
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

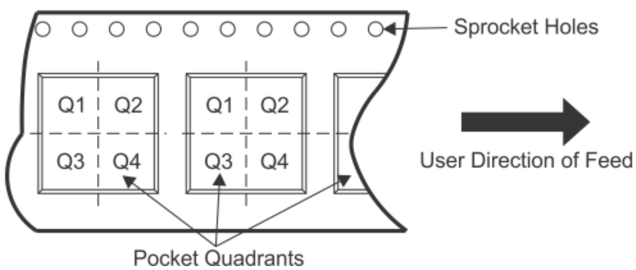


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

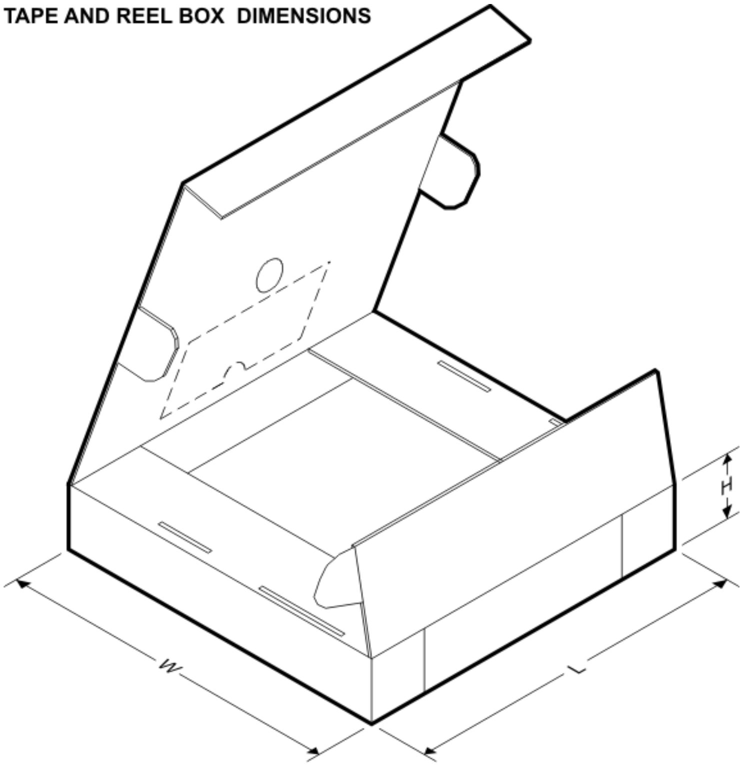
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92CK16TMTCX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

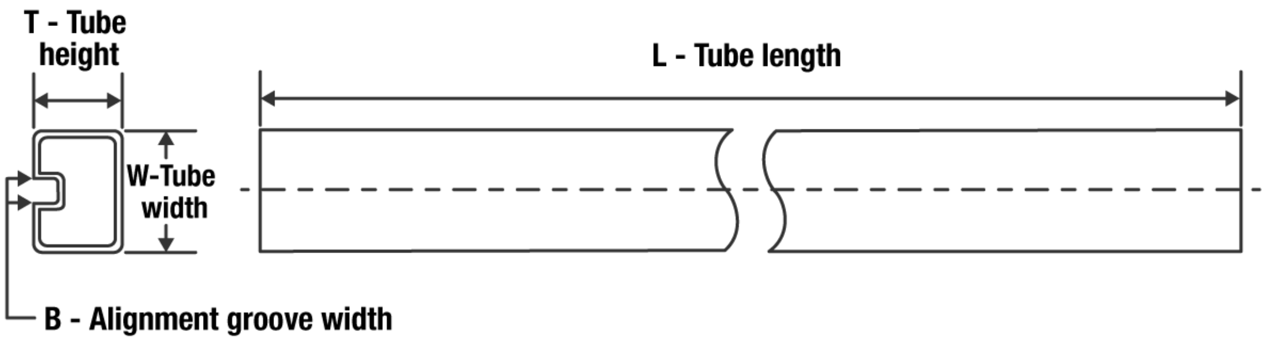
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92CK16TMTCX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

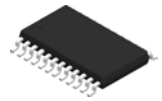
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS92CK16TMTC	PW	TSSOP	24	61	495	8	2514.6	4.06
DS92CK16TMTC	PW	TSSOP	24	61	495	8	2514.6	4.06
DS92CK16TMTC/NOPB	PW	TSSOP	24	61	495	8	2514.6	4.06

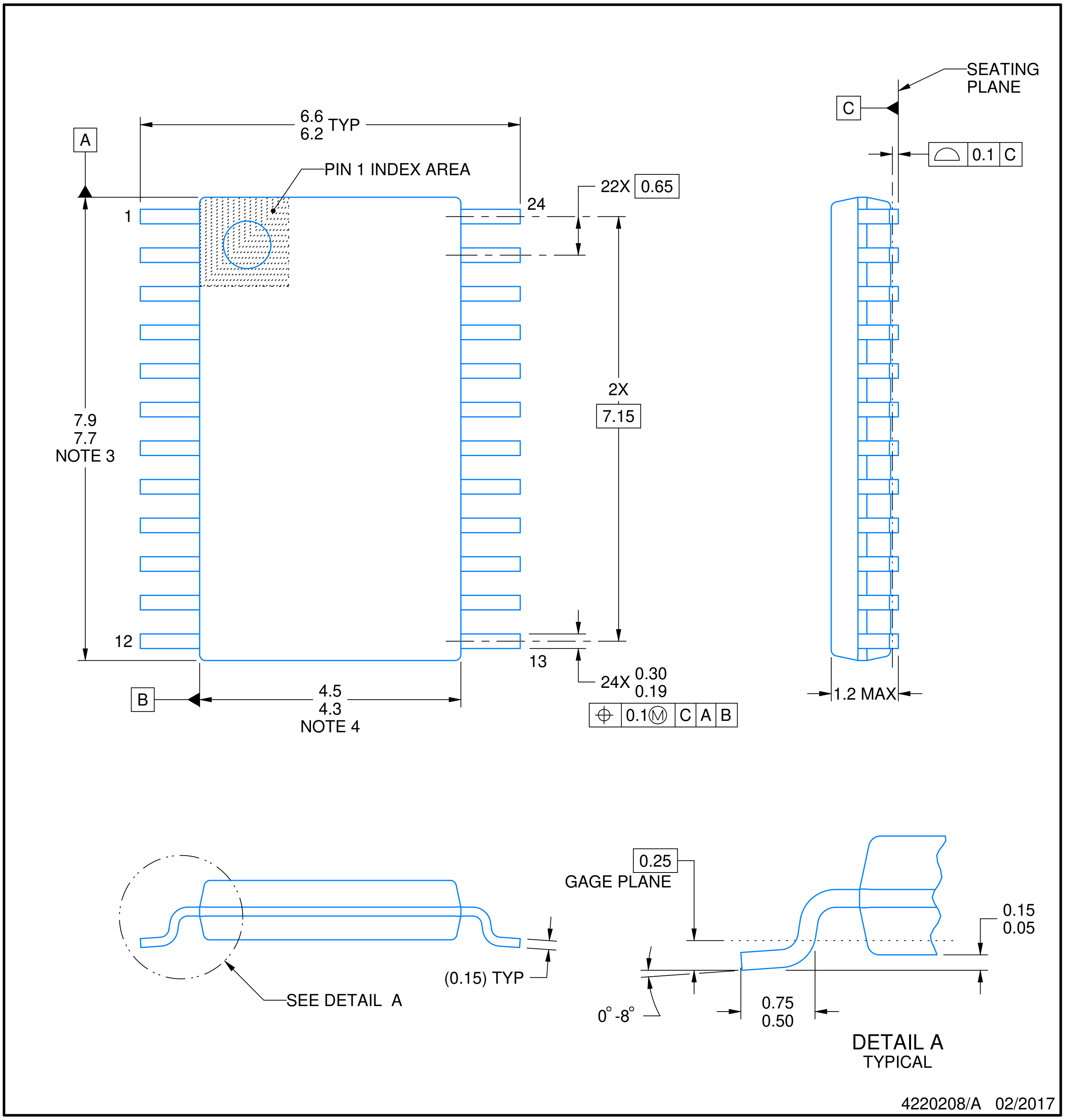
PACKAGE OUTLINE



PW0024A

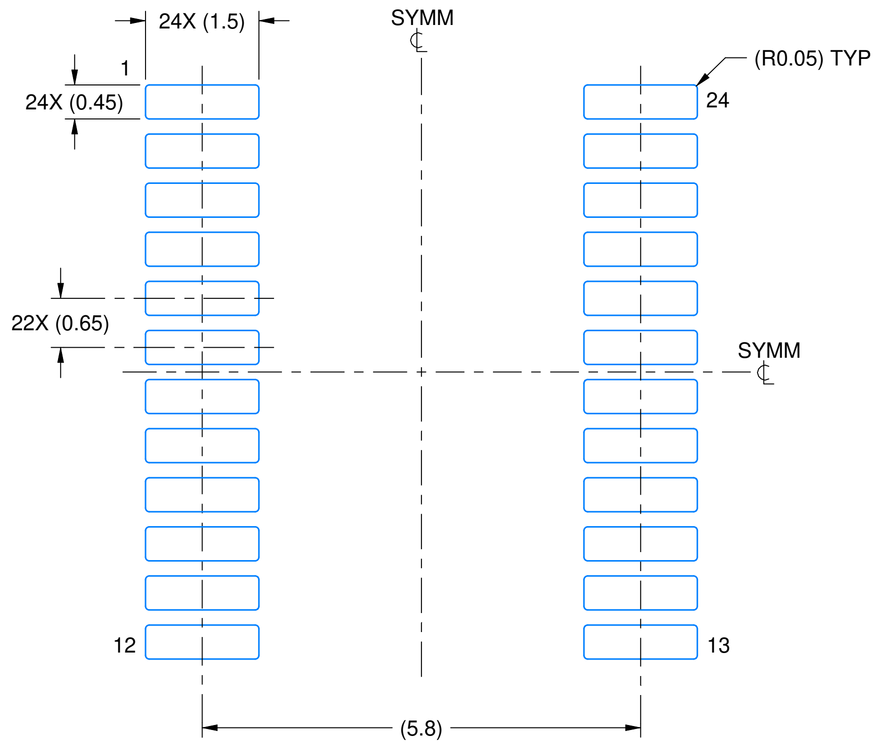
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

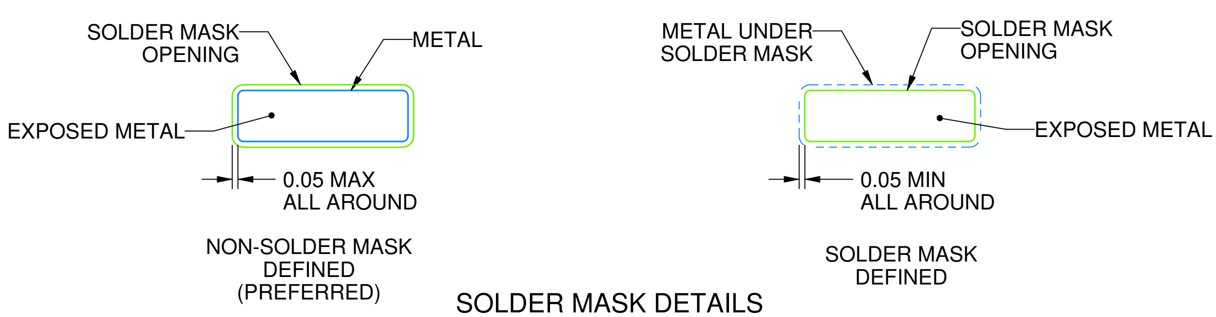


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

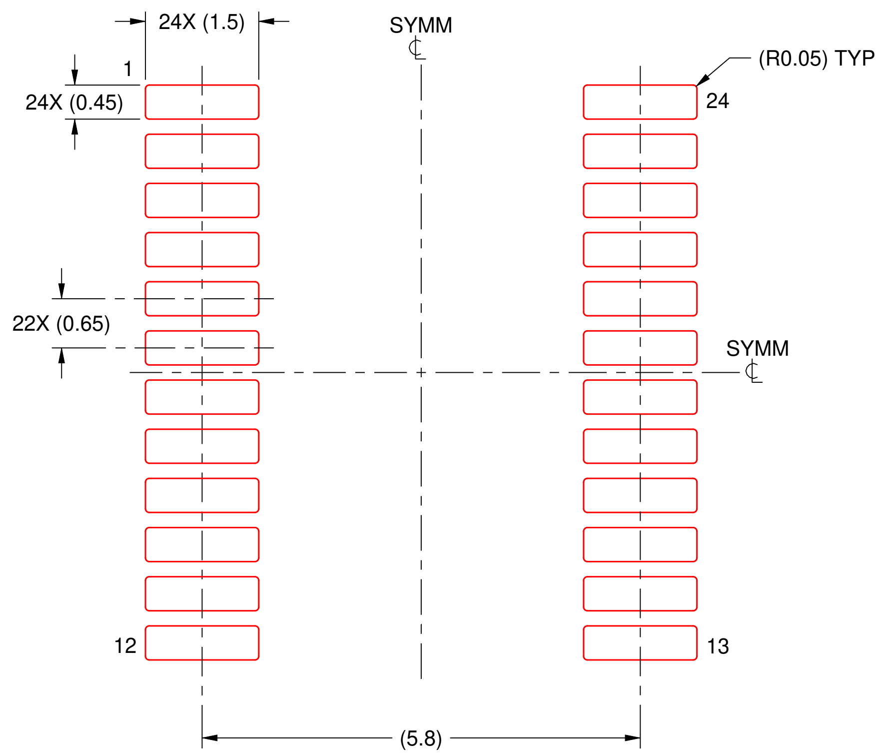


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.