SAM9N12/CN11-EK

User Guide

11186A–ATARM–29-Nov-12

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Section 1

Introduction

1.1 SAM9N12/CN11 Evaluation Kit

This User Guide introduces the SAM9N12 and SAM9CN11 Evaluation Kits and describes their development and debugging capabilities running on SAM9N12 and SAM9CN11 devices.

The Atmel® SAM9N12/CN11 Evaluation Kit is a fully-featured evaluation platform for the Atmel SAM9N12 and SAM9CN11 microcontrollers. The evaluation kit allows users to extensively evaluate, prototype and create application-specific designs.

SAM9N12/CN11 Evaluation Kit consists of two boards:

- The Evaluation Kit (EK) board
- The Display Module (DM) board

1.2 User Guide Content

This guide gives details on how the SAM9N12/CN11-EK has been designed. It is made up of 8 sections:

- Section 1 Introduction (including references, applicable documents)
- Section 2 Kit Contents
- Section 3 Power Up
- Section 4 Evaluation Kit Hardware
- Section 5 EK Schematics
- Section 6 Display Module Hardware
- Section 7 DM Schematics
- Section 8 Revision History

1.3 References and Applicable Documents

The documents listed below should be referred for more information on the SAM9CN11-EK.

Table 1-1. References and Applicable Documents

Title	Comment
SAM9N12/CN11 Datasheet	www.atmel.com

Section 2

Kit Contents

2.1 Deliverables

The Atmel SAM9N12/CN11 Evaluation Kit contains the following items:

- Board
  - One SAM9N12/CN11-EK board
  - One SAM9N12/CN11-DM board
- Power supply
  - Universal input AC/DC power supply with US, Europe and UK plug adapters
  - One 3V lithium battery type CR1225
- Cables
  - One serial RS232 cable
  - One micro A/B-type USB cable
  - One RJ45 crossed cable
- A Welcome letter

Figure 2-1. Unpacked SAM9N12/CN11-EK

Unpack and inspect the kit carefully. Contact your local Atmel distributor, should you have issues concerning the contents of the kit.

2.2 Evaluation Board Specifications

Table 2-1. SAM9N12/CN11 Evaluation Kit Specifications

Characteristics	Specifications
Clock speed	400 MHz PCK, 133 MHz MCK
Ports	Ethernet, USB, RS232, JTAG, Audio, SD card
Board supply voltage	5V DC from connector, or 5V DC from Micro USB receptacle
Temperature - operating - storage	 -10°C to + 50°C -40°C to + 85°C
Relative humidity	0 to 90% (non condensing)
Dimensions - SAM9N12/CN11-EK - SAM9N12/CN11-DM	 135 mm x 100 mm 135 mm x 70 mm
RoHS status	Compliant

2.3 Electrostatic Warning

The SAM9N12/CN11 Evaluation Kit is shipped in a protective anti-static package. The board system must not be subjected to high electrostatic potentials. We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

Section 3

Power Up

3.1 Power up the Board

Unpack the board, taking care to avoid electrostatic discharge. Unpack the power supply, select the right power plug adapter corresponding to that of your country, and insert it in the power supply.

Connect the power supply DC connector to the board and plug the power supply to an AC power plug. The board LCD should light up and display a graphic demo program. Then, click or touch icons displayed on the screen and enjoy the demo.

3.2 Battery

The SAM9N12/CN11-EK ships with a 3V coin battery.

This battery is not required for the board to start up.

The coin battery is provided for user convenience in case the user would like to exercise the date and time backup function of the SAM9N12/CN11 devices when the board is switched off.

3.3 Sample Code and Technical Support

After boot-up, designers can run sample code or their own application on the development kit. Users can download sample code and get technical support from the Atmel web site: http://www.atmel.com/.

3.4 Recovery Procedure

All boards of Evaluation Kit have passed strict test procedures before shipment. The demo software boots from SPI DataFlash® and stores the binary image in the NAND Flash. If the contents of either of the Flash have been deleted, follow the instructions below to recover it to the state as it was when shipped by Atmel.

Under the web page of SAM9N12/CN11-EK, find the test package of AT91SAM9N12/CN11-EK_test_xx_public.zip (xx is the version number), which is the file for Flash content burning. A step-by-step instruction is available in name of SAM9N12/CN11_EK_Test_Software on how to recover the contents and how to make test for each section of the boards.

Section 43

Evaluation Kit Hardware

4.1 Board Overview

This section introduces the Atmel SAM9N12/CN11 Evaluation Kit design. It introduces system-level concepts, such as power distribution, memory, and interface assignments.

The SAM9N12/CN11-EK board is built around on the integration of an ARM®926-based microcontroller (BGA 217 package) with on-board SDRAM, NAND-Flash and a set of popular peripherals. It is designed to provide a high performance processor evaluation solution with high flexibility for various kinds of applications.

Figure 4-1. SAM9N12 Board Architecture

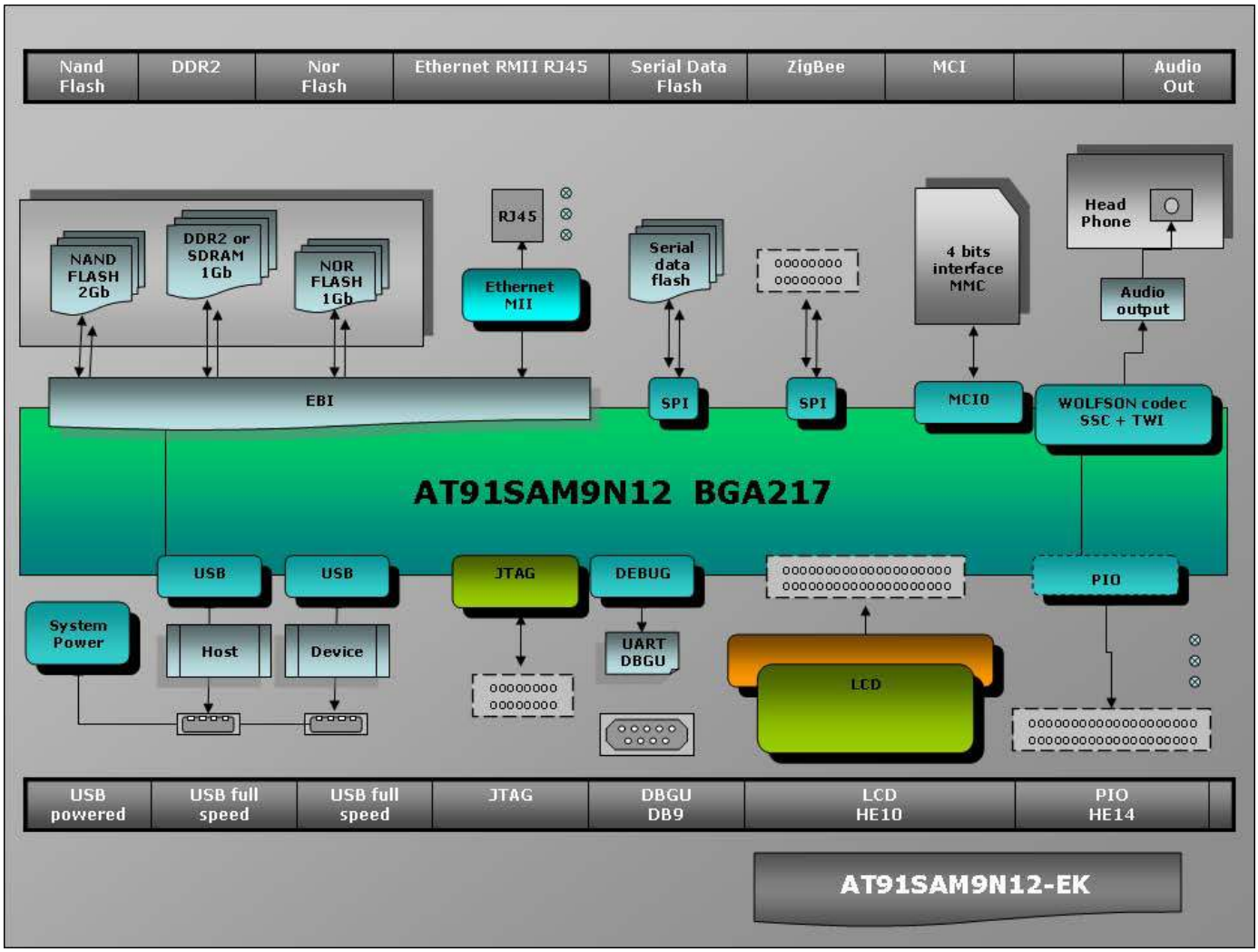
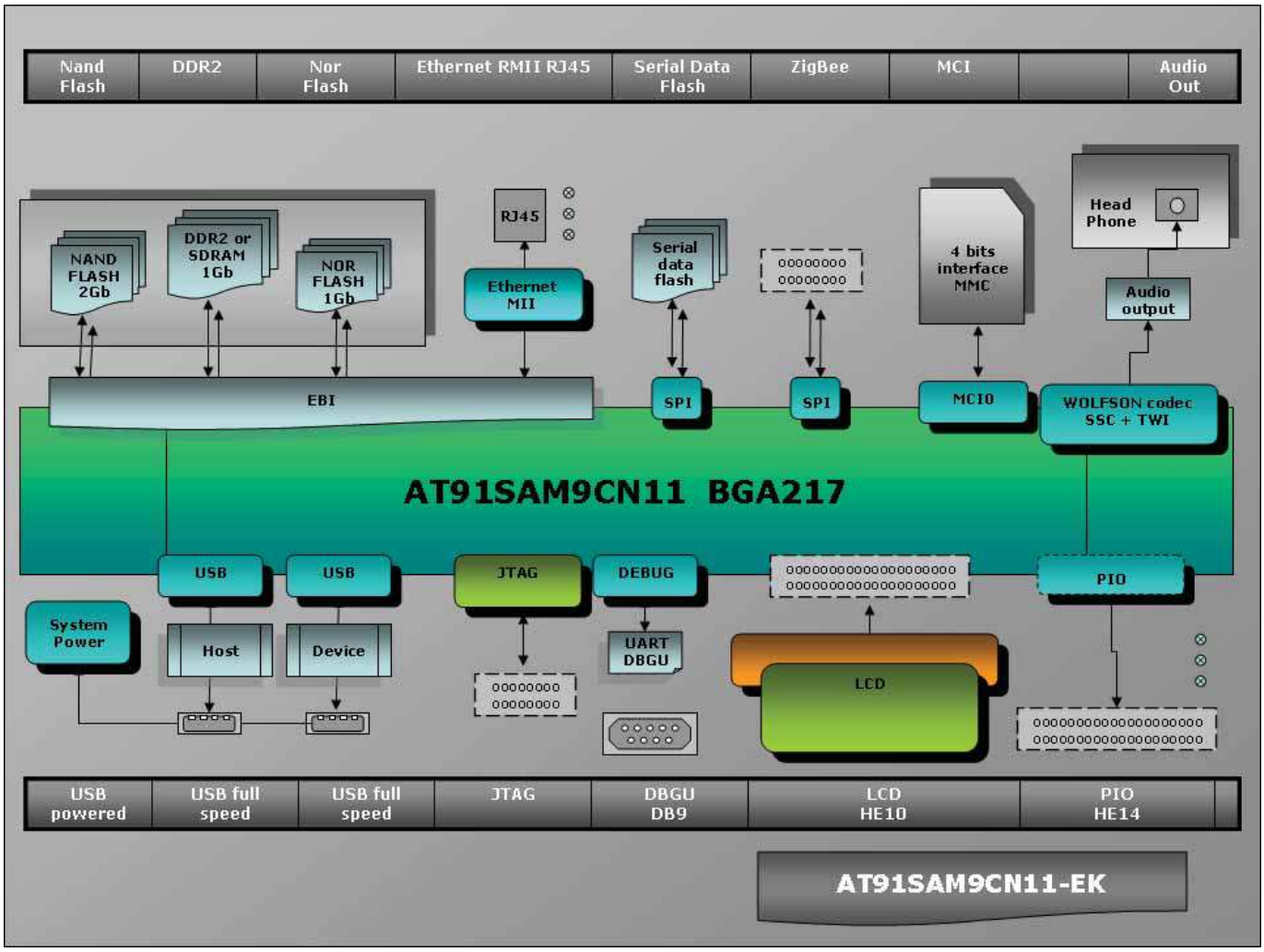


Figure 4-2. SAM9CN11 Board Architecture



4.2 Equipment List

4.2.1 Features List

Here is the list of the EK board components:

- SAM9N12/CN11 microcontroller BGA
  - 16 MHz crystal
  - 32.768 kHz crystal
- Memory
  - 1 Gbit DDR2 memory
  - 2 Gbits NAND Flash memory with chip selection control switch
  - Optional NOR Flash
  - 32 Mbits SPI serial DataFlash with chip selection control switch
  - 512 Kbits serial EEPROM
  - 1 Kbit 1-Wire EEPROM

  - SD/MMC interface
- Communication
  - One Ethernet Physical Transceiver Layer with RJ45 connector
  - UART DBGU port with level shifter IC
  - JTAG/ICE port
  - USB Host and Device
  - ZigBee®
- Add-on Display Module
  - TFT LCD module with touch screen
  - QTouch® elements for user QTouch: K1 to K4
- Audio CODEC with input stereo headphone and microphone
- On-board power regulation and backup battery
- Two user LEDs and one power LED
- System buttons: NRST, WKUP, OE_CS
- One user button

4.2.2 Interface Connection

The SAM9N12/CN11-EK board includes hardware interfaces such as:

- DC power supply (J1)
- Backup battery (Bt1)
- USB host, type A connector (J2)
- USB device, micro B connector (J3)
- One Ethernet 10/100 interface through an ETH controller (J16)
- DBGU (RX and TX only) connected to a 9-way male RS232 connector (J11)
- JTAG, 20 pin IDC connector (J4)
- SD connector (J8)
- Headphone (J13), line-in (J15), on board mic-phone (mic1)
- DM board connection for QTouch and TFT LCD display with touch screen and backlight (J9, J10)
- ZigBee connector (J12)
- Three IO expansion ports (J5, J6, J7)
- Test points (various test points are located throughout the board)

4.2.3 Configuration Items

- Power selection switch (SW1)
- Push button - NAND/DataFlash OS_CS (PB1)
- Push button - NRST, board reset (PB2)
- Push button - Wake-up (PB3)
- Push button - PB_USER (PB4)

Figure 4-3. SAM9N12-EK Board Layout

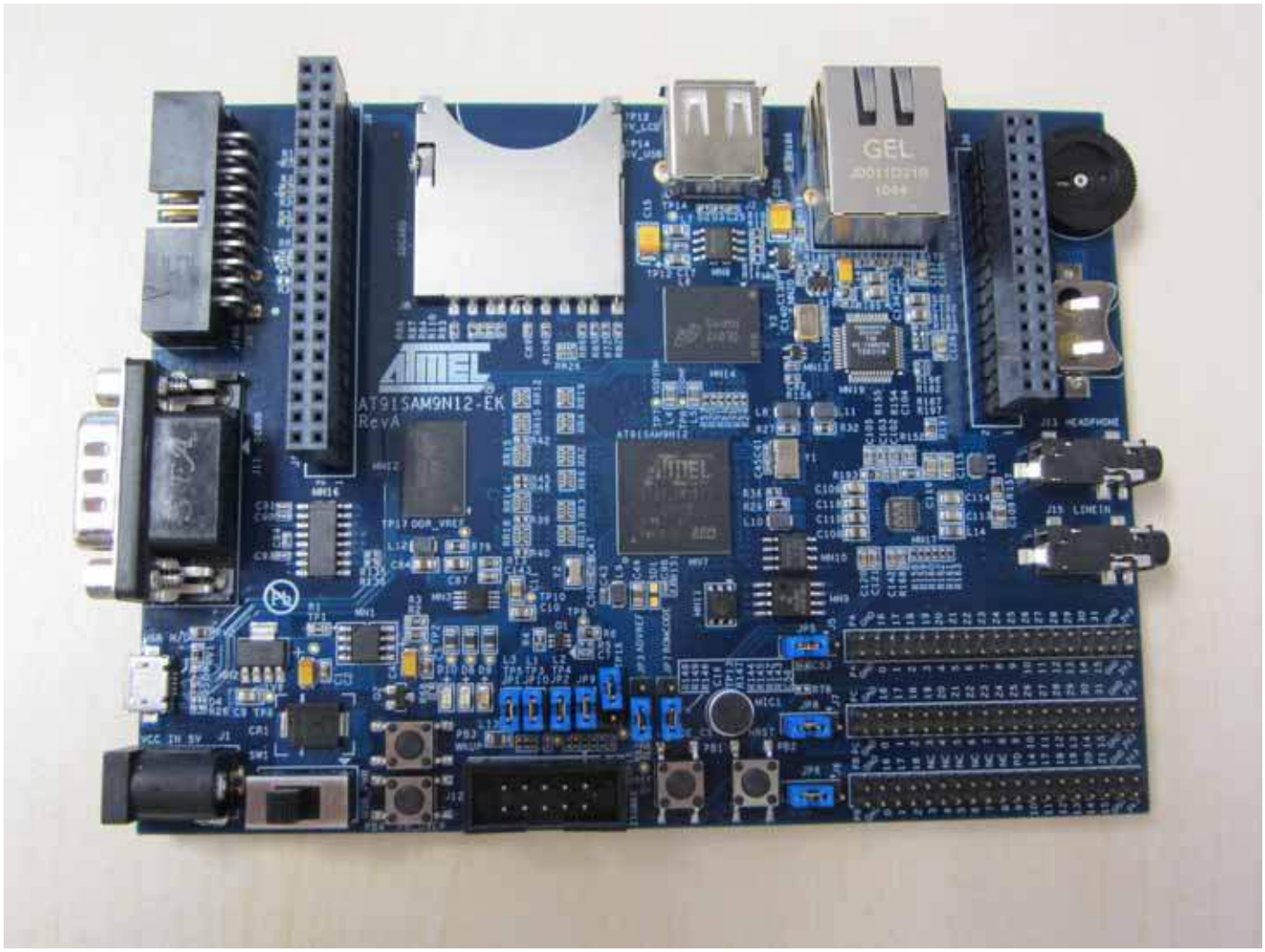
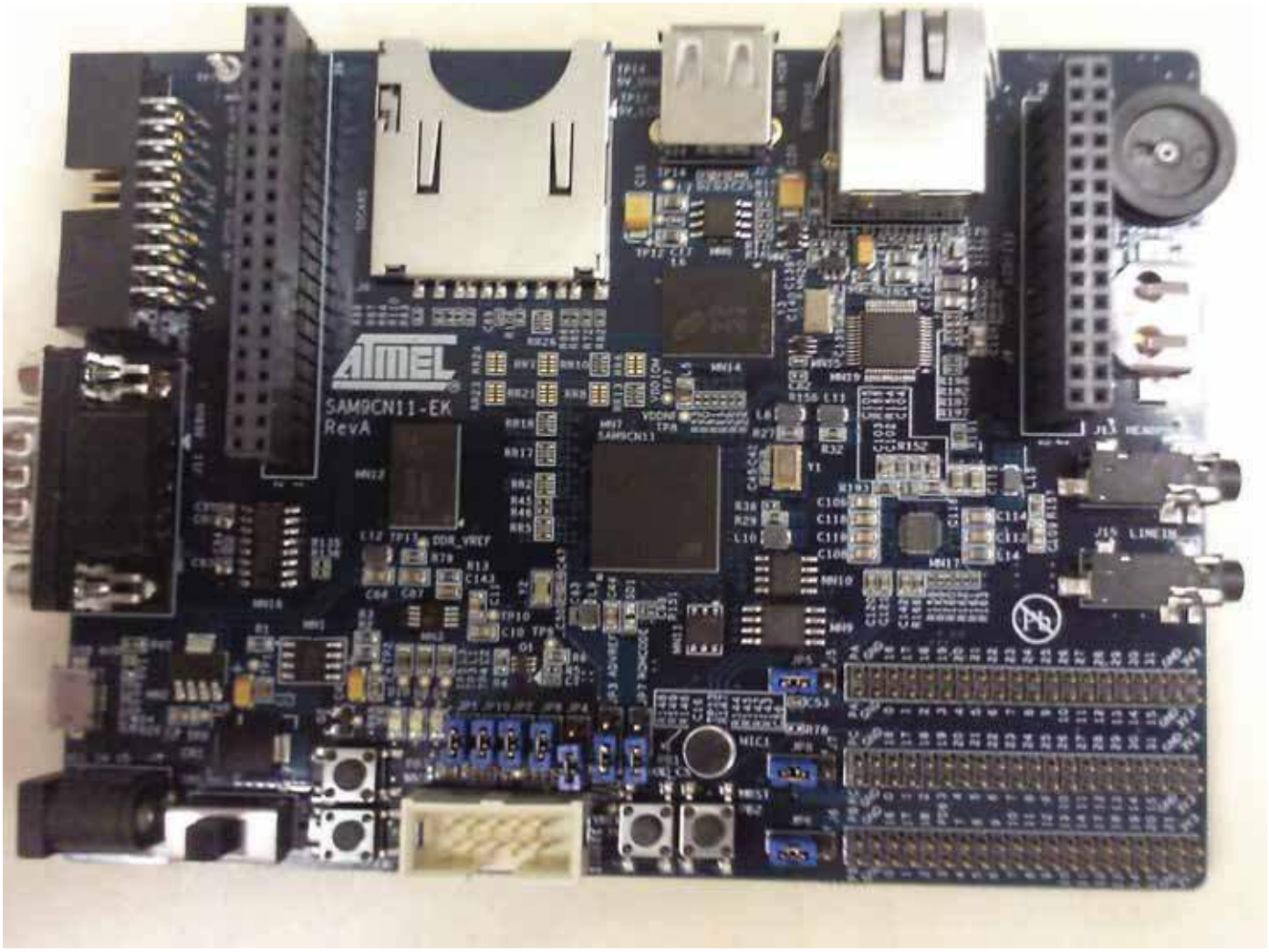


Figure 4-4. SAM9CN11-EK Board Layout



4.3 Function Blocks

4.3.1 Processor

The EK board is equipped with a SAM9N12/CN11 device in BGA217 package. The processor runs at a nominal frequency of 400 MHz for the core and 133 MHz for the system bus.

4.3.2 Clock Distribution

The SAM9N12/CN11-EK board includes three clock systems. Two of the clock systems are alternatives for the SAM9N12/CN11 main clock and one clock system is an oscillator used for the Ethernet controller chip.

Table 4-1 lists the main components associated with these clock systems.

Table 4-1. Main Components Associated with the Clock Systems

QTY	Description	Component assignment
1	Crystal for Internal Clock, 16 MHz	Y1
1	Crystal for RTC Clock, 32.768 kHz	Y2
1	Crystal for Ethernet Clock, 25 MHz	Y3

4.3.3 Reset and Wake-up Circuitry

The reset sources for the EK board are:

- Power-on reset
- Push-button reset (PB2)
- JTAG reset from an in-circuit emulator (JTAG interface is equipped on EK board)

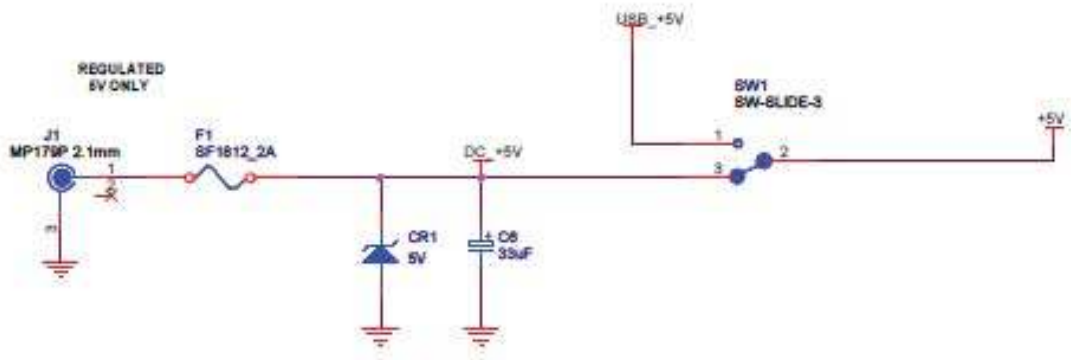
To disable any bootable content in NAND Flash or DataFlash, please refer to "Push Buttons" .

4.3.4 Power Supplies

The SAM9N12/CN11-EK board evaluation and development platform embeds all the necessary power rails required for the SAM9N12/CN11 processor and peripherals. The SAM9N12/CN11-EK board can be supplied by either a USB connection via J3 or a 5V DC block through input J1 (refer to usb schematic).

A manual power supply selection (SW1) between the USB supply and the 5V power supply is provided to select the main power line.

Figure 4-5. Power Input



Connector J1 is provided for use with a DC adapter. It is a 2.5 mm male power jack. Table 4-2 below lists the DC adapter connector pinouts.

Table 4-2. Power Input Configuration

PIN	INPUT
1 (Center)	Positive
2	No connection
3 (Outside)	Ground

4.3.5 Power Rails

The SAM9N12/CN11-EK Board contains three regulated power supplies:

- 3.3V DC supply
- 1.8V DC supply
- 1.0V DC core supply

The outputs of these regulated power supplies are distributed as necessary to the circuits on boards.

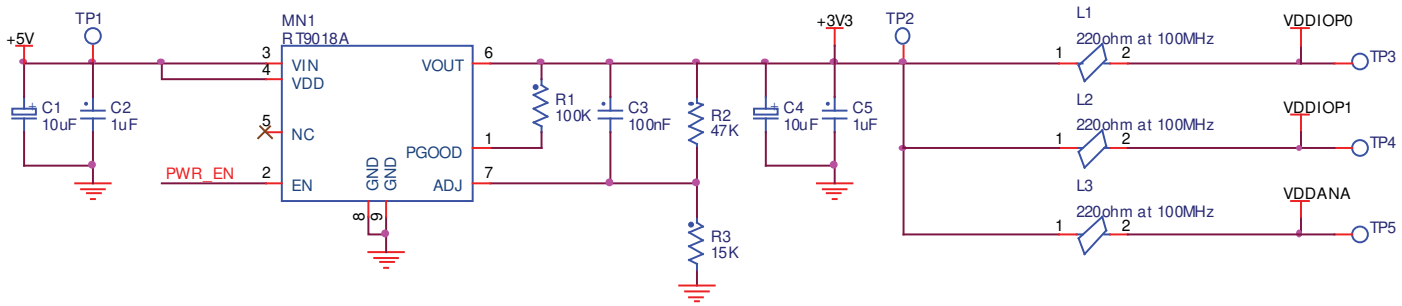
The USB supplies and the 5V input DC block are further regulated to 3.3V. The main 3.3V regulator is based on a RICHTEK RT9018A low dropout regulator providing a fixed output of 3.3V. Its output is used for:

- VDDIOP0
- VDDIOP1
- VDDANA
- VDDOSC
- VDDUSB
- VDDFUSE

When the 3.3V supply is present, power LED D10 is lit.

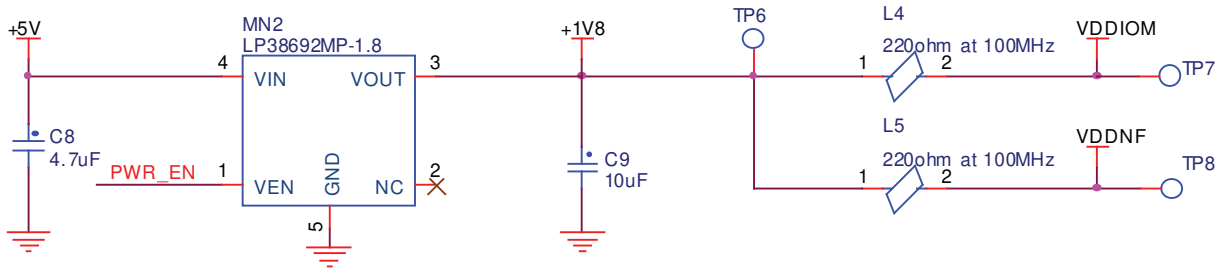
Test points TP2 to TP5 are used to perform testing.

Figure 4-6. 3.3V Supply



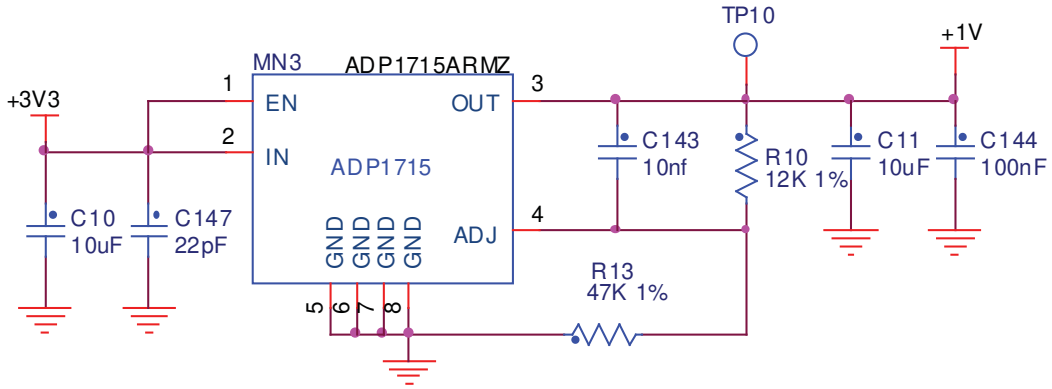
The 1.8V DC core supply is based on an LDO LP38692MP IC. It is powered by the 5V DC supply. Its output is used for VDDIOM and VDDNF. Test point TP6 is used to perform testing.

Figure 4-7. 1.8V Supply



The 1.0V DC core supply is based on an LDO ADP1715AR. It is powered by the output of the 3.3V CC supply. Its output is used for VDDCORE and VDDPLL. Test point TP10 is used to perform testing.

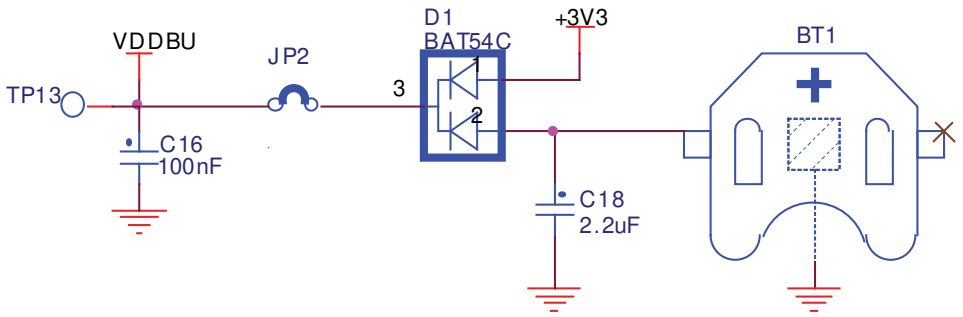
Figure 4-8. 1V Supply



4.3.6 Battery Backup

VDDBU pin is powered from the 3.3V rail and a backup battery BT1 via a dual Schottky diode D1. Test point TP13 and jumper JP2 are used to perform testing.

Figure 4-9. Backup Battery



Note: Test points (TPn) are provided for easy access to each of the regulated power lines.

4.3.7 Memory

4.3.7.1 DDR2 SDRAM

The SAM9N12/CN11 processor uses DDR2 SDRAM as the system memory. The DDR2 interface uses 1.8V power. The DDR2 chips and SAM9N12/CN11 processor are connected directly. The interface is 1.8V provided by an on-board voltage regulator.

VREF, which is half the interface voltage, or 0.9V, is provided by a simple voltage divider of 1.8V.

- One 1 Gbit DDR2-SDRAM memory (Micron MT47H64M16HR 8Meg*16*8), 16 bits data interface connected to D[0-15].

4.3.7.2 NAND FLASH

The SAM9N12/CN11-EK has native support for NAND Flash memory and implements an 8-bit NAND Flash with 2 Gbits in size.

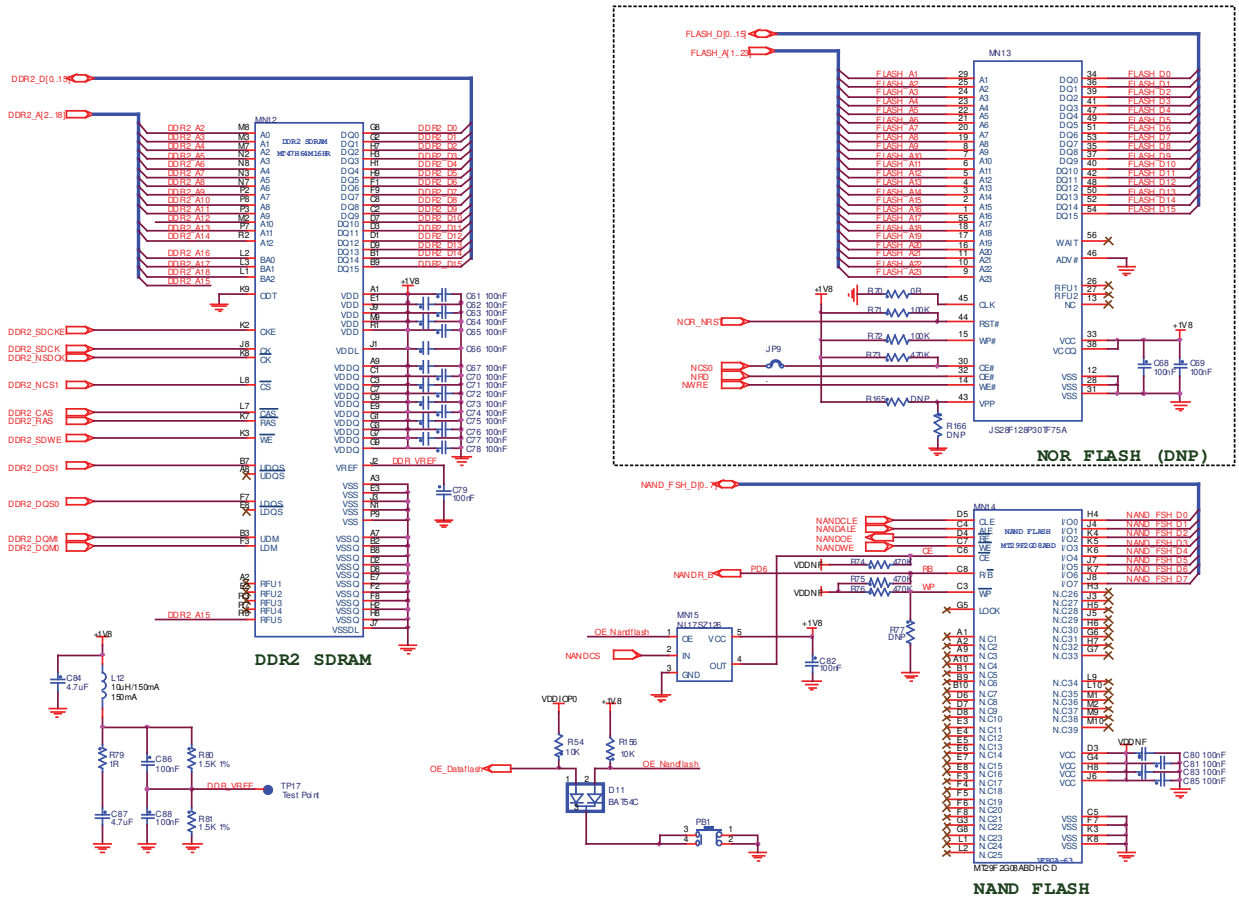
- One 2 Gbits NAND Flash (Micro MT29F2G08ABDHC), 16 bits data interface connected to D[0-15].

4.3.7.3 NOR FLASH

The SAM9N12/CN11-EK provides an optional 128 Mbits of Flash memory using a chip-select signal. The Flash memory is used with the 16-bit port size.

- One reserved position for 128 Mbits NOR Flash (Numonyx JS28F128P30TF75A).

Figure 4-10. External memory



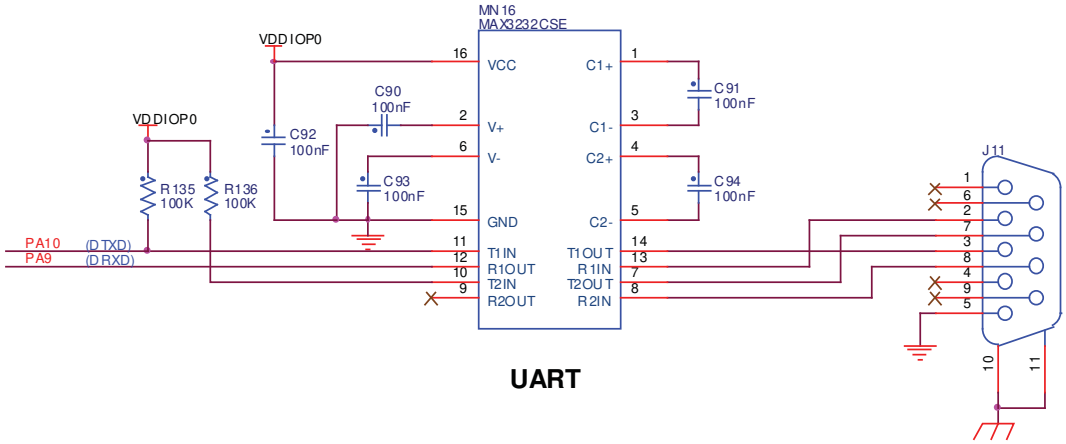
A 3-state buffer is in serial with NAND flash's CE signal, with PB1 to give a manually disable manner for NAND boot.

4.3.8 UART DBGU

The Universal Asynchronous Receiver Transmitter features a two-pin UART that can be used for communication and trace purposes and offers an ideal medium for in-situ programming solutions.

This two-pin UART (TXD and RXD only) is buffered through an RS232 transceiver MN16 and brought to the DB9 male connector J11.

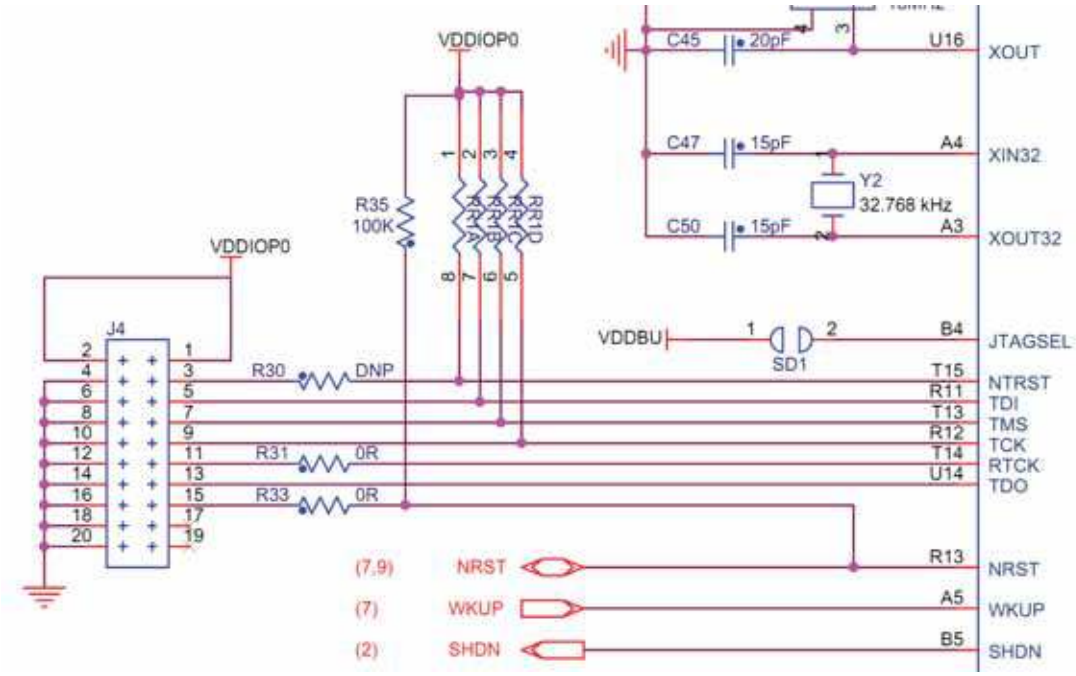
Figure 4-11. UART



4.3.9 JTAG Interface

The SAM9N12/CN11-EK board includes a JTAG interface port (J4), to provide debug level access to the processor. The JTAG port is a 20-pin male connector. This port provides the required interface for in-circuit emulators such as ARM's Multi-ICE.

Figure 4-12. JTAG

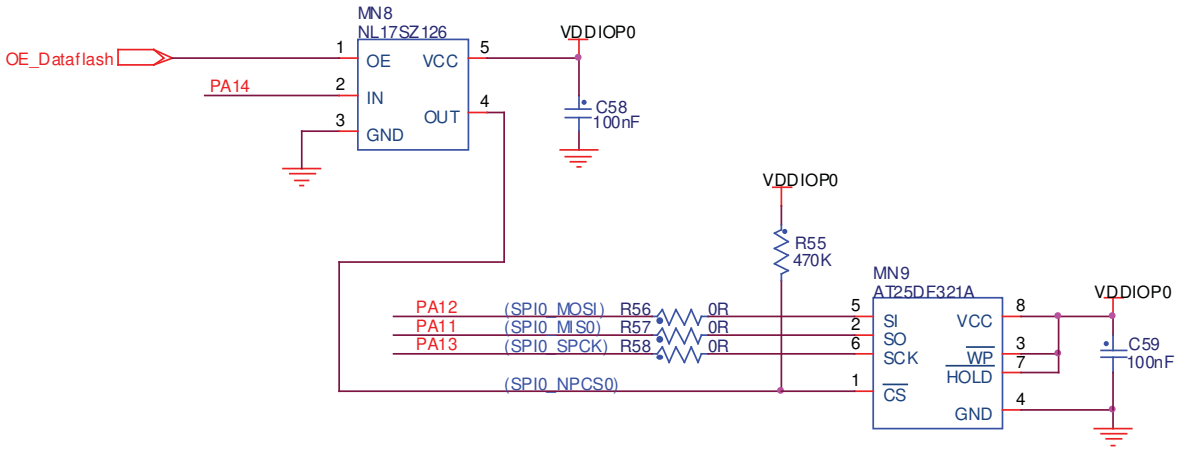


4.3.10 Serial Peripheral Interface (SPI) Controller

The SAM9N12/CN11 serial processor provides two high-speed Serial Peripheral Interface (SPI) controllers. One port is used to interface with the on-board serial DataFlash.

A 3-state buffer is in serial with DataFlash CS signal, with PB1 to give a manually disable manner for DataFlash boot.

Figure 4-13. SPI DataFlash

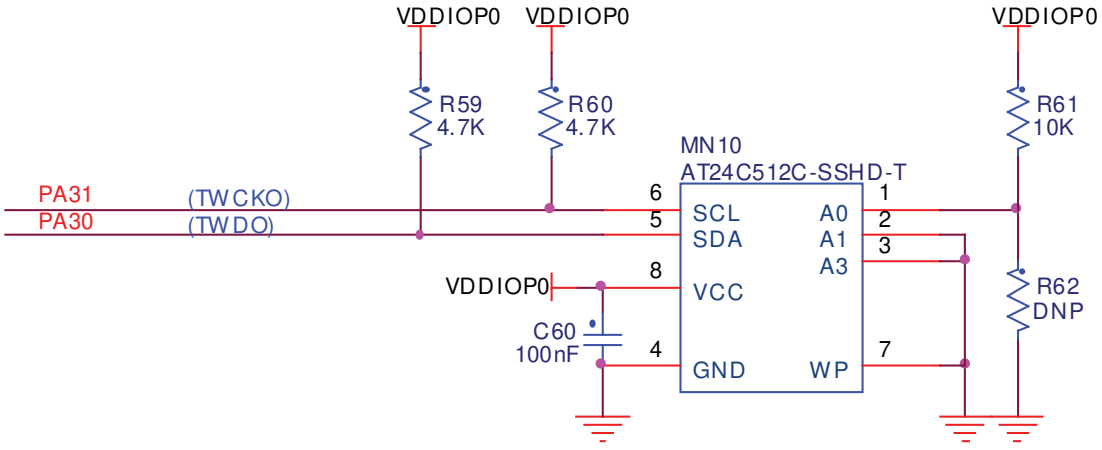


4.3.11 Two Wire Interface (TWI)

The SAM9N12/CN11 processor has two full speed (400 kHz) master/slave I2C serial controllers. The controllers are fully compatible with the industry standard I2C interfaces. On the EK board, TWI0 port is used to interface with serial EEPROM, QTouch device and audio CODEC interface.

SAM9N12/CN11 processor supports TWI EEPROM boot at the device address of 0x50. On board, the EEPROM device address is 0x51. Customer needs to dismount R61 and mount R62 as 10 kohms, if EEPROM boot is needed.

Figure 4-14. EEPROM



4.3.12 USB Ports

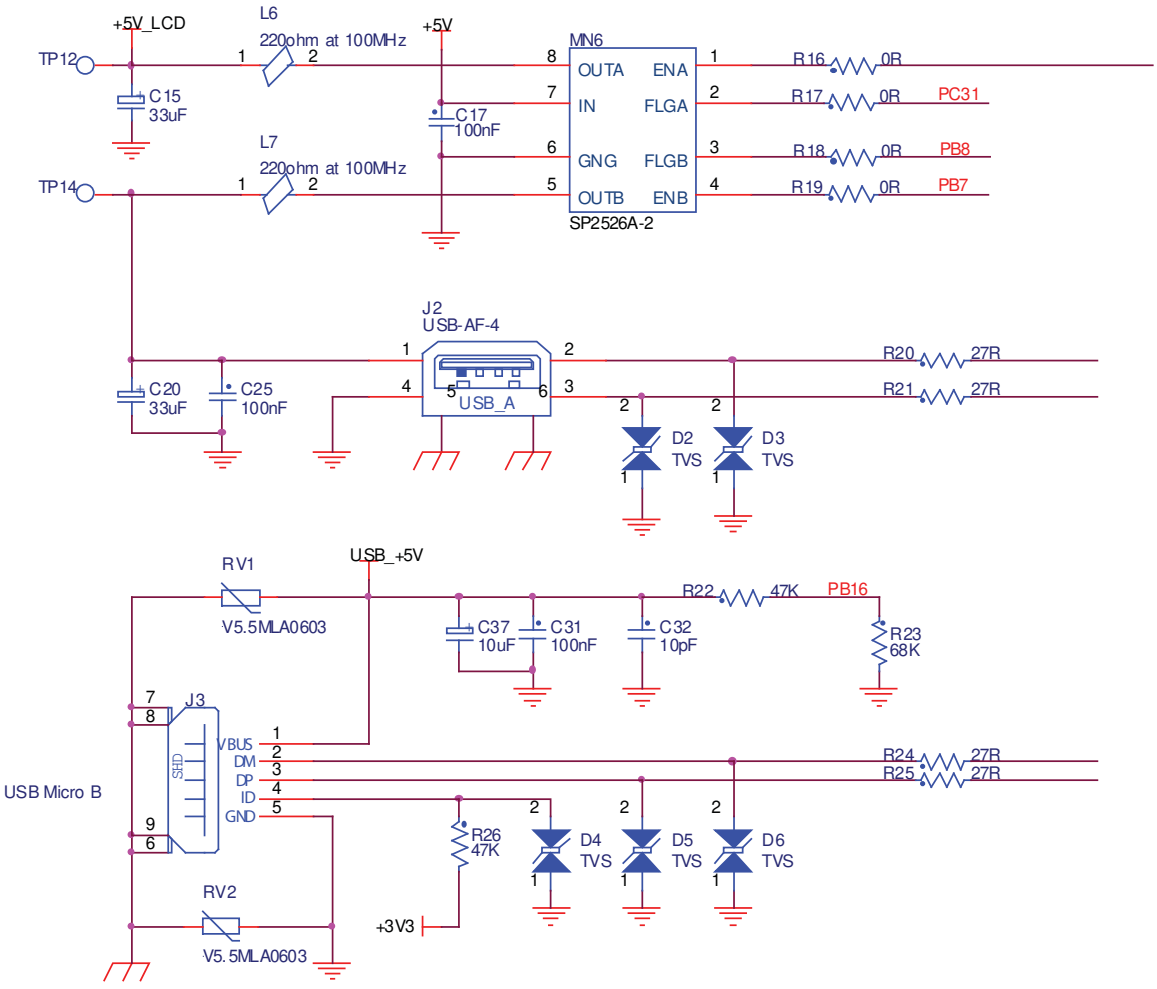
The SAM9N12/CN11-EK features two full speed (OHCI) USB ports:

- Host full speed, type A USB receptacle, J2
- Device full speed, micro B USB receptacle, J3

SAM9N12/CN11-EK features USB power function from device port J3. SW1 functions as switch between USB supply and DC input jack J1.

The USB host ports are equipped with 500 mA power switch for bus-powered applications.

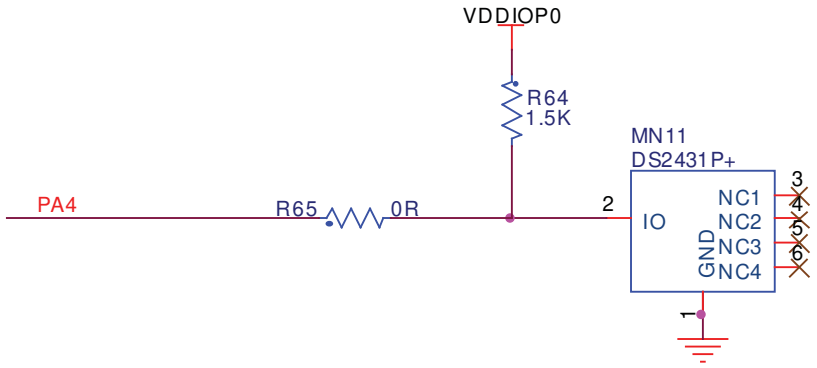
Figure 4-15. USB Port



4.3.13 1-Wire EEPROM

The SAM9N12/CN11 Evaluation Kit uses 1-Wire device as “soft label” to store the information such as chip type, manufacture’s name, production date, etc.

Figure 4-16. 1-Wire

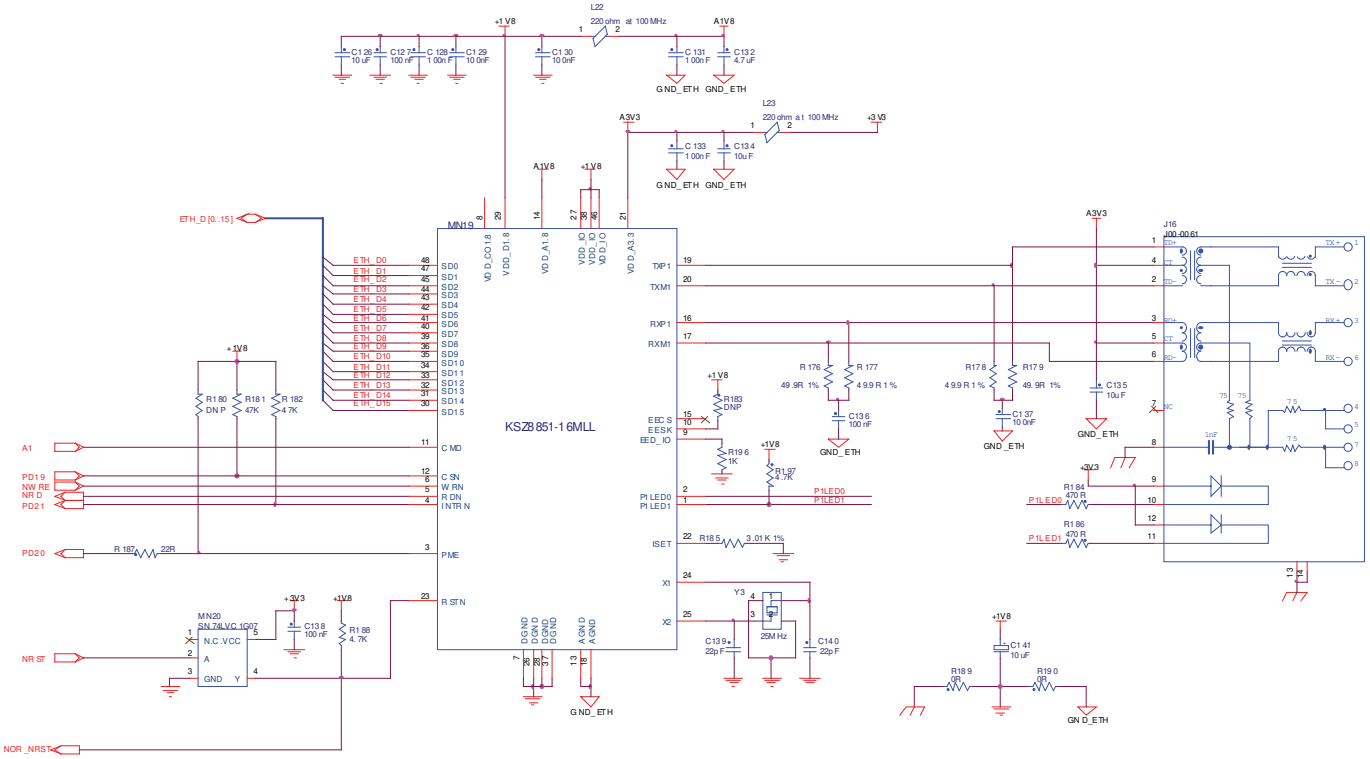


4.3.14 ETH on EBI

The SAM9N12/CN11 Evaluation Kit uses EBI-based 8-bit EMAC controller KSZ8851 to implement a 10/100 Ethernet access. The board integrates an RJ45 connector with embedded transformer, and two status LEDs.

For more information about the Ethernet controller device, refer to the Micrel KSZ8851 manufacturer's datasheet.

Figure 4-17. Ethernet



4.3.15 Audio

The SAM9N12/CN11-EK includes a WM8904 audio CODEC for digital sound input and output. This interface includes features and audio jacks for:

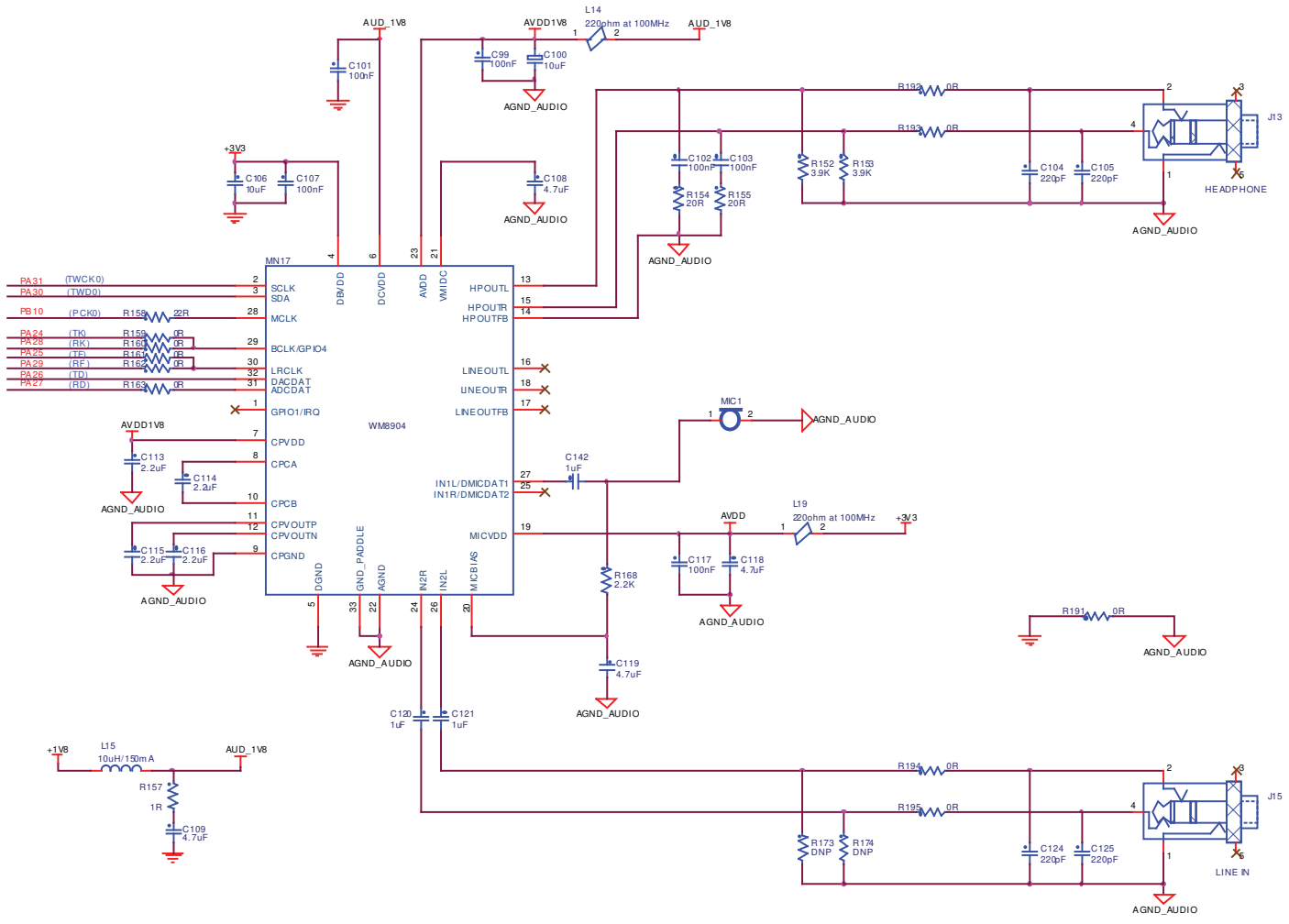
- Line In (J13)
- Headphone output (J15)
- Microphone on board

The SAM9N12/CN11 programmable clock output PCK0 is used to generate the WM8904 master clock (MCLK).

The bit clock is shared; it can be the SSC Transmitter Clock (TK) or the Receiver Clock (RK). The default setting on SAM9N12/CN11-EK is TK and RK shorted together through R159/R160. Please note that trying different ADC/DAC rates would mean different RK/TK rates; this default setting can be modified.

The 0-ohm resistors R159 to R163 have been implemented to offer a disconnection possibility (freeing these dedicated PIO lines for other custom usages).

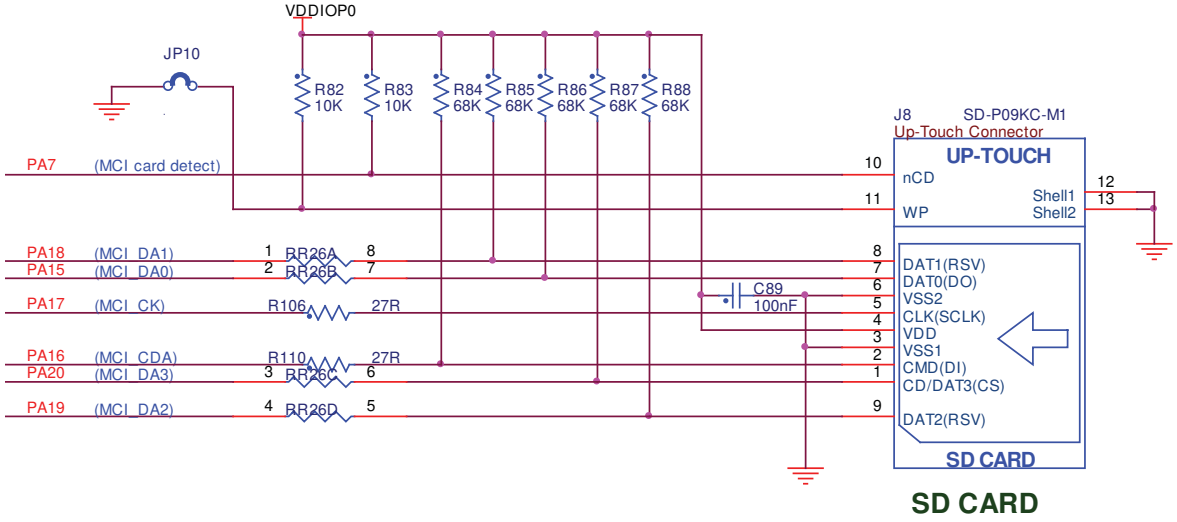
Figure 4-18. Audio CODEC



4.3.16 SD Card

The SAM9N12/CN11 has a high-speed Multimedia Card Interface (MCI). It is used as a 4-bit interface connected to an SD card slot.

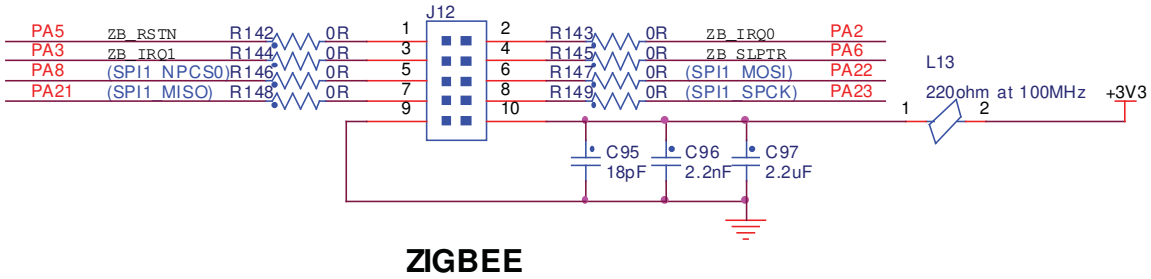
Figure 4-19. SD Card



4.3.17 ZigBee Interface

The EK board has a 10-pin male connector for the Atmel RZ600 ZigBee module. DNP 0-ohm resistors have been implemented in series with the PIO lines that are used elsewhere in the design. Thereby, it enables their individual disconnection, should a conflict occur in user application.

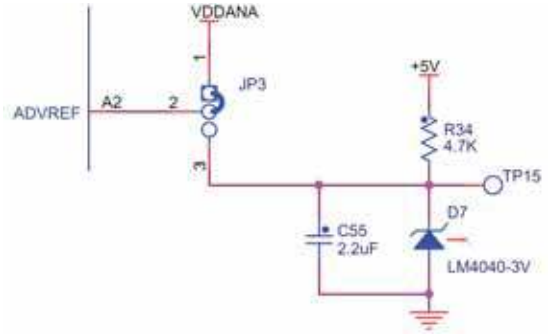
Figure 4-20. ZigBee



4.3.18 Analog Interface

The 3.0V voltage reference is based on an LM4040 (Precision Micropower Shunt Voltage Reference). This ADVREF level can be set as 3.0V or 3.3V via the jumper JP3.

Figure 4-21. Analog Reference



A 10 kohm potentiometer (VR1) is connected to AD6 port PB17 to implement an easy access to ADC programming and debugging (or to implement an analog user control such as display brightness, volume, etc).

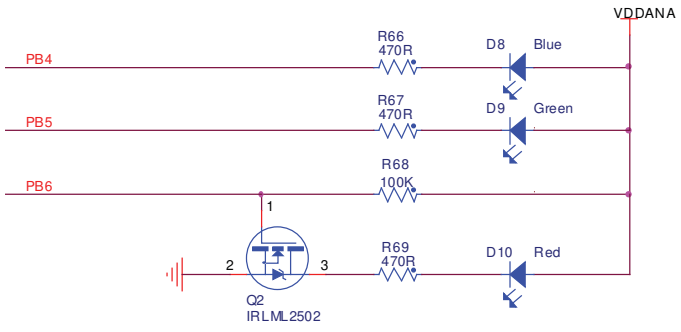
Figure 4-22. Potentiometer

4.3.19 LED Indicators

There are three LEDs for general purpose on the SAM9N12/CN11-EK board:

- D8 blue and D9 green LEDs are user defined and controlled by the GPIO.
- D10 red LED is a power LED indicating that the 3.3V rail is enabled. It can also be controlled by the GPIO (by default, the GPIO is disabled and an on-board pull-up to 3.3V lights the LED).

Figure 4-23. LED



4.3.20 Push Buttons

SAM9N12/CN11-EK has three mechanical push buttons for system application (PB1 to PB3) and one for free use (PB4).

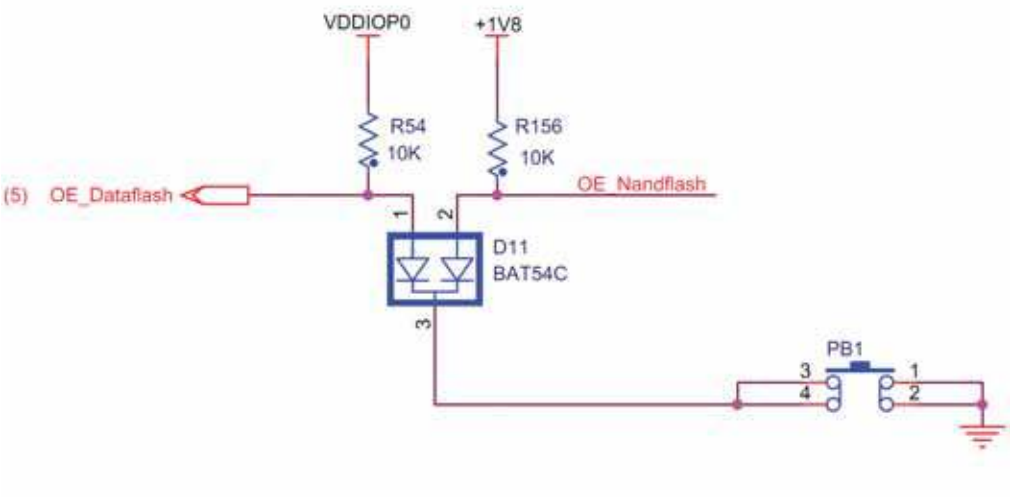
4.3.20.1 PB1 Output Enable Chip Select

Access to the RomBoot:

1. Press simultaneously the PBs OE-CS and NRST
2. Release the PB NRST
3. Then release PB OE-CS

The program boots to the ROM code whatever the contents of the NAND Flash or serial DataFlash. Please refer to SAM9N12/CN11 datasheet boot strategy for details.

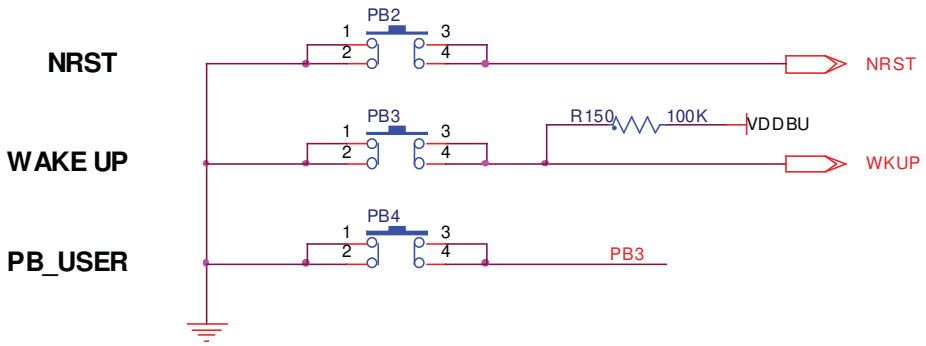
Figure 4-24. PB1



4.3.20.2 PB2 NRST

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components, or be asserted low externally to reset the microcontroller. It will reset the core and the peripherals except for the backup region.

Figure 4-25. Push Button



4.3.21 Expansion Ports

Most of GPIOs are led to expansion ports J5, J6, J7.

LCD and touch screen connector include J9 and J10 to interface DM board.

Figure 4-26. PIO Expansion Ports

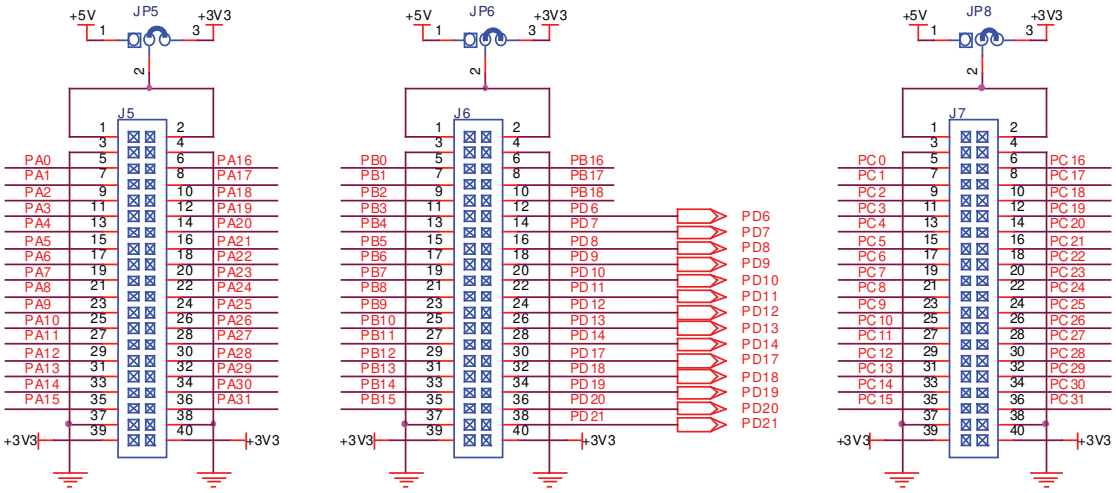
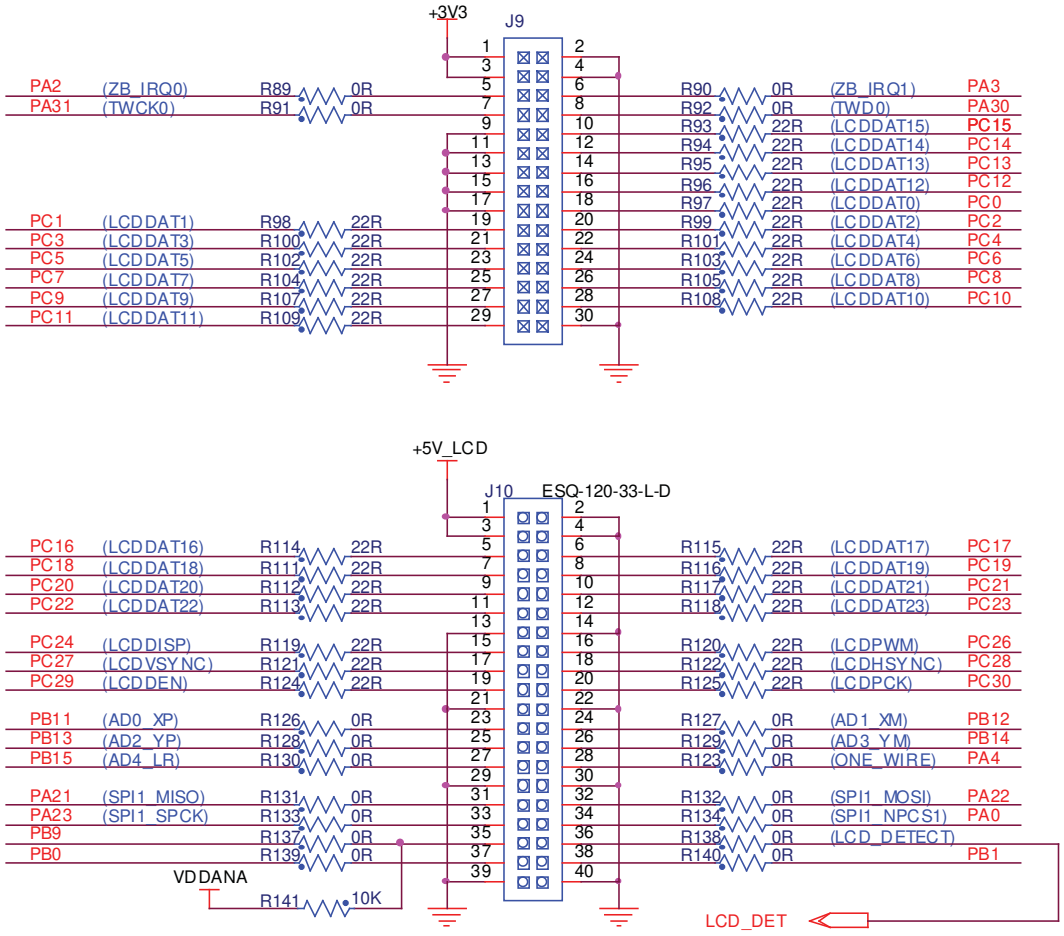


Figure 4-27. LCD Expansion Ports



4.3.22 PIO Usage

- PIO A Pin Assignment

Table 4-3. PIO A Pin Assignment and Signal Descriptions

Signal	Alternate	Periph A	Periph B	Periph C	
PA0		TXD0	SPI1_NPCS1		(LCD connector)
PA1		RXD0	SPI0_NPCS2		
PA2		RTS0			ZB_IRQ0
PA3		CTS0			ZB_IRQ1
PA4		SCK0			One Wire
PA5		TXD1			ZB_RSTN
PA6		RXD1			ZB_SLPTR
PA7		TXD2	SPI0_NPCS1		MCI card detect
PA8		RXD2	SPI1_NPCS0		ZigBee
PA9		DRXD			DBGU
PA10		DTXD			DBGU
PA11		SPI0_MISO	MCI_DA4		Serial DataFlash
PA12		SPI0_MOSI	MCI_DA5		Serial DataFlash
PA13		SPI0_SPCK	MCI_DA6		Serial DataFlash
PA14		SPI0_NPCS0	MCI_DA7		Serial DataFlash
PA15		MCI_DA0			MCI
PA16		MCI_CDA			MCI
PA17		MCI_CK			MCI
PA18		MCI_DA1			MCI
PA19		MCI_DA2			MCI
PA20		MCI_DA3			MCI
PA21		TIOA0	SPI1_MISO		ZigBee
PA22		TIOA1	SPI1_MOSI		ZigBee
PA23		TIOA2	SPI1_SPCK		ZigBee
PA24		TCLK0	TK		Audio
PA25		TCLK1	TF		Audio
PA26		TCLK2	TD		Audio
PA27		TIOB0	RD		Audio
PA28		TIOB1	RK		Audio
PA29		TIOB2	RF		Audio
PA30		TWD0	SPI1_NPCS3		Audio & LCD connector
PA31		TWCK0	SPI1_NPCS2		Audio & LCD connector

■ PIO B Pin Assignment

Table 4-4. PIO B Pin Assignment and Signal Descriptions

Signal	Alternate	Periph A	Periph B	Periph C	
PB0			RTS2		(LCD connector)
PB1			CTS2		(LCD connector)
PB2			SCK2		JUMPER to GND
PB3			SPI0_NPCS3		PB_USER1
PB4					USER_LED1
PB5					USER_LED2
PB6	AD7				PWR_LED
PB7	AD8				EN5V_HOST
PB8	AD9				OVCUR_USB
PB9	AD10		PCK1		(LCD connector)
PB10	AD11		PCK0		Audio
PB11	AD0		PWM0		TSC
PB12	AD1		PWM1		TSC
PB13	AD2		PWM2		TSC
PB14	AD3		PWM3		TSC
PB15	AD4				(TSC)
PB16	AD5				VBUS_SENSE
PB17	AD6				Analog input
PB18		IRQ	ADTRG		LCDHSYNC (+0R)

■ PIO C Pin Assignment

Table 4-5. PIO C Pin Assignment and Signal Descriptions

Signal	Alternate	Periph A	Periph B	Periph C	
PC0		LCDDAT0		TWD1	LCD
PC1		LCDDAT1		TWCK1	LCD
PC2		LCDDAT2		TIOA3	LCD
PC3		LCDDAT3		TIOB3	LCD
PC4		LCDDAT4		TCLK3	LCD
PC5		LCDDAT5		TIOA4	LCD
PC6		LCDDAT6		TIOB4	LCD
PC7		LCDDAT7		TCLK4	LCD
PC8		LCDDAT8		UTXD0	LCD
PC9		LCDDAT9		URXD0	LCD
PC10		LCDDAT10		PWM0	LCD
PC11		LCDDAT11		PWM1	LCD
PC12		LCDDAT12		TIOA5	LCD
PC13		LCDDAT13		TIOB5	LCD
PC14		LCDDAT14		TCLK5	LCD
PC15		LCDDAT15		PCK0	LCD
PC16		LCDDAT16		UTXD1	LCD
PC17		LCDDAT17		URXD1	LCD
PC18		LCDDAT18		PWM0	LCD
PC19		LCDDAT19		PWM1	LCD
PC20		LCDDAT20		PWM2	LCD
PC21		LCDDAT21		PWM3	LCD
PC22		LCDDAT22	TXD3		LCD
PC23		LCDDAT23	RXD3		LCD
PC24		LCDDISP	RTS3		LCD
PC25			CTS3		EN5V_LCD
PC26		LCDPWM	SCK3		LCD
PC27		LCDVSYNC		RTS1	LCD
PC28		LCDHSYNC		CTS1	LCD
PC29		LCDDEN		SCK1	LCD
PC30		LCDPCK			LCD
PC31		FIQ		PCK1	OVCUR_LCD

■ PIO D Pin Assignment

Table 4-6. PIO D Pin Assignment and Signal Descriptions

Signal	Alternate	Periph A	Periph B	Periph C	
PD0		NANDOE			NAND Flash
PD1		NANDWE			NAND Flash
PD2		A21/NANDALE			NAND Flash
PD3		A22/NANDCLE			NAND Flash
PD4		NCS3			NAND Flash
PD5		NWAIT			
PD6		D16			NAND Flash
PD7		D17			NAND Flash
PD8		D18			NAND Flash
PD9		D19			NAND Flash
PD10		D20			NAND Flash
PD11		D21			NAND Flash
PD12		D22			NAND Flash
PD13		D23			NAND Flash
PD14		D24			
PD15		D25	A20		
PD16		D26	A23		
PD17		D27	A24		
PD18		D28	A25		
PD19		D29	NCS2		
PD20		D30	NCS4		
PD21		D31	NCS5		ETH INT

4.4 Connectors

4.4.1 Power Supply

Figure 4-28. Power Supply Connector J1

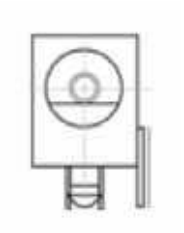


Table 4-7. Power Supply Connector J1 Signal Descriptions

Pin	Mnemonic	Signal description
1	Center	+5V
2		Floating
3		GND

4.4.2 JTAG/ICE Connector

Figure 4-29. JTAG J4

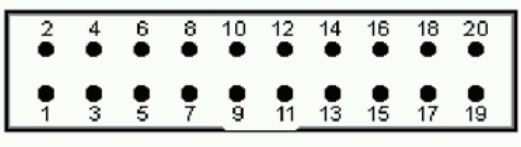


Table 4-8. JTAG/ICE Connector J4 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VTref. 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply. 3.3V power	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST TARGET RESET - Active-low output signal that resets the target	JTAG Reset. Output from SAM-ICE to the reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground.

Table 4-8. JTAG/ICE Connector J4 Signal Descriptions

5	TDI TEST DATA INPUT - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground.
7	TMS TEST MODE SELECT	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground.
9	TCK TEST CLOCK - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
10	GND	Common ground.
11	RTCK - Input return test clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Common ground.
13	TDO JTAG TEST DATA OUTPUT - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground.
15	nSRST RESET	Active-low reset signal. Target CPU reset signal.
16	GND	Common ground.
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Common ground
19	RFU	This pin is not connected in SAM-ICE
20	GND	Common ground

4.4.3 DBGU

Figure 4-30. DBGU Connector J11

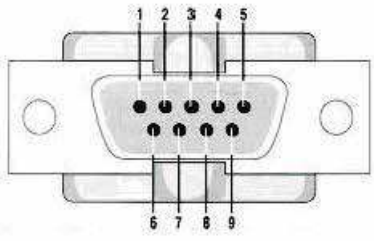


Table 4-9. DBGU Connector J11 Signal Descriptions

Pin	Mnemonic	PIO (Via translator)	Description
1, 4, 6, 9			No connection
2	RXD (Received Data)	PA9	RS232 serial data output signal
3	TXD (Transmitted Data)	PA10	RS232 serial data input signal
5	GND		Common ground
7	RTS (Request To Send)		Not used
8	CTS (Clear To Send)		Not used
Mechanical pins			Shield

4.4.4 USB MicroB

Figure 4-31. USB Device Micro B Connector J3

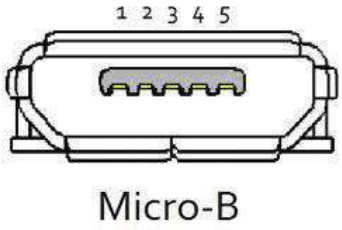


Table 4-10. USB Device Micro B Connector J3 Signal Descriptions

Pin	Mnemonic	Description
1	Vbus	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	On the go identification
5	GND	Common ground
6, 7, 8, 9	Shield	Mechanical pins

4.4.5 USB Type A port

Figure 4-32. USB Type A Port J2

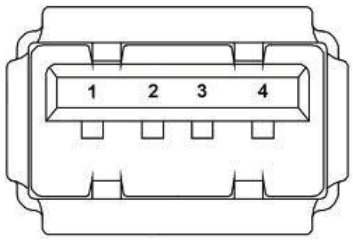


Table 4-11. USB Type A Port J2 Signal Descriptions

Pin	Mnemonic	Description
1	Vbus	5V power
2	DM	Data minus
3	DP	Data plus
4	GND	Common ground
5, 6	Shield	Mechanical pins

4.4.6 SD Card MCI

Figure 4-33. SD/MMC Socket J8

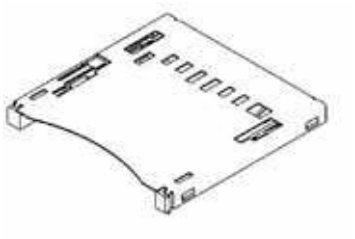


Table 4-12. SD Socket J8 Signal Descriptions

Pin	Function	PIO
1	MCI_DA3	PA20
2	MCI_CMD	PA16
3	GND	
4	VDDIOP0	
5	MCI_CLK	PA17
6	GND	
7	MCI_DA0	PA15
8	MCI_DA1	PA18
9	MCI_DA2	PA19
10	MCI_CD	PA7
11	WP	
12	GND	
13	GND	

4.4.7 Ethernet RJ45 Socket

Figure 4-34. Ethernet RJ45 Socket J16

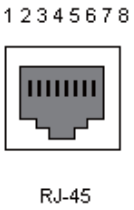


Table 4-13. RJ45 Socket J16 Signal Descriptions

Pin	Mnemonic	Description
1	TX+	Differential output plus
2	TX-	Differential output minus
3	RX+	Differential input plus
4	Reserved	
5	Reserved	
6	RX-	Differential input minus
7	Reserved	
8	Reserved	

4.4.8 Zigbee Socket J12

Figure 4-35. Zigbee Socket J12

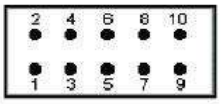


Table 4-14. Zigbee Socket J12 Signal Descriptions

Function	Signal Name	Port	Pin	Pin	Port	Signal Name	Function
Reset	/RST		1	2		IRQ0	Interrupt Request
Interrupt Request	IRQ1		3	4		SLP_TR	SLP_TR
SPI chip select	/CS		5	6		MOSI	SPI MOSI
SPI MISO	MISO		7	8		SCLK	SPI CLK
Power Supply	GND	GND	9	10	VCC	VCC	VCC

4.4.9 LCD Socket

Figure 4-36. LCD Socket J9

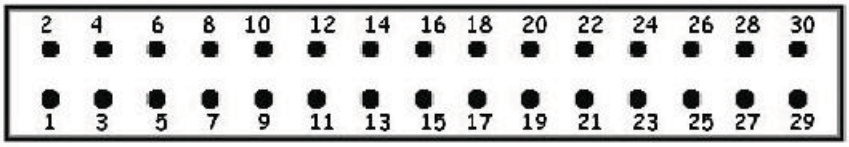


Table 4-15. LCD Socket J9 Signal Descriptions

LCD	ISI	Pin Num	Pin Num	ISI	LCD
3V3	3V3	1	2	GND	GND
VDDISI	VDDISI	3	4	GND	GND
ZB_IRQ0	ZB_IRQ0	5	6		ZB_IRQ1
TWCK0	TWCK0	7	8		TWD0
GND	GND	9	10	ISI_MCK	LCDDAT15
GND	GND	11	12	ISI_VSYNC	LCDDAT13
GND	GND	13	14	ISI_HSYNC	LCDDAT14
GND	GND	15	16	ISI_PCK	LCDDAT12
GND	GND	17	18	ISI_D0	LCDDAT0
LCDDAT1	ISI_D1	19	20	ISI_D2	LCDDAT2
LCDDAT3	ISI_D3	21	22	ISI_D4	LCDDAT4
LCDDAT5	ISI_D5	23	24	ISI_D6	LCDDAT6
LCDDAT7	ISI_D7	25	26	ISI_D8	LCDDAT8
LCDDAT9	ISI_D9	27	28	ISI_D10	LCDDAT10
LCDDAT11	ISI_D11	29	30	GND	GND

Figure 4-37. LCD Socket J10

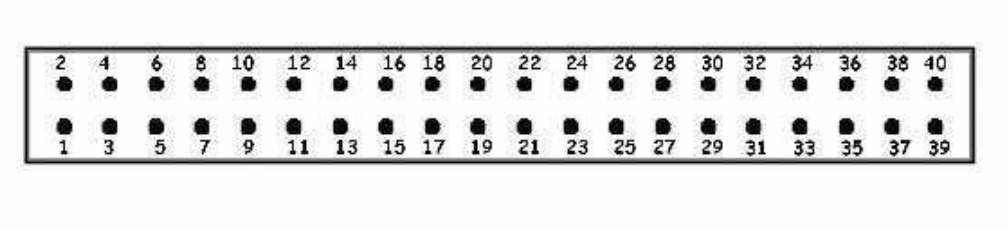


Table 4-16. LCD Socket J10 Signal Descriptions

LCD		Pin Num	Pin Num		LCD
5V	5V_INTER	1	2	GND	GND
5V	5V_INTER	3	4	GND	GND
LCDDAT16		5	6		LCDDAT17
LCDDAT18		7	8		LCDDAT19
LCDDAT20		9	10		LCDDAT21
LCDDAT22		11	12		LCDDAT23
GND	GND	13	14	GND	GND
LCDDISP		15	16		LCDPWM
LCDCSYNC		17	18		LCDHSYNC
LCDDEN		19	20		LCDPCK
GND	GND	21	22	GND	GND
AD0_XP	TSC	23	24	TSC	AD1_XM
AD2_YP	TSC	25	26	TSC	AD3_YM
AD4_LR	TSC	27	28		ONE_WIRE
GND	GND	29	30	GND	GND
SPI1_MISO		31	32		SPI1_MOSI
SPI1_SPCK		33	34		SPI1_NPCS1
EN_PWRLCD	SELCONFIG	35	36	LCD_DETECT	LCD_DETECT#
PD16		37	38		PD17
GND	GND	39	40	GND	GND

4.4.10 IO Expansion Port

Figure 4-38. IO Expansion Socket J5

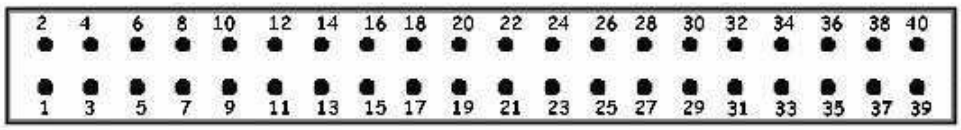


Table 4-17. IO Expansion Socket J5 Signal Descriptions

PIO	Power	Pin Num	Pin Num	Power	PIO
	3V3, or 5V	1	2	3V3, or 5V	
	GND	3	4	GND	
PA0		5	6		PA16
PA1		7	8		PA17
PA2		9	10		PA18
PA3		11	12		PA19
PA4		13	14		PA20
PA5		15	16		PA21
PA6		17	18		PA22
PA7		19	20		PA23
PA8		21	22		PA24
PA9		23	24		PA25
PA10		25	26		PA26
PA11		27	28		PA27
PA12		29	30		PA28
PA13		31	32		PA29
PA14		33	34		PA30
PA15		35	36		PA31
	GND	37	38	GND	
	3V3	39	40	3V3	

Figure 4-39. IO Expansion Socket J6

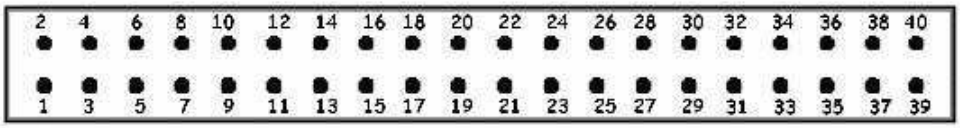


Table 4-18. IO Expansion Socket J6 Signal Descriptions

PIO	Power	Pin Num	Pin Num	Power	PIO
	3V3, or 5V	1	2	3V3, or 5V	
	GND	3	4	GND	
PB0		5	6		PB16
PB1		7	8		PB17
PB2		9	10		PB18
PB3		11	12		PD6
PB4		13	14		PD7
PB5		15	16		PD8
PB6		17	18		PD9
PB7		19	20		PD10
PB8		21	22		PD11
PB9		23	24		PD12
PB10		25	26		PD13
PB11		27	28		PD14
PB12		29	30		PD17
PB13		31	32		PD18
PB14		33	34		PD19
PB15		35	36		PD20
	GND	37	38		PD21
	3V3	39	40	3V3	

Figure 4-40. IO Expansion Socket J7

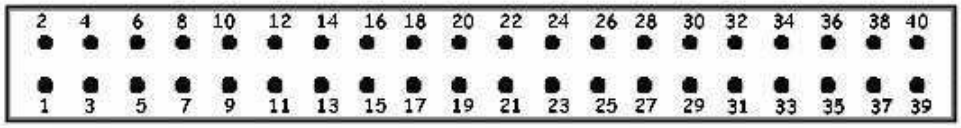


Table 4-19. IO Expansion Socket J7 Signal Descriptions

PIO	Power	Pin Num	Pin Num	Power	PIO
	3V3, or 5V	1	2	3V3, or 5V	
	GND	3	4	GND	
PC0		5	6		PC16
PC1		7	8		PC17
PC2		9	10		PC18
PC3		11	12		PC19
PC4		13	14		PC20
PC5		15	16		PC21
PC6		17	18		PC22
PC7		19	20		PC23
PC8		21	22		PC24
PC9		23	24		PC25
PC10		25	26		PC26
PC11		27	28		PC27
PC12		29	30		PC28
PC13		31	32		PC29
PC14		33	34		PC30
PC15		35	36		PC31
	GND	37	38	GND	
	3V3	39	40	3V3	

Section 5

EK Schematics

5.1 SAM9N12-EK Schematics

This section contains the following schematics:

- Top Level
- Power Supply
- AT91SAM9N12
- EBI Interface
- PIO Interfaces
- DDR2 NAND Flash
- Serial Interfaces
- Audio
- ETH

5 V
POWER SUPPLY
USER INTERFACE
Sheet 2,5,7

POWER
PIO
3V3
1V8
1V

USB
HOST
HOST DEVICE
HE 10
ICE INTERFACE
Sheet 3

PIO
PIO A,...E

RS232
DBGU
LCD INTERFACE
4.3"
480x272
TFT
TOUCH SCREEN
HE 14
ISI
CAMERA INTERFACE
HE 14
ZIGBEE INTERFACE
MMC SD
SDIO
CARD READER
Sheet 7

PIO

ATMEL
ARM9 Processor
SAM9N12 (LFBGA217)
Sheet 3,4,5

EBI DATA INTERFACE
EBI ADDRESS INTERFACE
EBI BUS INTERFACE
RES.ARRAYS
EBI ADAPTER
Sheet 4

EBI DDR2 INTERFACE
EBI FLASH INTERFACE
EBI NANDFLASH INTERFACE
EBI
DDR2 128MB
FLASH
NAND FLASH
Sheet 6

EBI ETH INTERFACE
EBI
10/100 FAST ETHERNET (RJ 45)
Sheet 9

PIO A,...D
MIC
LINEOUT
HPOUT
AUDIO
Sheet 8

HE 14
PIO CONNECTOR
1-WRIE EEPROM
TWI0
SERIAL EEPROM
SPI0
SERIAL DATA FLASH
Sheet 5

PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE	PIOD		PIOD	
PA0	TXD0	PA16	MCI_CDA	PB0	--	PB16	VBUS_SENSE	PC0	LCDDAT0	PC16	LCDDAT16	PD0	NANDOE	PD16	D26
PA1	RXD0	PA17	MCI_CK	PB1	--	PB17	AD6	PC1	LCDDAT1	PC17	LCDDAT17	PD1	NANDWE	PD17	D27
PA2	ZB_IRQ0	PA18	MCI_DA1	PB2	ROM CODE	PB18	ADTRG	PC2	LCDDAT2	PC18	LCDDAT18	PD2	NANDALE/A21	PD18	D28
PA3	ZB_IRQ1	PA19	MCI_DA2	PB3	PB_USER1			PC3	LCDDAT3	PC19	LCDDAT19	PD3	NANDCLE	PD19	NCS2
PA4	One Wire	PA20	MCI_DA3	PB4	USER_LED1			PC4	LCDDAT4	PC20	LCDDAT20	PD4	NANDCS	PD20	D30
PA5	ZB_RSTN	PA21	SPI1_MISO	PB5	USER_LED2			PC5	LCDDAT5	PC21	LCDDAT21	PD5	NWAIT	PD21	D31
PA6	ZB_SLPTR	PA22	SPI1_MOSI	PB6	PWR_LE			PC6	LCDDAT6	PC22	LCDDAT22	PD6	D16		
PA7	MCI card detect	PA23	SPI1_SPCK	PB7	EN5V_HOST			PC7	LCDDAT7	PC23	LCDDAT23	PD7	D17		
PA8	SPI1_NPCS0	PA24	TK	PB8	OVCUR_USB			PC8	LCDDAT8	PC24	LCDDISP	PD8	D18		
PA9	DRXD	PA25	TF	PB9	--			PC9	LCDDAT9	PC25	EN5V_LCD	PD9	D19		
PA10	DTXD	PA26	TD	PB10	PCK0			PC10	LCDDAT10	PC26	LCDPWM	PD10	D20		
PA11	SPI0_MISO	PA27	RD	PB11	AD0			PC11	LCDDAT11	PC27	LCDVSYNC	PD11	D21		
PA12	SPI0_MOSI	PA28	RK	PB12	AD1			PC12	LCDDAT12	PC28	LCDHSYNC	PD12	D22		
PA13	SPI0_SPCK	PA29	RF	PB13	AD2			PC13	LCDDAT13	PC29	LCDDEN	PD13	D23		
PA14	SPI0_NPCS0	PA30	TWD0	PB14	AD3			PC14	LCDDAT14	PC30	LCDPCK	PD14	D24		
PA15	MCI_DA0	PA31	TWCKO	PB15	AD4			PC15	LCDDAT15	PC31	OVCUR_LCD	PD15	A20		

NOTE

"DNP" means the component is not populated by default

REV	MODIF.	DES.	DATE	VER.	DATE
C	NOR_NRST		25-NOV-11	XXX	XX-XXX-XX
B	EBI		25-SEP-11	XXX	XX-XXX-XX
A	INIT EDIT		20-AUG-11	XXX	XX-XXX-XX

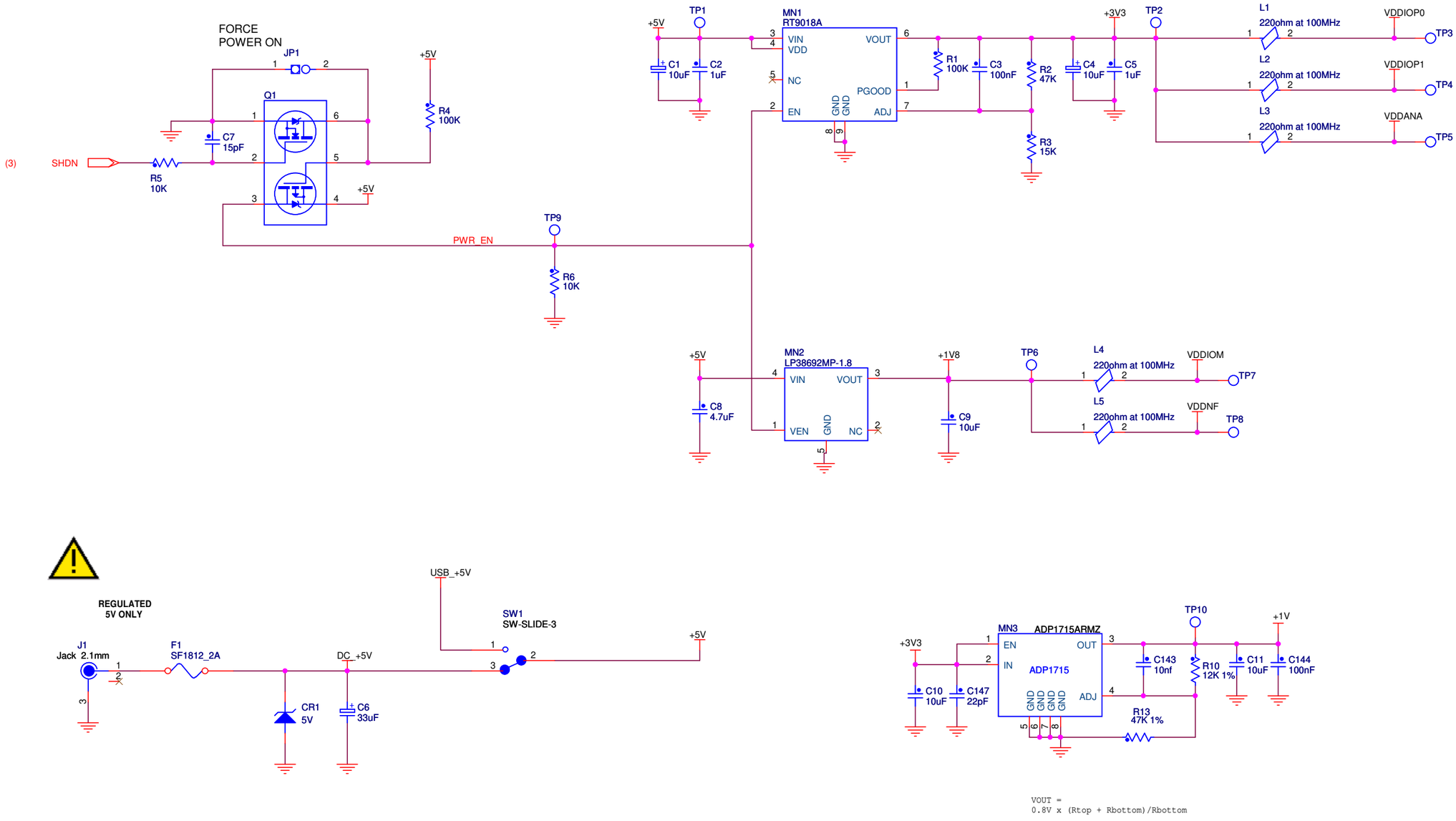
ATMEL ROUSSET

SAM9N12-EK_RevC
BGA217
TOP LEVEL

SCALE 1/1

REV. C

SHEET 1/9



REV	MODIF.	DES.	DATE	VER.	DATE
C	NOR NRST	PP	25-NOV-11	XXX	XX-XXX-XX
B	EBI	PP	25-SEPT-11	XXX	XX-XXX-XX
A	INIT EDIT	PP	20-AUG-11	XXX	XX-XXX-XX

ATMEL ROUSSET

SAM9N12-EK_RevC

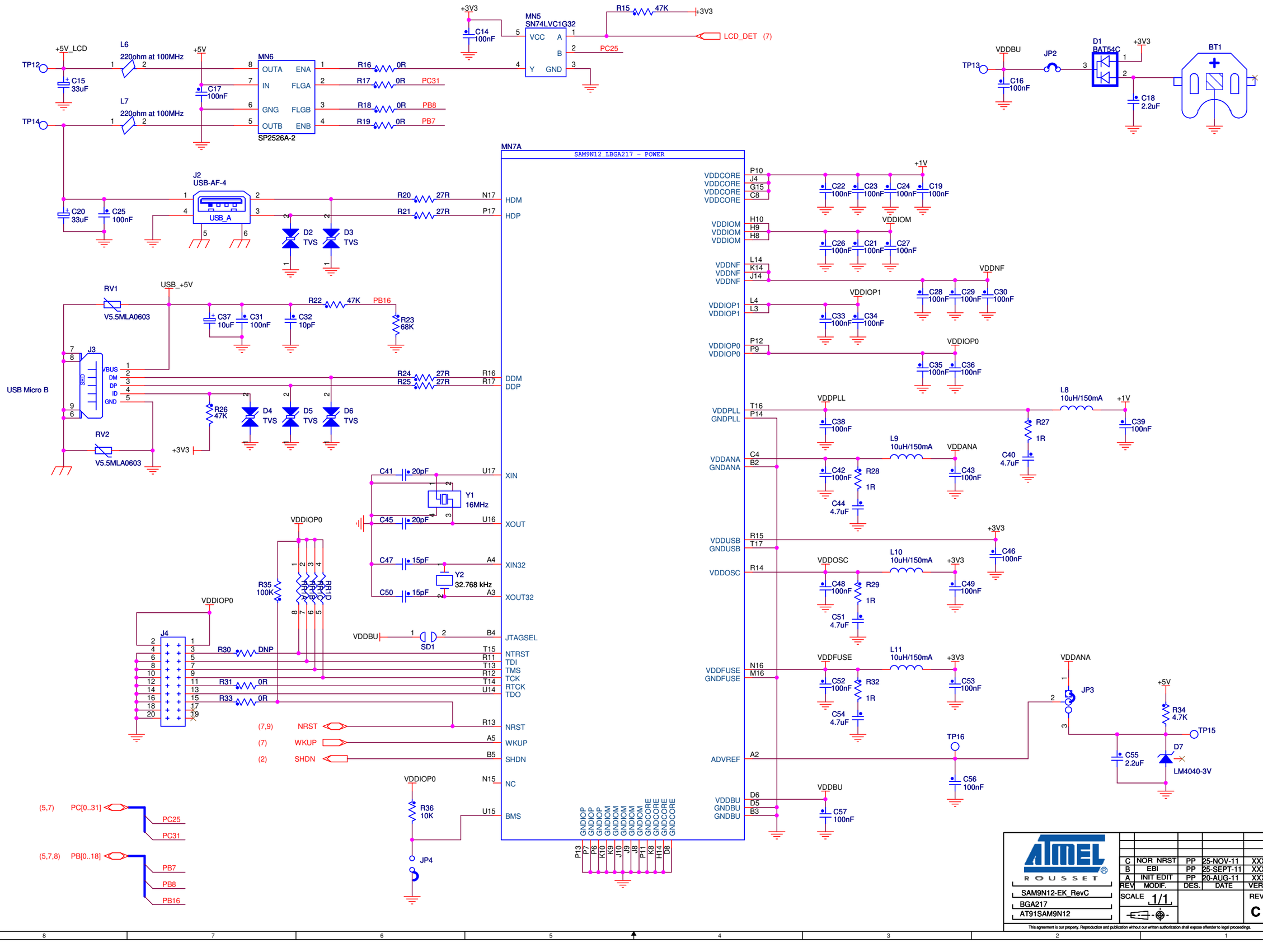
BGA217

POWER SUPPLY

SCALE 1/1

REV. C

SHEET 2/9


+5V_LCD
TP12
TP14
L6
220ohm at 100MHz
L7
220ohm at 100MHz
C15
33uF
C17
100nF
+5V
MN6
OUTA
ENA
IN
FLGA
GNG
FLGB
OUTB
ENB
SP2526A-2
R16 0R
R17 0R
R18 0R
R19 0R
PC31
PB8
PB7
+3V3
C14
100nF
MN5
SN74LVC1G32
VCC
A
B
Y
GND
R15 47K
PC25
LCD_DET (7)
VDDBU
TP13
JP2
D1
BAT54C
C16
100nF
C18
2.2uF
BT1
J2
USB-AF-4
USB_A
C20
33uF
C25
100nF
R20 27R
R21 27R
N17
P17
HDM
HDP
D2
TVS
D3
TVS
RV1
V5.5MLA0603
USB_+5V
R22 47K
PB16
C37
10uF
C31
100nF
C32
10pF
R23
68K
J3
USB Micro B
VBUS
DM
DP
ID
GND
SHD
R24 27R
R25 27R
R16
R17
DDM
DDP
D4
TVS
D5
TVS
D6
TVS
R26
47K
RV2
V5.5MLA0603
+3V3
C41 20pF
C45 20pF
Y1
16MHz
U17
U16
XIN
XOUT
C47 15pF
C50 15pF
Y2
32.768 kHz
A4
A3
XIN32
XOUT32
VDDIOP0
R35
100K
RP10
VDDIOP0
J4
R30 DNP
R31 0R
R33 0R
VDDBU
SD1
B4
T15
R11
T13
R12
T14
U14
JTAGSEL
NTRST
TDI
TMS
TCK
RTCK
TDO
(7,9) NRST
(7) WKUP
(2) SHDN
R13
A5
B5
NRST
WKUP
SHDN
VDDIOP0
R36
10K
JP4
N15
U15
NC
BMS
(5,7) PC[0..31]
PC25
PC31
(5,7,8) PB[0..18]
PB7
PB8
PB16
MN7A
SAM9N12_LBGA217 - POWER
VDDCORE
VDDCORE
VDDCORE
VDDCORE
P10
J4
G15
C8
+1V
C22 100nF
C23 100nF
C24 100nF
C19 100nF
VDDIOM
VDDIOM
VDDIOM
H10
H9
H8
VDDIOM
C26 100nF
C21 100nF
C27 100nF
VDDNF
VDDNF
VDDNF
L14
K14
J14
VDDNF
C28 100nF
C29 100nF
C30 100nF
VDDIOP1
VDDIOP1
L4
L3
VDDIOP1
C33 100nF
C34 100nF
VDDIOP0
VDDIOP0
P12
P9
VDDIOP0
C35 100nF
C36 100nF
VDDPLL
GNDPLL
T16
P14
VDDPLL
C38 100nF
L8
10uH/150mA
+1V
C39 100nF
R27
1R
C40
4.7uF
VDDANA
GNDANA
C4
B2
L9
10uH/150mA
VDDANA
C42 100nF
R28
1R
C44
4.7uF
C43 100nF
VDDUSB
GNDUSB
R15
T17
+3V3
C46 100nF
VDDOSC
R14
VDDOSC
L10
10uH/150mA
+3V3
C48 100nF
R29
1R
C51
4.7uF
C49 100nF
VDDFUSE
GNDFUSE
N16
M16
VDDFUSE
L11
10uH/150mA
+3V3
C52 100nF
R32
1R
C54
4.7uF
C53 100nF
ADVREF
A2
TP16
C56 100nF
VDDBU
GNDBU
GNDBU
D6
D5
B3
VDDBU
C57 100nF
VDDANA
JP3
+5V
R34
4.7K
TP15
C55
2.2uF
D7
LM4040-3V
GNDIOP
GNDIOP
GNDIOM
GNDIOM
GNDIOM
GNDIOM
GNDIOM
GNDCORE
GNDCORE
GNDCORE
GNDCORE
P13
P7
P6
K10
K9
J10
J9
J8
P11
K8
H14
D8
ATMEL
ROUSSET
SAM9N12-EK_RevC
BGA217
AT91SAM9N12
C NOR NRST PP 25-NOV-11 XXX XX-XXX-XX
B EBI PP 25-SEPT-11 XXX XX-XXX-XX
A INIT EDIT PP 20-AUG-11 XXX XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. C
SHEET 3/9
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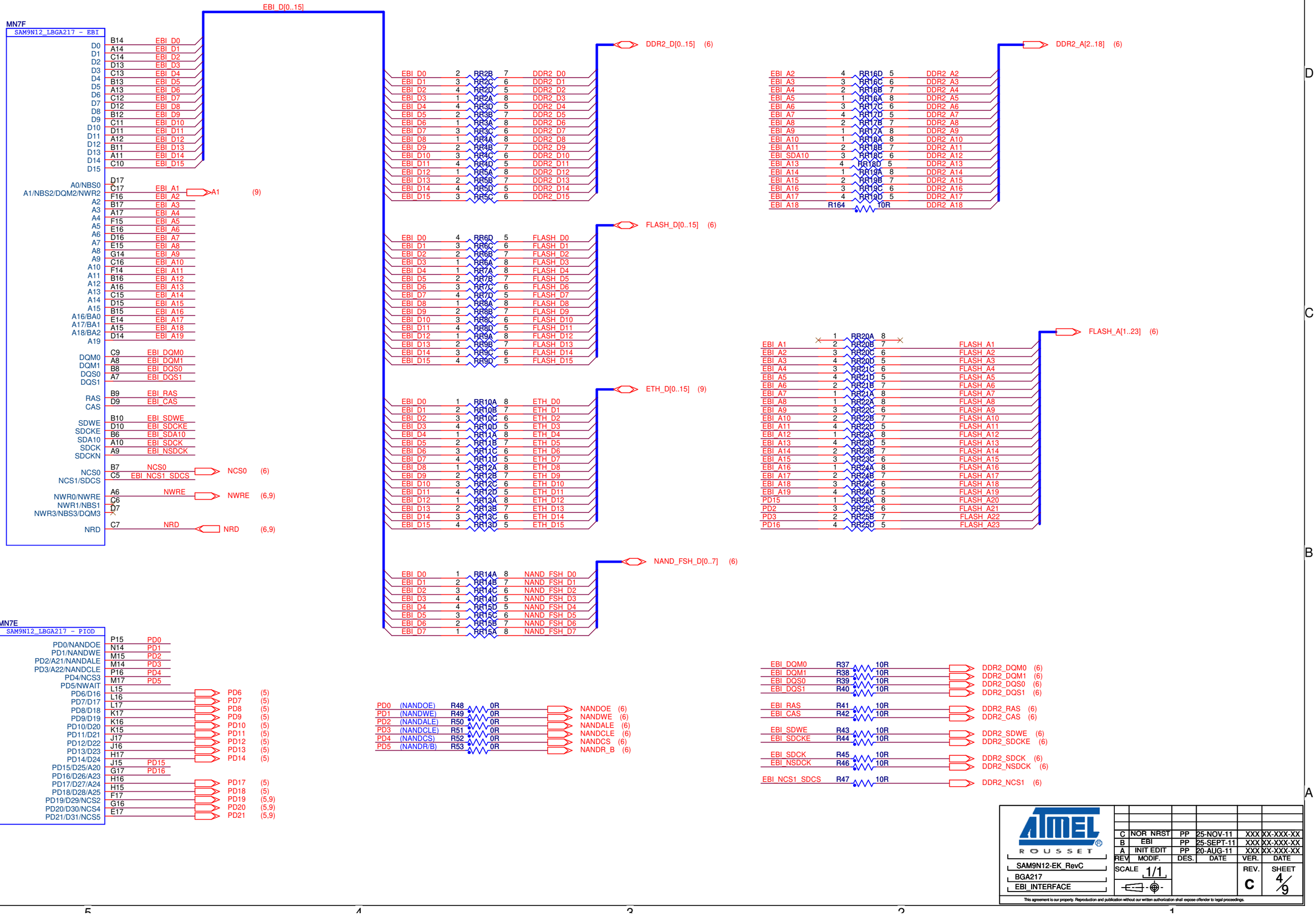
MN7F
SAM9N12_LBGA217 - EBI
EBI_D[0..15]
D0 B14 EBI_D0
D1 A14 EBI_D1
D2 C14 EBI_D2
D3 D13 EBI_D3
D4 C13 EBI_D4
D5 B13 EBI_D5
D6 A13 EBI_D6
D7 C12 EBI_D7
D8 D12 EBI_D8
D9 B12 EBI_D9
D10 C11 EBI_D10
D11 D11 EBI_D11
D12 A12 EBI_D12
D13 B11 EBI_D13
D14 A11 EBI_D14
D15 C10 EBI_D15
D17
A0/NBS0 C17 EBI_A1 A1 (9)
A1/NBS2/DQM2/NWR2 F16 EBI_A2
A2 B17 EBI_A3
A3 A17 EBI_A4
A4 F15 EBI_A5
A5 E16 EBI_A6
A6 D16 EBI_A7
A7 E15 EBI_A8
A8 G14 EBI_A9
A9 C16 EBI_A10
A10 F14 EBI_A11
A11 B16 EBI_A12
A12 A16 EBI_A13
A13 C15 EBI_A14
A14 D15 EBI_A15
A15 B15 EBI_A16
A16/BA0 E14 EBI_A17
A17/BA1 A15 EBI_A18
A18/BA2 D14 EBI_A19
A19
DQM0 C9 EBI_DQM0
DQM1 A8 EBI_DQM1
DQS0 B8 EBI_DQS0
DQS1 A7 EBI_DQS1
RAS B9 EBI_RAS
CAS D9 EBI_CAS
SDWE B10 EBI_SDWE
SDCKE D10 EBI_SDCKE
SDA10 B6 EBI_SDA10
SDCK A10 EBI_SDCK
SDCKN A9 EBI_NSDCK
NCS0 B7 NCS0 NCS0 (6)
NCS1/SDCS C5 EBI_NCS1_SDCS
NWR0/NWRE A6 NWRE NWRE (6,9)
NWR1/NBS1 C6
NWR3/NBS3/DQM3 D7
NRD C7 NRD NRD (6,9)
MN7E
SAM9N12_LBGA217 - PIOD
PD0/NANDOE P15 PD0
PD1/NANDWE N14 PD1
PD2/A21/NANDALE M15 PD2
PD3/A22/NANDCLE M14 PD3
PD4/NCS3 P16 PD4
PD5/NWAIT M17 PD5
PD6/D16 L15 PD6 (5)
PD7/D17 L16 PD7 (5)
PD8/D18 L17 PD8 (5)
PD9/D19 K17 PD9 (5)
PD10/D20 K16 PD10 (5)
PD11/D21 K15 PD11 (5)
PD12/D22 J17 PD12 (5)
PD13/D23 J16 PD13 (5)
PD14/D24 H17 PD14 (5)
PD15/D25/A20 J15 PD15
PD16/D26/A23 G17 PD16
PD17/D27/A24 H16 PD17 (5)
PD18/D28/A25 H15 PD18 (5)
PD19/D29/NCS2 F17 PD19 (5,9)
PD20/D30/NCS4 G16 PD20 (5,9)
PD21/D31/NCS5 E17 PD21 (5,9)
DDR2_D[0..15] (6)
EBI_D0 2 RR2B 7 DDR2_D0
EBI_D1 3 RR2C 6 DDR2_D1
EBI_D2 4 RR2D 5 DDR2_D2
EBI_D3 1 RR2A 8 DDR2_D3
EBI_D4 4 RR3D 5 DDR2_D4
EBI_D5 2 RR3B 7 DDR2_D5
EBI_D6 1 RR3A 8 DDR2_D6
EBI_D7 3 RR3C 6 DDR2_D7
EBI_D8 1 RR4A 8 DDR2_D8
EBI_D9 2 RR4B 7 DDR2_D9
EBI_D10 3 RR4C 6 DDR2_D10
EBI_D11 4 RR4D 5 DDR2_D11
EBI_D12 1 RR5A 8 DDR2_D12
EBI_D13 2 RR5B 7 DDR2_D13
EBI_D14 4 RR5D 5 DDR2_D14
EBI_D15 3 RR5C 6 DDR2_D15
FLASH_D[0..15] (6)
EBI_D0 4 RR6D 5 FLASH_D0
EBI_D1 3 RR6C 6 FLASH_D1
EBI_D2 2 RR6B 7 FLASH_D2
EBI_D3 1 RR6A 8 FLASH_D3
EBI_D4 1 RR7A 8 FLASH_D4
EBI_D5 2 RR7B 7 FLASH_D5
EBI_D6 3 RR7C 6 FLASH_D6
EBI_D7 4 RR7D 5 FLASH_D7
EBI_D8 1 RR8A 8 FLASH_D8
EBI_D9 2 RR8B 7 FLASH_D9
EBI_D10 3 RR8C 6 FLASH_D10
EBI_D11 4 RR8D 5 FLASH_D11
EBI_D12 1 RR9A 8 FLASH_D12
EBI_D13 2 RR9B 7 FLASH_D13
EBI_D14 3 RR9C 6 FLASH_D14
EBI_D15 4 RR9D 5 FLASH_D15
ETH_D[0..15] (9)
EBI_D0 1 RR10A 8 ETH_D0
EBI_D1 2 RR10B 7 ETH_D1
EBI_D2 3 RR10C 6 ETH_D2
EBI_D3 4 RR10D 5 ETH_D3
EBI_D4 1 RR11A 8 ETH_D4
EBI_D5 2 RR11B 7 ETH_D5
EBI_D6 3 RR11C 6 ETH_D6
EBI_D7 4 RR11D 5 ETH_D7
EBI_D8 1 RR12A 8 ETH_D8
EBI_D9 2 RR12B 7 ETH_D9
EBI_D10 3 RR12C 6 ETH_D10
EBI_D11 4 RR12D 5 ETH_D11
EBI_D12 1 RR13A 8 ETH_D12
EBI_D13 2 RR13B 7 ETH_D13
EBI_D14 3 RR13C 6 ETH_D14
EBI_D15 4 RR13D 5 ETH_D15
NAND_FSH_D[0..7] (6)
EBI_D0 1 RR14A 8 NAND_FSH_D0
EBI_D1 2 RR14B 7 NAND_FSH_D1
EBI_D2 3 RR14C 6 NAND_FSH_D2
EBI_D3 4 RR14D 5 NAND_FSH_D3
EBI_D4 4 RR15D 5 NAND_FSH_D4
EBI_D5 3 RR15C 6 NAND_FSH_D5
EBI_D6 2 RR15B 7 NAND_FSH_D6
EBI_D7 1 RR15A 8 NAND_FSH_D7
PD0 (NANDOE) R48 0R NANDOE (6)
PD1 (NANDWE) R49 0R NANDWE (6)
PD2 (NANDALE) R50 0R NANDALE (6)
PD3 (NANDCLE) R51 0R NANDCLE (6)
PD4 (NANDCS) R52 0R NANDCS (6)
PD5 (NANDR/B) R53 0R NANDR_B (6)
DDR2_A[2..18] (6)
EBI_A2 4 RR16D 5 DDR2_A2
EBI_A3 3 RR16C 6 DDR2_A3
EBI_A4 2 RR16B 7 DDR2_A4
EBI_A5 1 RR16A 8 DDR2_A5
EBI_A6 3 RR17C 6 DDR2_A6
EBI_A7 4 RR17D 5 DDR2_A7
EBI_A8 2 RR17B 7 DDR2_A8
EBI_A9 1 RR17A 8 DDR2_A9
EBI_A10 1 RR18A 8 DDR2_A10
EBI_A11 2 RR18B 7 DDR2_A11
EBI_SDA10 3 RR18C 6 DDR2_A12
EBI_A13 4 RR18D 5 DDR2_A13
EBI_A14 1 RR19A 8 DDR2_A14
EBI_A15 2 RR19B 7 DDR2_A15
EBI_A16 3 RR19C 6 DDR2_A16
EBI_A17 4 RR19D 5 DDR2_A17
EBI_A18 R164 10R DDR2_A18
FLASH_A[1..23] (6)
1 RR20A 8
EBI_A1 2 RR20B 7 FLASH_A1
EBI_A2 3 RR20C 6 FLASH_A2
EBI_A3 4 RR20D 5 FLASH_A3
EBI_A4 3 RR21C 6 FLASH_A4
EBI_A5 4 RR21D 5 FLASH_A5
EBI_A6 2 RR21B 7 FLASH_A6
EBI_A7 1 RR21A 8 FLASH_A7
EBI_A8 1 RR22A 8 FLASH_A8
EBI_A9 3 RR22C 6 FLASH_A9
EBI_A10 2 RR22B 7 FLASH_A10
EBI_A11 4 RR22D 5 FLASH_A11
EBI_A12 1 RR23A 8 FLASH_A12
EBI_A13 4 RR23D 5 FLASH_A13
EBI_A14 2 RR23B 7 FLASH_A14
EBI_A15 3 RR23C 6 FLASH_A15
EBI_A16 1 RR24A 8 FLASH_A16
EBI_A17 2 RR24B 7 FLASH_A17
EBI_A18 3 RR24C 6 FLASH_A18
EBI_A19 4 RR24D 5 FLASH_A19
PD15 1 RR25A 8 FLASH_A20
PD2 3 RR25C 6 FLASH_A21
PD3 2 RR25B 7 FLASH_A22
PD16 4 RR25D 5 FLASH_A23
EBI_DQM0 R37 10R DDR2_DQM0 (6)
EBI_DQM1 R38 10R DDR2_DQM1 (6)
EBI_DQS0 R39 10R DDR2_DQS0 (6)
EBI_DQS1 R40 10R DDR2_DQS1 (6)
EBI_RAS R41 10R DDR2_RAS (6)
EBI_CAS R42 10R DDR2_CAS (6)
EBI_SDWE R43 10R DDR2_SDWE (6)
EBI_SDCKE R44 10R DDR2_SDCKE (6)
EBI_SDCK R45 10R DDR2_SDCK (6)
EBI_NSDCK R46 10R DDR2_NSDCK (6)
EBI_NCS1_SDCS R47 10R DDR2_NCS1 (6)
ATMEL
ROUSSET
SAM9N12-EK_RevC
BGA217
EBI_INTERFACE
C NOR_NRST PP 25-NOV-11 XXX XX-XXX-XX
B EBI PP 25-SEPT-11 XXX XX-XXX-XX
A INIT EDIT PP 20-AUG-11 XXX XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. C
SHEET 4/9
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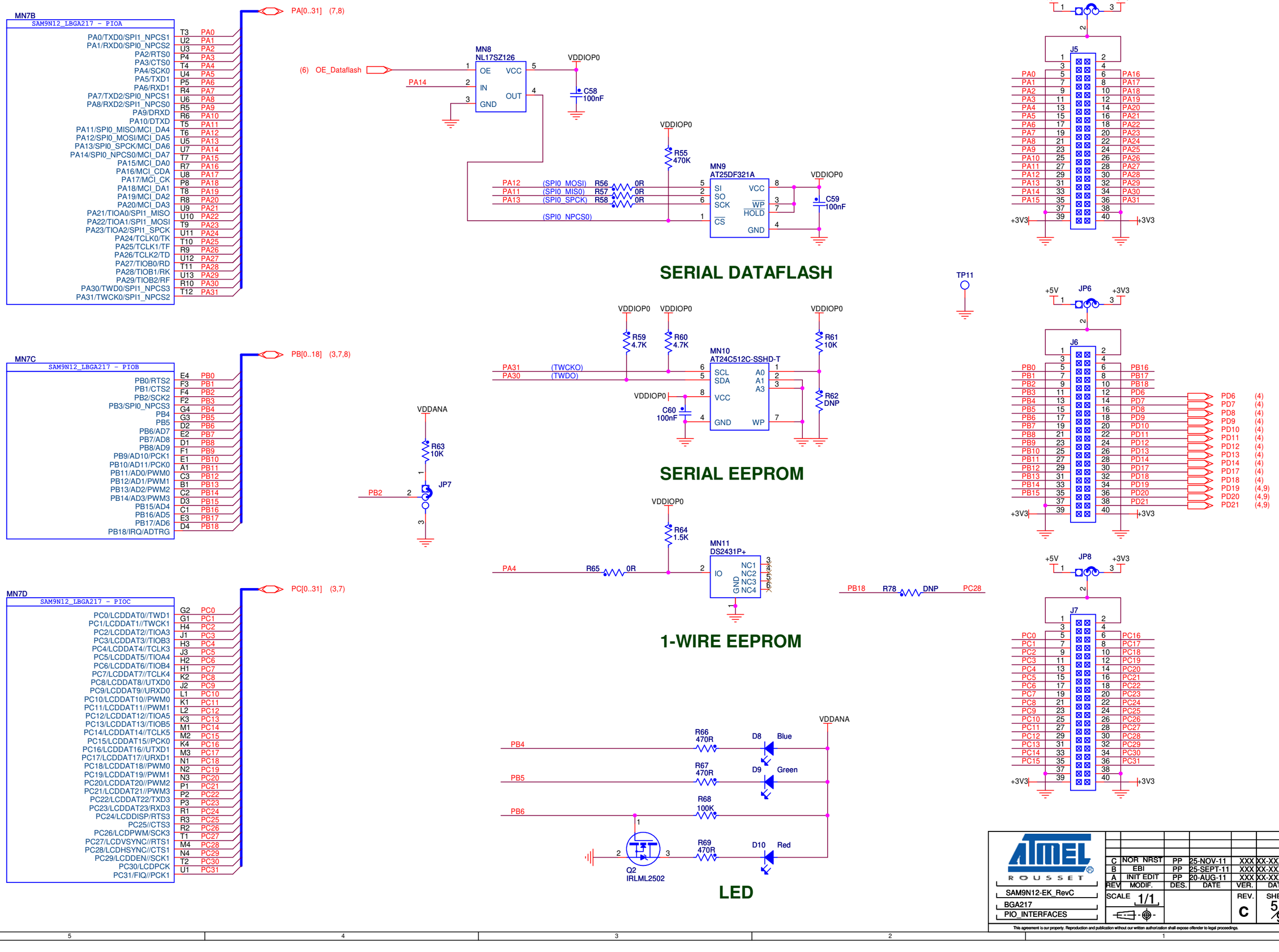
MN7B
SAM9N12_LBGA217 - PIOA
PA[0..31] (7,8)
MN8
NL17SZ126
(6) OE_Dataflash
PA14
VDDIOP0
C58
100nF
R55
470K
MN9
AT25DF321A
PA12 (SPI0_MOSI) R56 0R
PA11 (SPI0_MISO) R57 0R
PA13 (SPI0_SPCK) R58 0R
(SPI0_NPCS0)
C59
100nF
SERIAL DATAFLASH
JP5
J5
TP11
MN7C
SAM9N12_LBGA217 - PIOB
PB[0..18] (3,7,8)
VDDANA
R63
10K
JP7
PB2
R59
4.7K
R60
4.7K
R61
10K
R62
DNP
MN10
AT24C512C-SSHD-T
PA31 (TWCKO)
PA30 (TWDO)
C60
100nF
SERIAL EEPROM
JP6
J6
R64
1.5K
MN11
DS2431P+
PA4
R65 0R
1-WIRE EEPROM
MN7D
SAM9N12_LBGA217 - PIOC
PC[0..31] (3,7)
PB18 R78 DNP PC28
JP8
J7
R66
470R
D8 Blue
R67
470R
D9 Green
R68
100K
R69
470R
D10 Red
PB4
PB5
PB6
Q2
IRLML2502
LED
ATMEL
ROUSSET
SAM9N12-EK_RevC
BGA217
PIO_INTERFACES
SCALE 1/1
REV. C
SHEET 5/9
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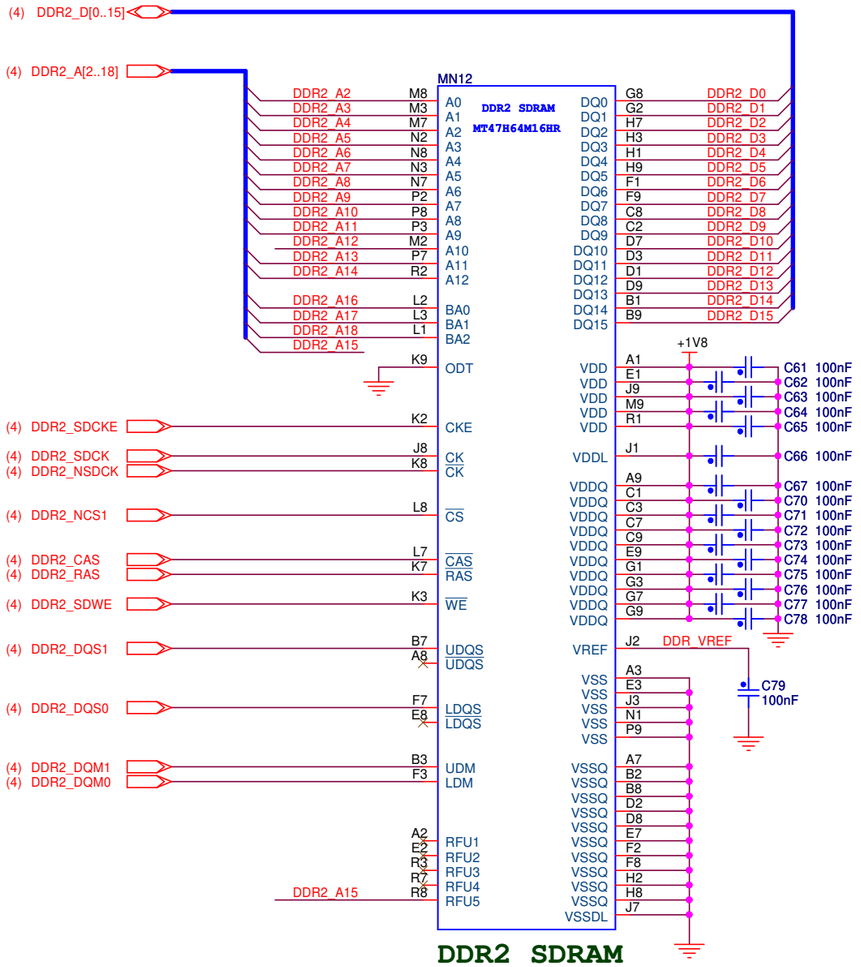

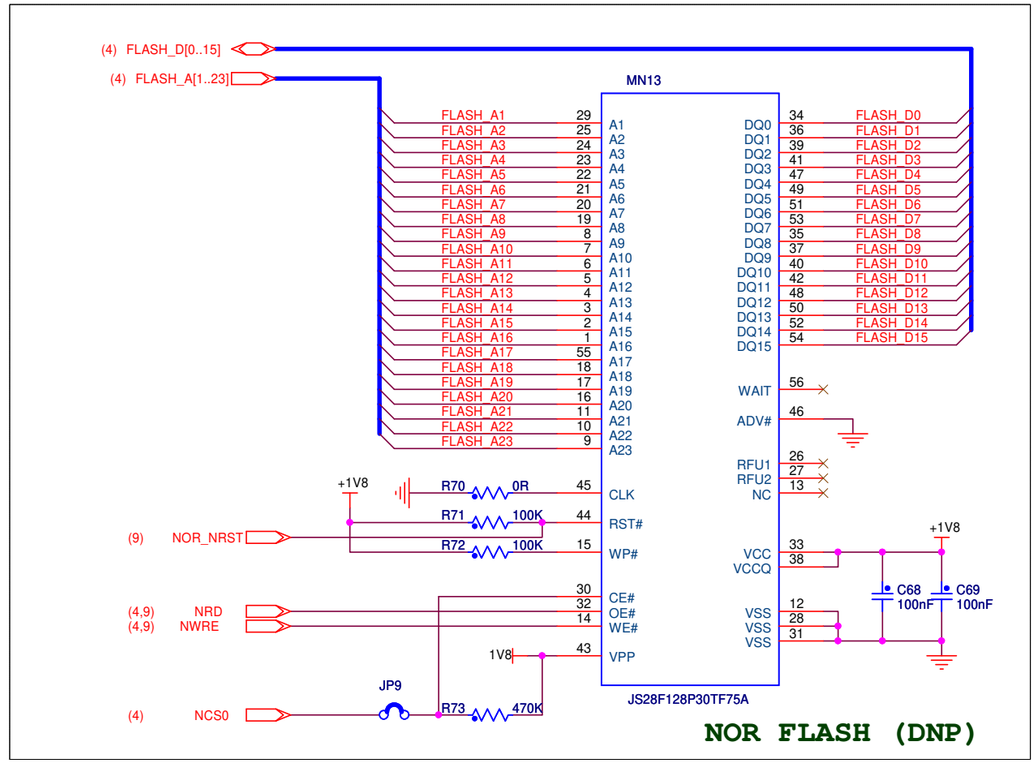

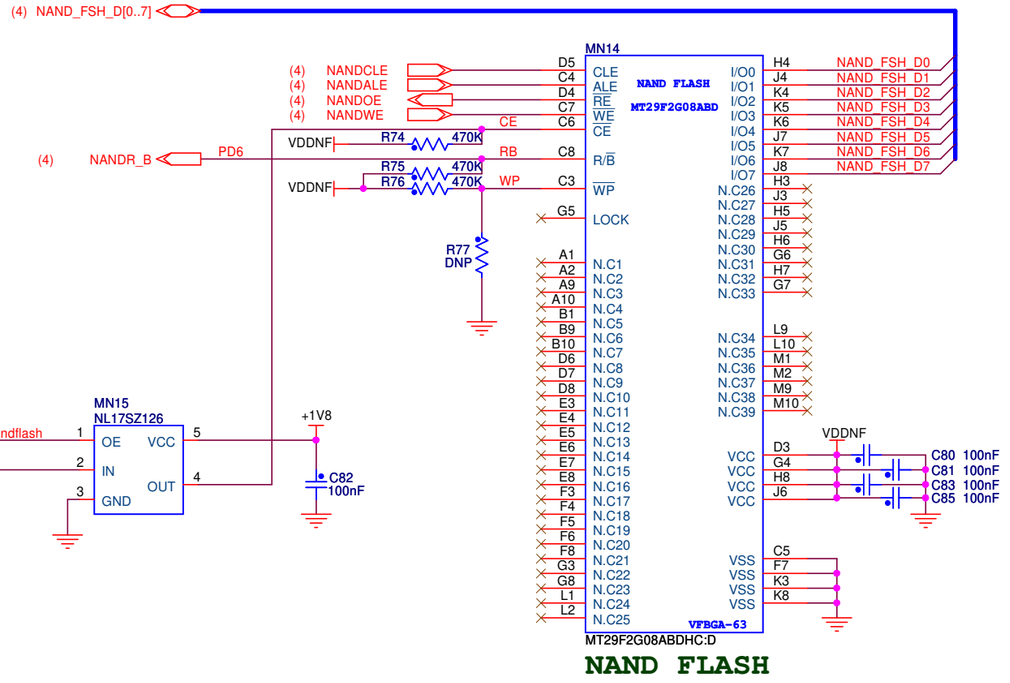

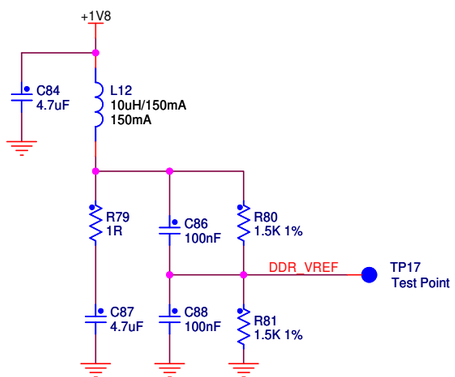

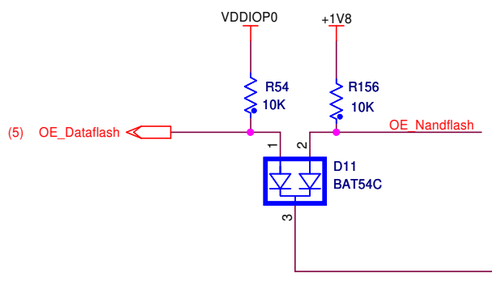

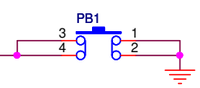

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B	EBI	PP	25-SEPT-11	XXX	XX-XXX-XX
A	INIT EDIT	PP	20-AUG-11	XXX	XX-XXX-XX
REV	MODIF.	DES.	DATE	VER.	DATE

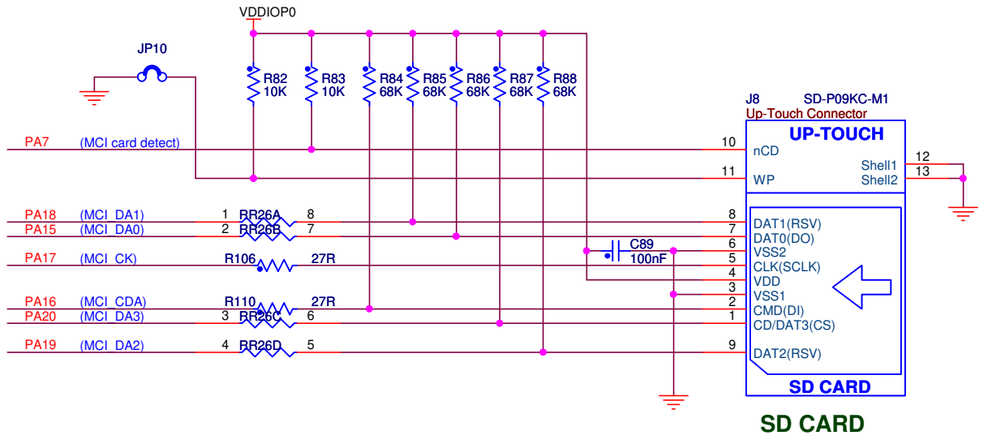
ATMEL ROUSSET

SAM9N12-EK_RevC
BGA217
DDR2 NAND FLASH

SCALE 1/1

REV. C

SHEET 6/9



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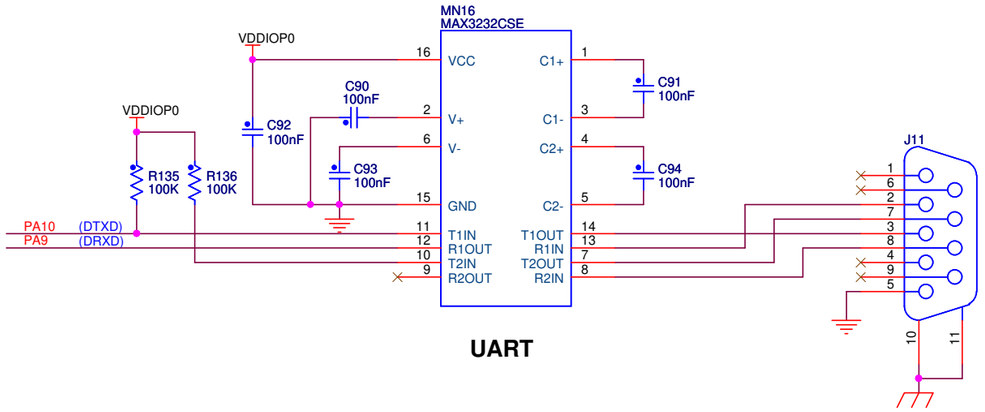

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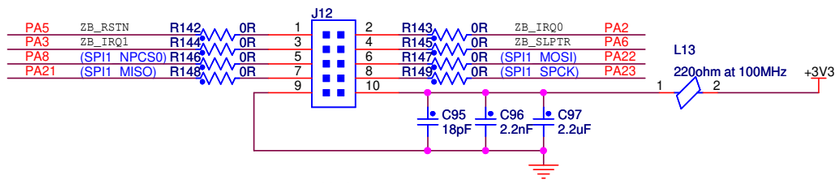
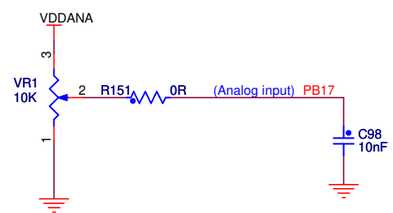
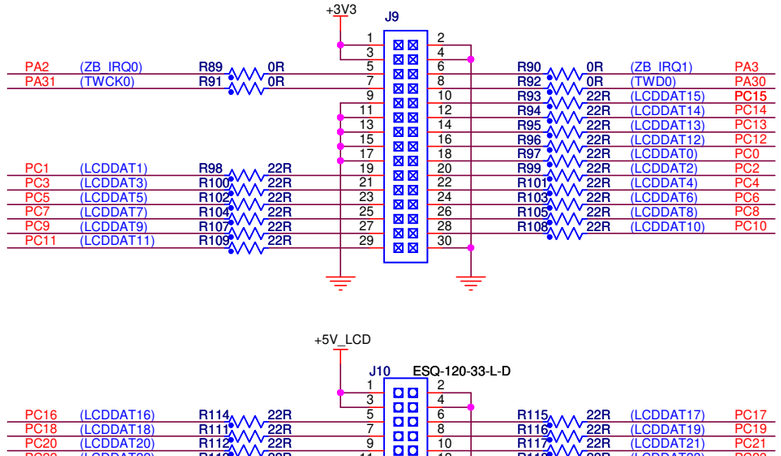
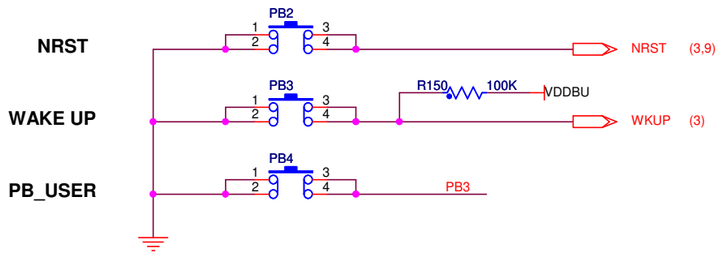
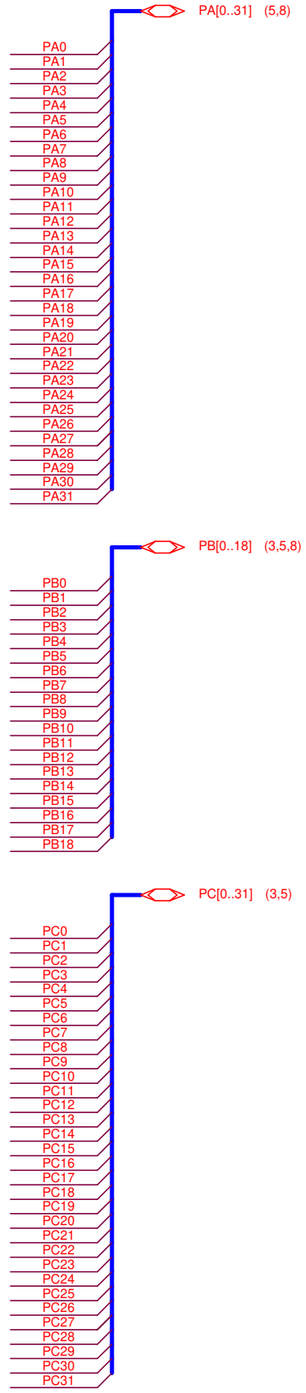


ZIGBEE









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B	EBI	PP	25-SEPT-11	XXX	XX-XXX-XX
A	INIT EDIT	PP	20-AUG-11	XXX	XX-XXX-XX

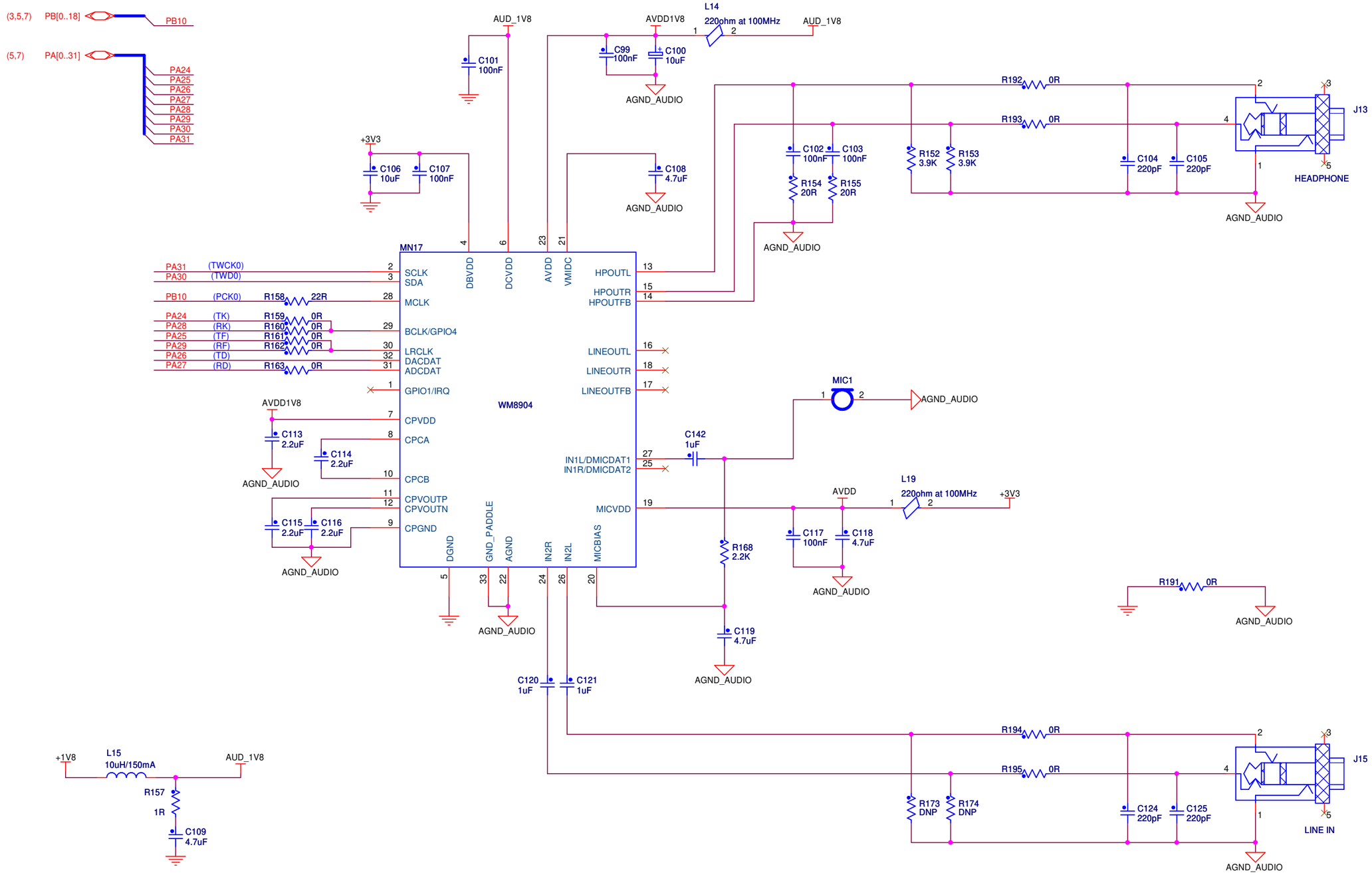
ATMEL ROUSSET

SAM9N12-EK_RevC
BGA217
SERIAL INTERFACES

SCALE 1/1

REV. C

SHEET 7/9



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B	EBI	PP	25-SEPT-11	XXX	XX-XXX-XX
A	INIT EDIT	PP	20-AUG-11	XXX	XX-XXX-XX

ATMEL ROUSSET

SAM9N12-EK_RevC

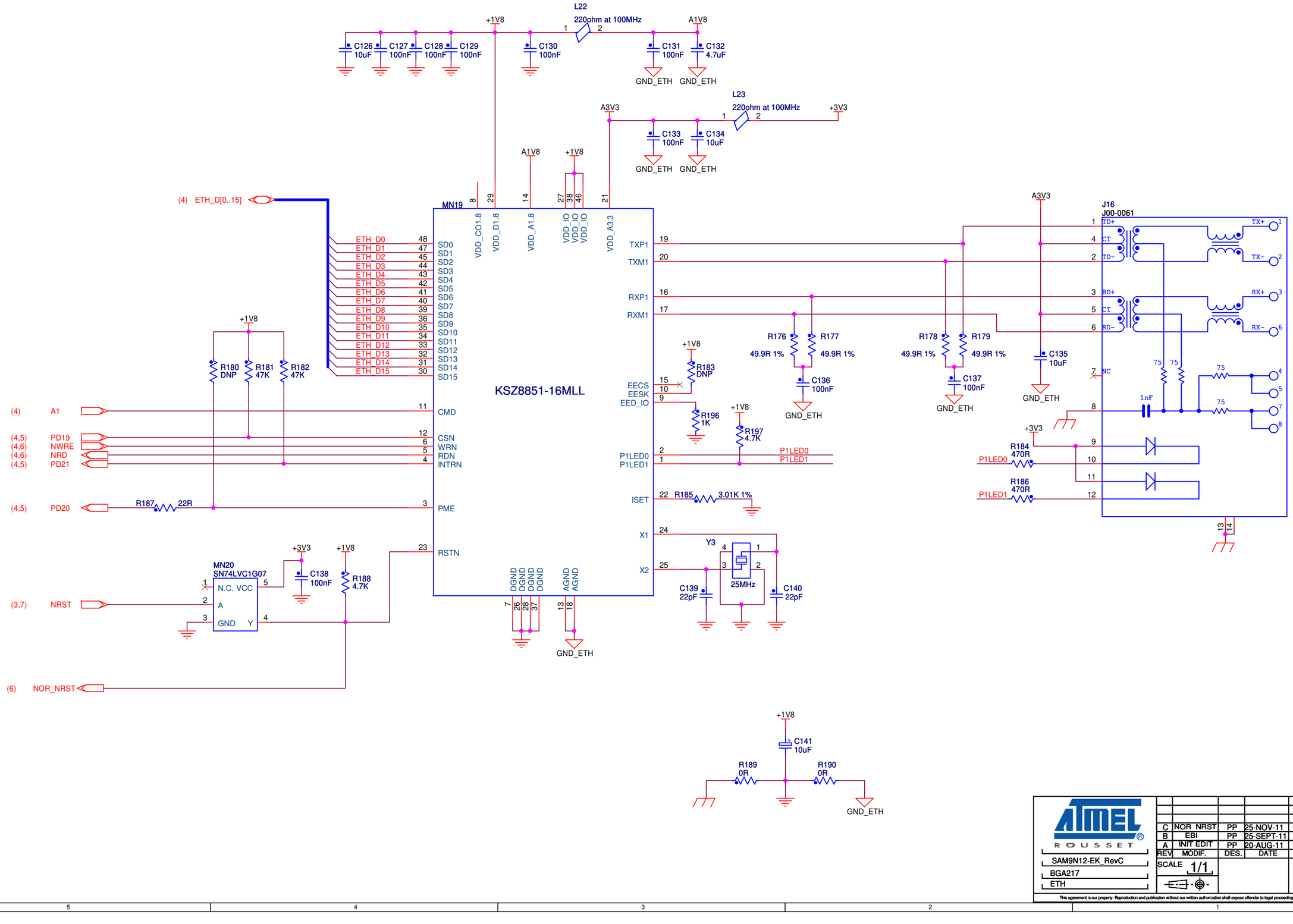
BGA217

AUDIO

SCALE 1/1

REV. C

SHEET 8/9



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B	EBI	PP	25-SEPT-11	XXX	XX-XXX-XX
A	INIT EDIT	PP	20-AUG-11	XXX	XX-XXX-XX
REV	MODIF.	DES.	DATE	VER.	DATE

SAM9N12-EK_RevC
BGA217
ETH

SCALE 1/1

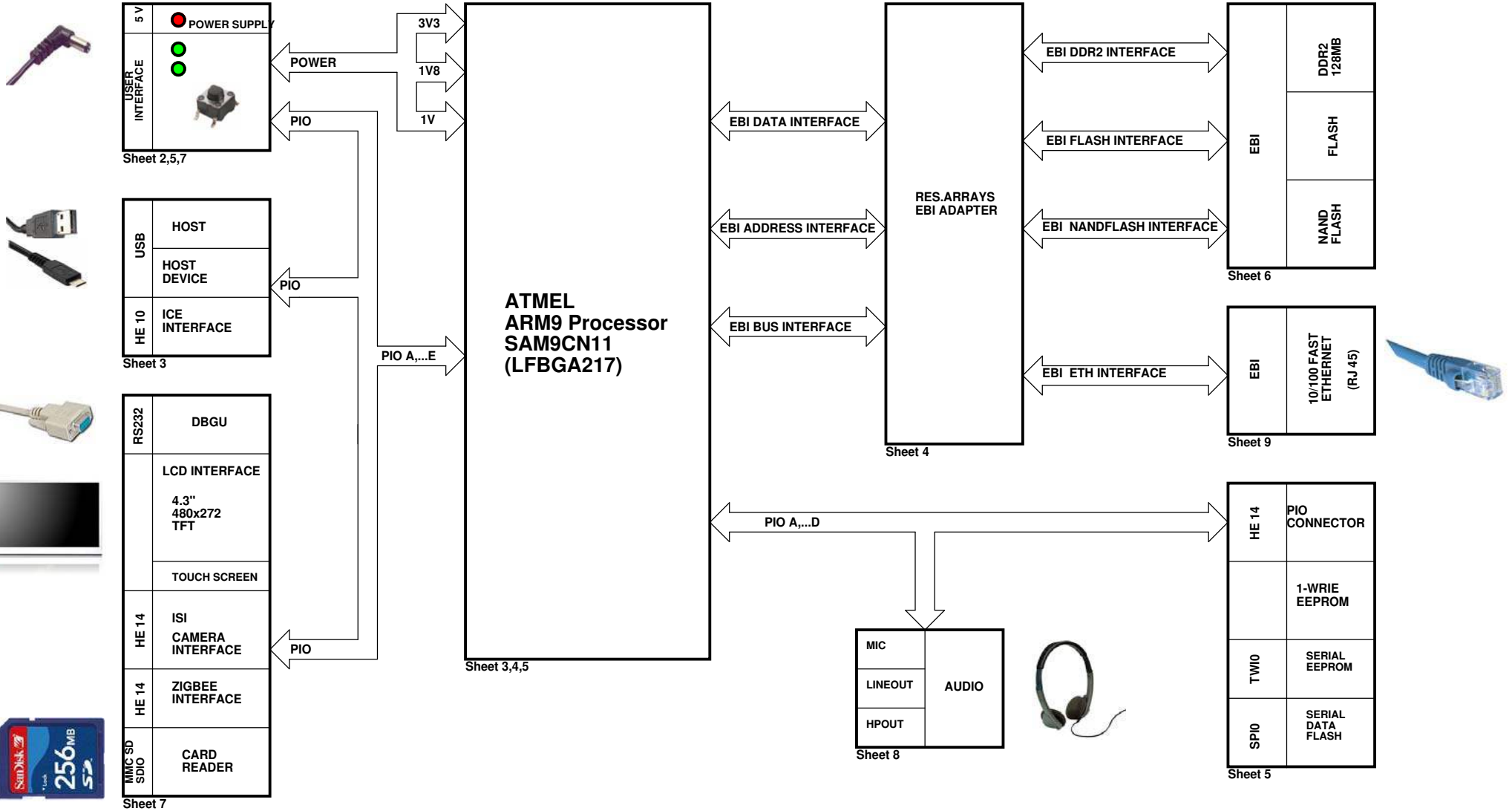
REV. C

SHEET 9/9

5.2 SAM9CN11-EK Schematics

This section contains the following schematics:

- Block Diagram
- Power Supply
- AT91SAM9CN11
- EBI Interface
- PIO Interfaces
- DDR2 NAND Flash
- Serial Interfaces
- Audio
- ETH



PIO MUXING															
PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE	PIOD		PIOD	
PA0	TXD0	PA16	MCI_CDA	PB0	--	PB16	VBUS_SENSE	PC0	LCDDAT0	PC16	LCDDAT16	PD0	NANDOE	PD16	D26
PA1	RXD0	PA17	MCI_CK	PB1	--	PB17	AD6	PC1	LCDDAT1	PC17	LCDDAT17	PD1	NANDWE	PD17	D27
PA2	ZB_IRQ0	PA18	MCI_DA1	PB2	ROM CODE	PB18	ADTRG	PC2	LCDDAT2	PC18	LCDDAT18	PD2	NANDALE/A21	PD18	D28
PA3	ZB_IRQ1	PA19	MCI_DA2	PB3	PB_USER1			PC3	LCDDAT3	PC19	LCDDAT19	PD3	NANDCLE	PD19	NCS2
PA4	One Wire	PA20	MCI_DA3	PB4	USER_LED1			PC4	LCDDAT4	PC20	LCDDAT20	PD4	NANDCS	PD20	D30
PA5	ZB_RSTN	PA21	SPI1_MISO	PB5	USER_LED2			PC5	LCDDAT5	PC21	LCDDAT21	PD5	NWAIT	PD21	D31
PA6	ZB_SLPTR	PA22	SPI1_MOSI	PB6	PWR_LE			PC6	LCDDAT6	PC22	LCDDAT22	PD6	D16		
PA7	MCI card detect	PA23	SPI1_SPCK	PB7	EN5V_HOST			PC7	LCDDAT7	PC23	LCDDAT23	PD7	D17		
PA8	SPI1_NPCS0	PA24	TK	PB8	OVCUR_USB			PC8	LCDDAT8	PC24	LCDDISP	PD8	D18		
PA9	DRXD	PA25	TF	PB9	--			PC9	LCDDAT9	PC25	EN5V_LCD	PD9	D19		
PA10	DTXD	PA26	TD	PB10	PCK0			PC10	LCDDAT10	PC26	LCDPWM	PD10	D20		
PA11	SPI0_MISO	PA27	RD	PB11	AD0			PC11	LCDDAT11	PC27	LCDVSYNC	PD11	D21		
PA12	SPI0_MOSI	PA28	RK	PB12	AD1			PC12	LCDDAT12	PC28	LCDHSYNC	PD12	D22		
PA13	SPI0_SPCK	PA29	RF	PB13	AD2			PC13	LCDDAT13	PC29	LCDDEN	PD13	D23		
PA14	SPI0_NPCS0	PA30	TWD0	PB14	AD3			PC14	LCDDAT14	PC30	LCDPCK	PD14	D24		
PA15	MCI_DA0	PA31	TWCKO	PB15	AD4			PC15	LCDDAT15	PC31	OVCUR_LCD	PD15	A20		

NOTE

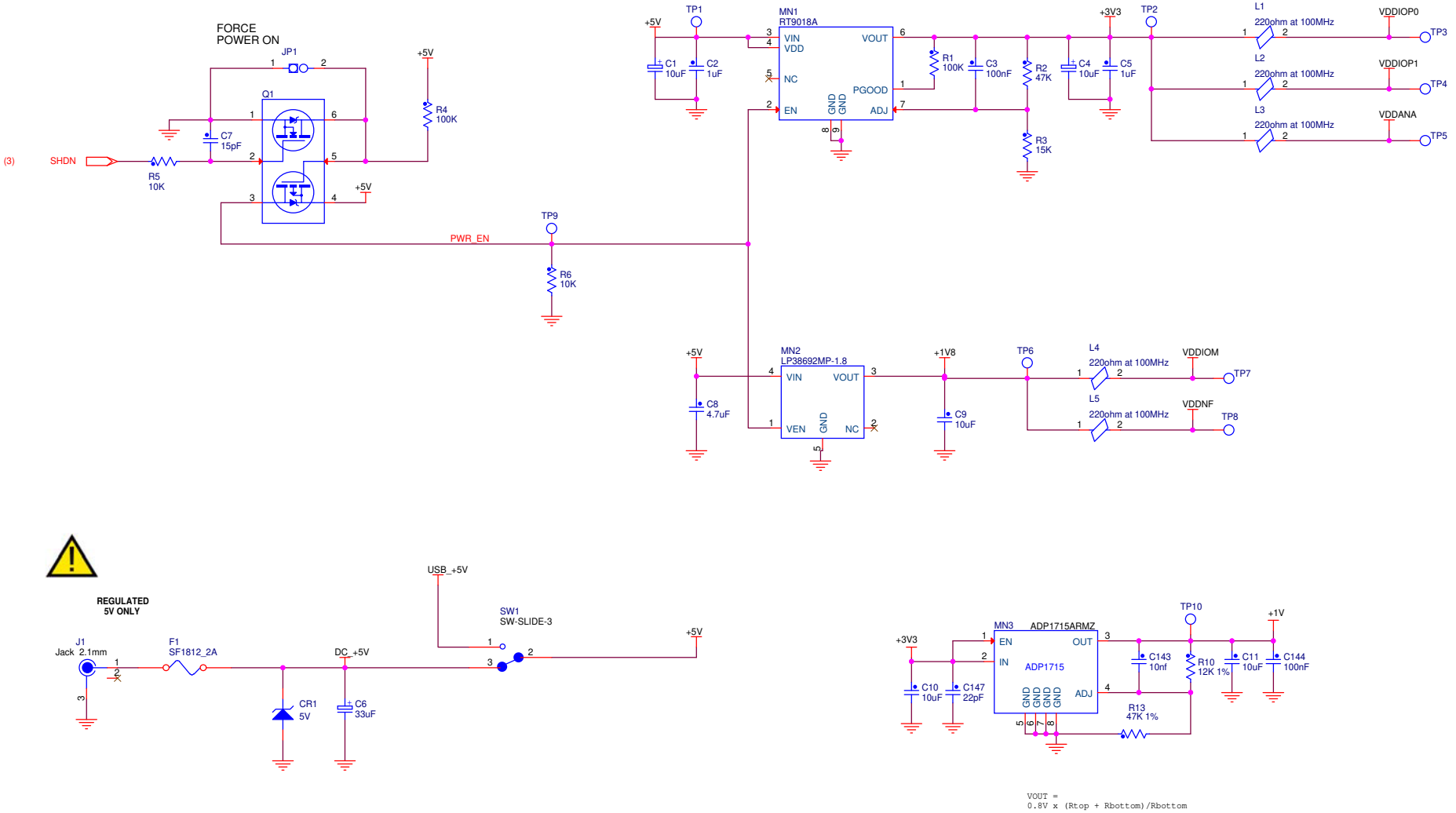
"DNP" means the component is not populated by default

A	INIT EDIT	PP	05-APR-12	PP	05-APR-12	
REV.	MODIF.	DES.	DATE	VER.	DATE	
SCALE 1/1				REV. A	SHEET 1/9	

ATMEL ROUSSET

SAM9CN11-EK

Block Diagram



REV.	MODIF.	DES.	DATE	VER.	DATE
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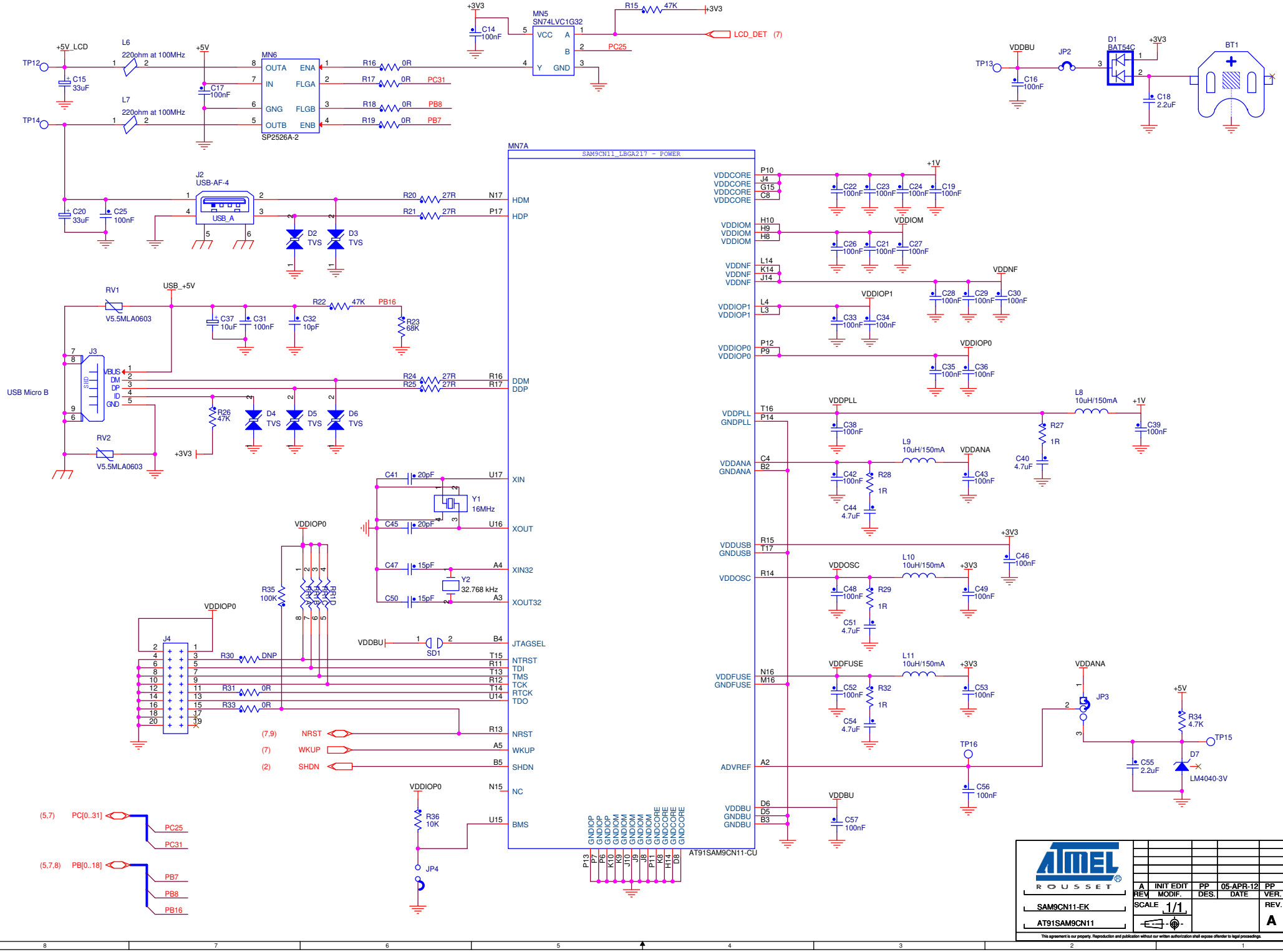
SAM9CN11-EK

POWER SUPPLY

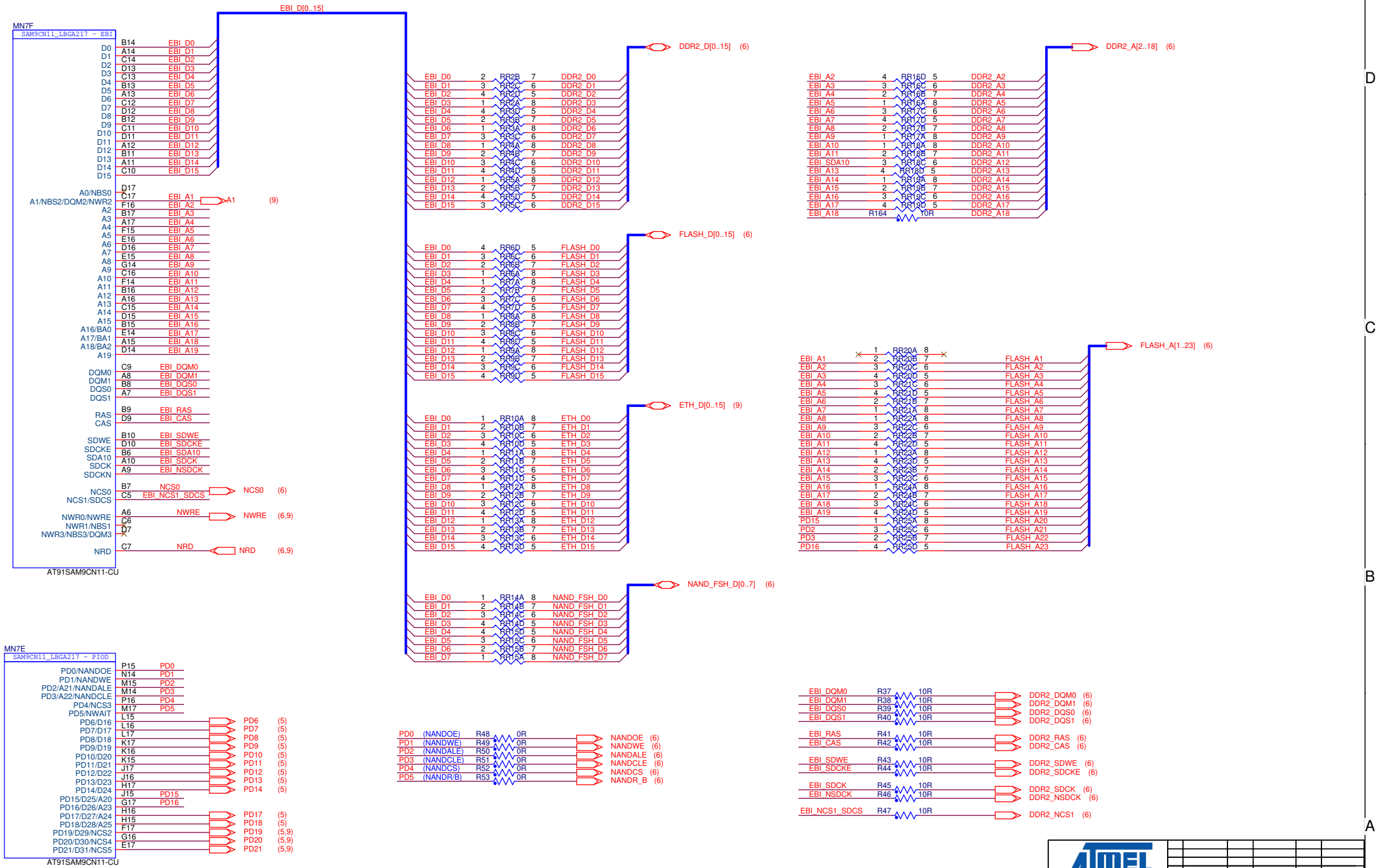
SCALE 1/1

REV. A

SHEET 2/9



A	INIT EDIT	PP	05-APR-12	PP	05-APR-12	
REV.	MODIF.	DES.	DATE	VER.	DATE	
SAM9CN11-EK	SCALE 1/1			REV.	SHEET	
AT91SAM9CN11				A	3/9	


MN7F
SAM9CN11_LBGA217 - EBI
AT91SAM9CN11-CU
EBI_D[0..15]
A1
(9)
NCS0
(6)
NWRE
(6,9)
NRD
(6,9)
DDR2_D[0..15] (6)
FLASH_D[0..15] (6)
ETH_D[0..15] (9)
NAND_FSH_D[0..7] (6)
DDR2_A[2..18] (6)
FLASH_A[1..23] (6)
MN7E
SAM9CN11_LBGA217 - PIOD
AT91SAM9CN11-CU
NANDOE (6)
NANDWE (6)
NANDALE (6)
NANDCLE (6)
NANDCS (6)
NANDR_B (6)
DDR2_DQM0 (6)
DDR2_DQM1 (6)
DDR2_DQS0 (6)
DDR2_DQS1 (6)
DDR2_RAS (6)
DDR2_CAS (6)
DDR2_SDWE (6)
DDR2_SDCKE (6)
DDR2_SDCK (6)
DDR2_NSDCK (6)
DDR2_NCS1 (6)
ATMEL
ROUSSET
SAM9CN11-EK
EBI_INTERFACE
A INIT EDIT PP 05-APR-12 PP 05-APR-12
REV. MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. A
SHEET 4/9
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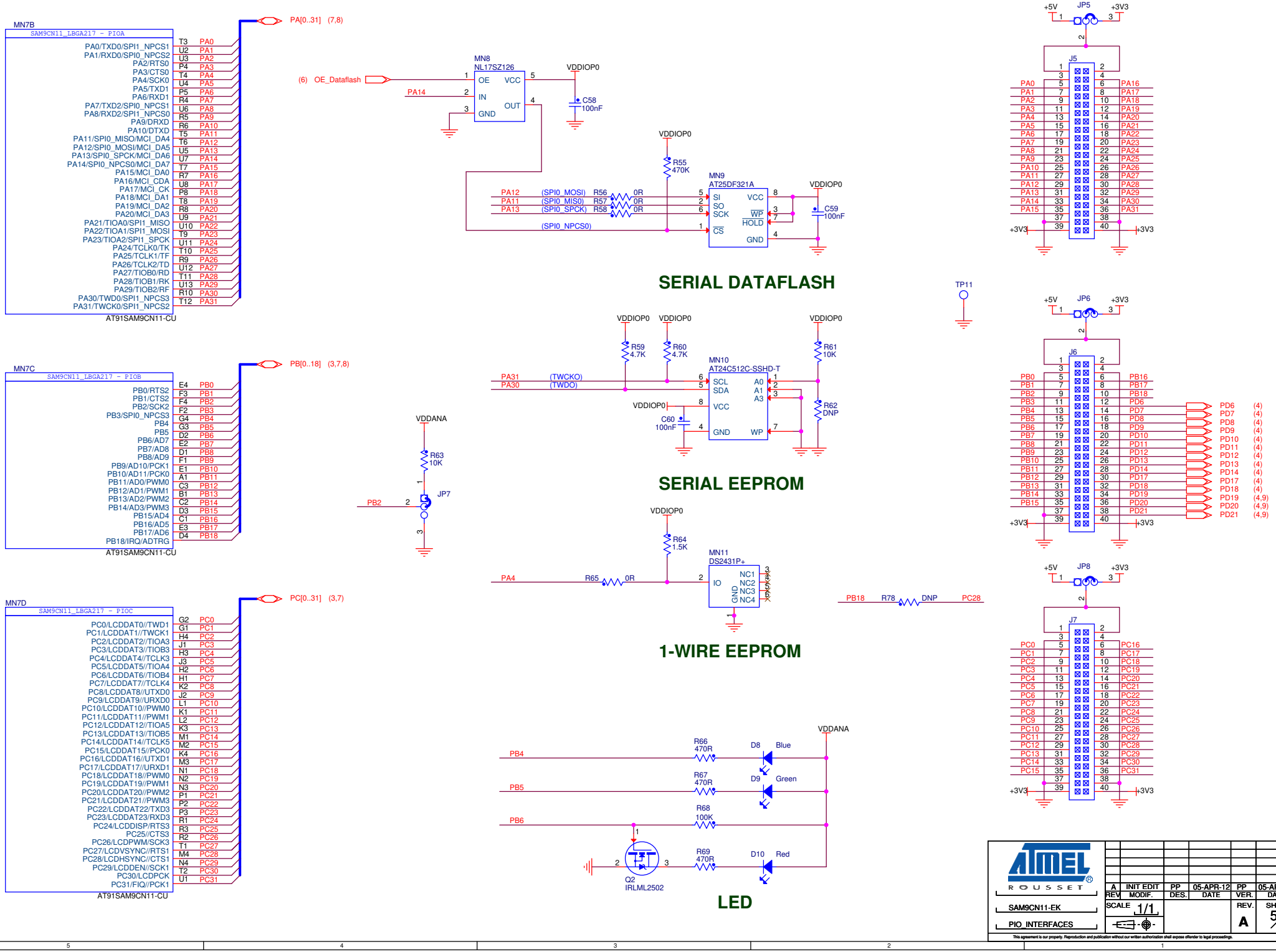
MN7B
SAM9CN11_LBGA217 - PIOA
PA0/TXD0/SPI1_NPCS1
PA1/RXD0/SPI0_NPCS2
PA2/RTS0
PA3/CTS0
PA4/SCK0
PA5/TXD1
PA6/RXD1
PA7/TXD2/SPI0_NPCS1
PA8/RXD2/SPI1_NPCS0
PA9/DRXD
PA10/DTXD
PA11/SPI0_MISO/MCI_DA4
PA12/SPI0_MOSI/MCI_DA5
PA13/SPI0_SPCK/MCI_DA6
PA14/SPI0_NPCS0/MCI_DA7
PA15/MCI_DA0
PA16/MCI_CDA
PA17/MCI_CK
PA18/MCI_DA1
PA19/MCI_DA2
PA20/MCI_DA3
PA21/TIOA0/SPI1_MISO
PA22/TIOA1/SPI1_MOSI
PA23/TIOA2/SPI1_SPCK
PA24/TCLK0/TK
PA25/TCLK1/TF
PA26/TCLK2/TD
PA27/TIOB0/RD
PA28/TIOB1/RK
PA29/TIOB2/RF
PA30/TWD0/SPI1_NPCS3
PA31/TWCK0/SPI1_NPCS2
AT91SAM9CN11-CU
PA[0..31] (7,8)
MN8
NL17SZ126
OE
VCC
IN
OUT
GND
(6) OE_Dataflash
PA14
VDDIOP0
C58
100nF
R55
470K
MN9
AT25DF321A
SI
SO
SCK
CS
VCC
WP
HOLD
GND
PA12 (SPI0_MOSI) R56 0R
PA11 (SPI0_MISO) R57 0R
PA13 (SPI0_SPCK) R58 0R
(SPI0_NPCS0)
C59
100nF
SERIAL DATAFLASH
+5V
JP5
+3V3
J5
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PA16
PA17
PA18
PA19
PA20
PA21
PA22
PA23
PA24
PA25
PA26
PA27
PA28
PA29
PA30
PA31
MN7C
SAM9CN11_LBGA217 - PIOB
PB0/RTS2
PB1/CTS2
PB2/SCK2
PB3/SPI0_NPCS3
PB4
PB5
PB6/AD7
PB7/AD8
PB8/AD9
PB9/AD10/PCK1
PB10/AD11/PCK0
PB11/AD0/PWM0
PB12/AD1/PWM1
PB13/AD2/PWM2
PB14/AD3/PWM3
PB15/AD4
PB16/AD5
PB17/AD6
PB18/IRQ/ADTRG
AT91SAM9CN11-CU
PB[0..18] (3,7,8)
VDDANA
R63
10K
JP7
PB2
TP11
MN10
AT24C512C-SSHD-T
SCL
SDA
VCC
A0
A1
A2
GND
WP
PA31 (TWCKO)
PA30 (TWDO)
R59
4.7K
R60
4.7K
R61
10K
R62
DNP
C60
100nF
SERIAL EEPROM
+5V
JP6
+3V3
J6
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
PB16
PB17
PB18
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD17
PD18
PD19
PD20
PD21
MN7D
SAM9CN11_LBGA217 - PIOC
PC0/LCDDAT0//TWD1
PC1/LCDDAT1//TWCK1
PC2/LCDDAT2//TIOA3
PC3/LCDDAT3//TIOB3
PC4/LCDDAT4//TCLK3
PC5/LCDDAT5//TIOA4
PC6/LCDDAT6//TIOB4
PC7/LCDDAT7//TCLK4
PC8/LCDDAT8//UTXD0
PC9/LCDDAT9//URXD0
PC10/LCDDAT10//PWM0
PC11/LCDDAT11//PWM1
PC12/LCDDAT12//TIOA5
PC13/LCDDAT13//TIOB5
PC14/LCDDAT14//TCLK5
PC15/LCDDAT15//PCK0
PC16/LCDDAT16//UTXD1
PC17/LCDDAT17//URXD1
PC18/LCDDAT18//PWM0
PC19/LCDDAT19//PWM1
PC20/LCDDAT20//PWM2
PC21/LCDDAT21//PWM3
PC22/LCDDAT22/TXD3
PC23/LCDDAT23/RXD3
PC24/LCDDISP/RTS3
PC25//CTS3
PC26/LCDPWM/SCK3
PC27/LCDVSYNC//RTS1
PC28/LCDHSYNC//CTS1
PC29/LCDDEN//SCK1
PC30/LCDPCK
PC31/FIQ//PCK1
AT91SAM9CN11-CU
PC[0..31] (3,7)
MN11
DS2431P+
IO
NC1
NC2
NC3
NC4
GND
PA4
R64
1.5K
R65
0R
1-WIRE EEPROM
PB18
R78
DNP
PC28
+5V
JP8
+3V3
J7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
PC16
PC17
PC18
PC19
PC20
PC21
PC22
PC23
PC24
PC25
PC26
PC27
PC28
PC29
PC30
PC31
VDDANA
PB4
PB5
PB6
R66
470R
R67
470R
R68
100K
R69
470R
D8
Blue
D9
Green
D10
Red
Q2
IRLML2502
LED
ATMEL
ROUSSET
SAM9CN11-EK
PIO_INTERFACES
A
INIT EDIT
PP
05-APR-12
REV.
MODIF.
DES.
DATE
SCALE 1/1
REV. A
SHEET 5/9
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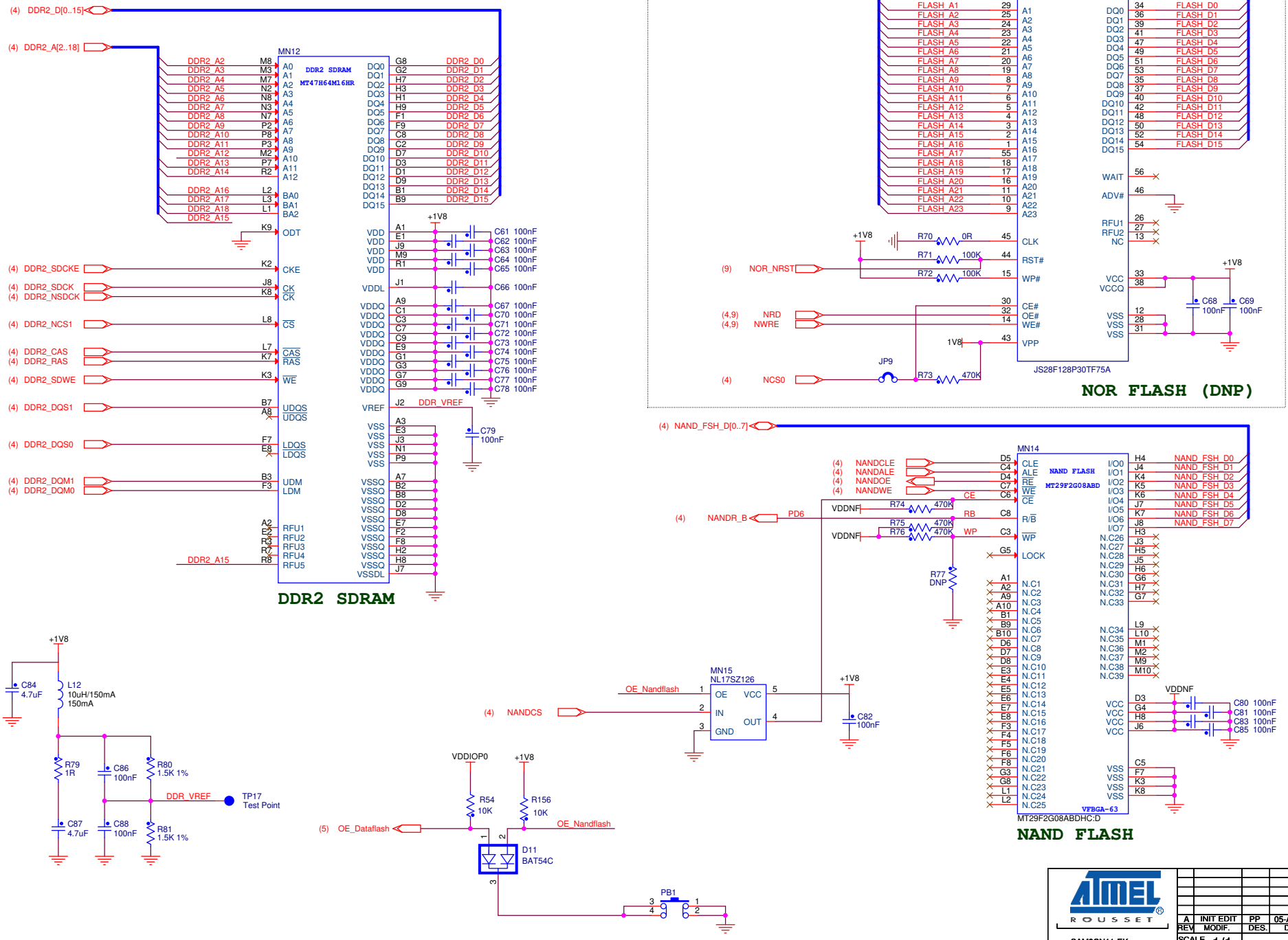
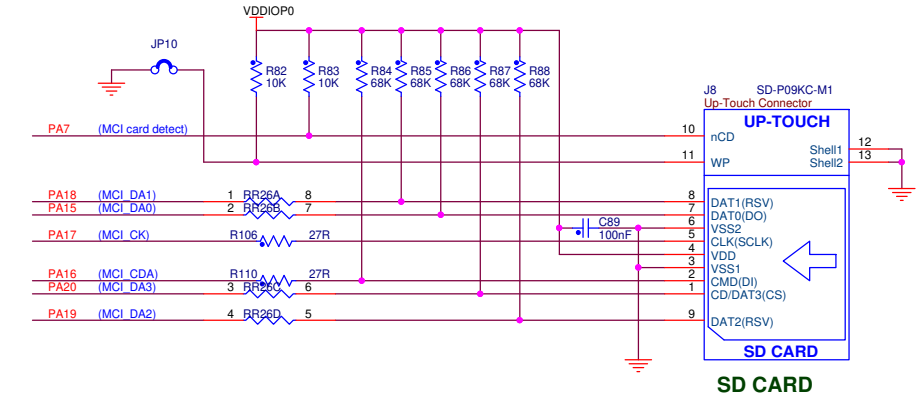
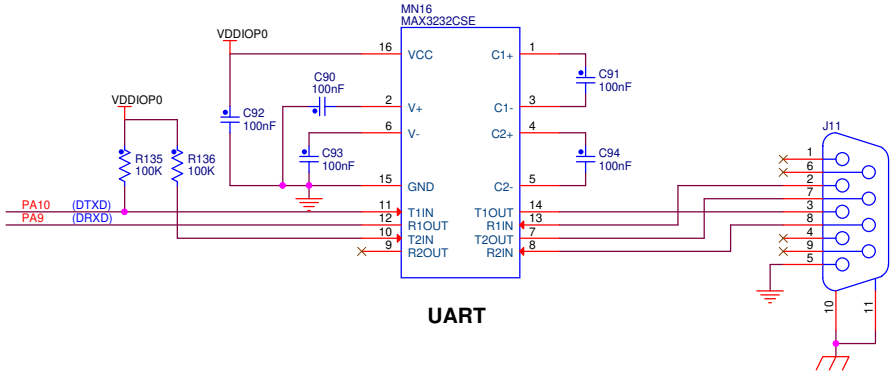
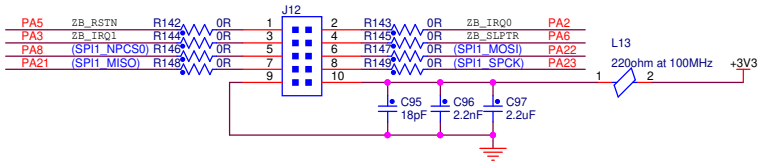

DDR2 SDRAM
MT47H64M16HR
MN12
(4) DDR2_D[0..15]
(4) DDR2_A[2..18]
(4) DDR2_SDCKE
(4) DDR2_SDCK
(4) DDR2_NSDCK
(4) DDR2_NCS1
(4) DDR2_CAS
(4) DDR2_RAS
(4) DDR2_SDWE
(4) DDR2_DQS1
(4) DDR2_DQS0
(4) DDR2_DQM1
(4) DDR2_DQM0
DDR2_A15
DDR_VREF
+1V8
VDDIOP0
(4) FLASH_D[0..15]
(4) FLASH_A[1..23]
MN13
JS28F128P30TF75A
NOR FLASH (DNP)
(9) NOR_NRST
(4,9) NRD
(4,9) NWRE
(4) NCS0
JP9
(4) NAND_FSH_D[0..7]
MN14
MT29F2G08ABDHC:D
NAND FLASH
(4) NANDCLE
(4) NANDALE
(4) NANDOE
(4) NANDWE
(4) NANDR_B
PD6
VDDNF
MN15
NL17SZ126
OE_Nandflash
(4) NANDCS
(5) OE_Dataflash
D11
BAT54C
PB1
TP17
Test Point
L12
10uH/150mA
150mA
SAM9CN11-EK
DDR2 NAND FLASH
SCALE 1/1
REV. A
SHEET 6/9



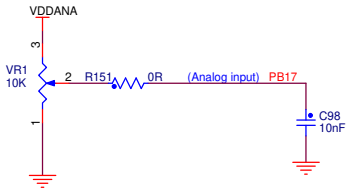
SD CARD

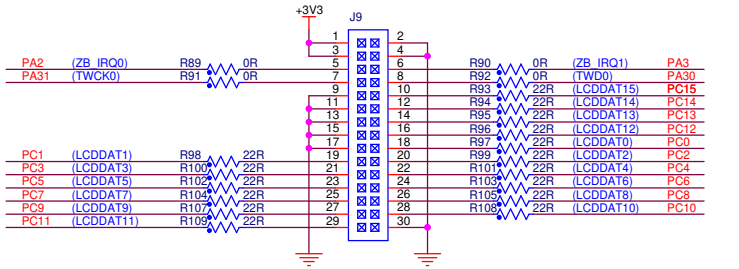


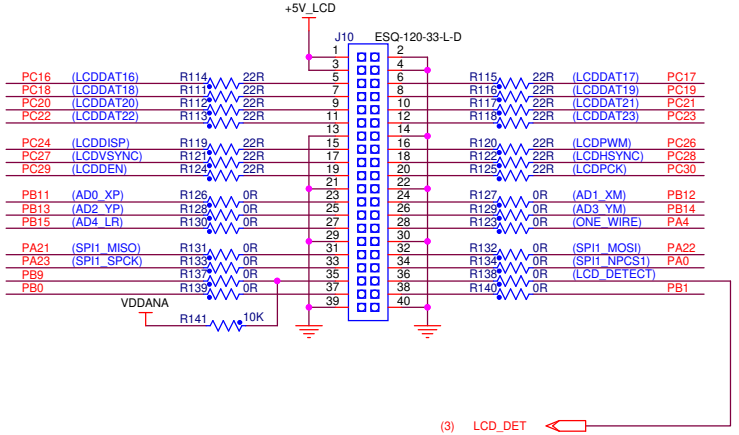
UART

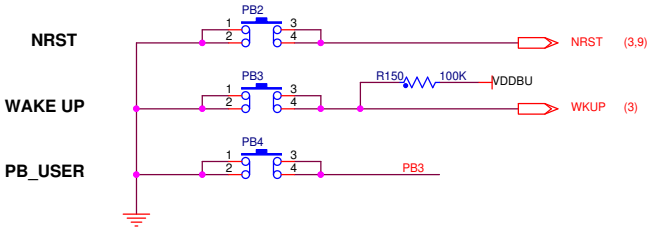


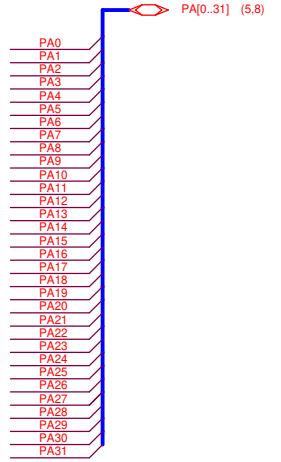
ZIGBEE

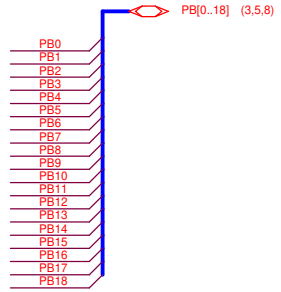


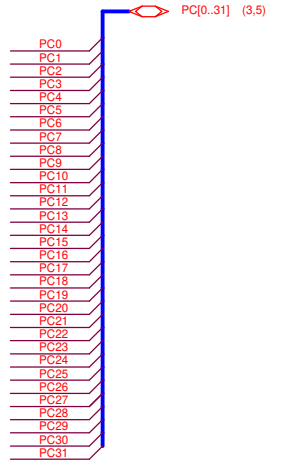












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REV.	MODIF.	DES.	DATE	VER.	DATE

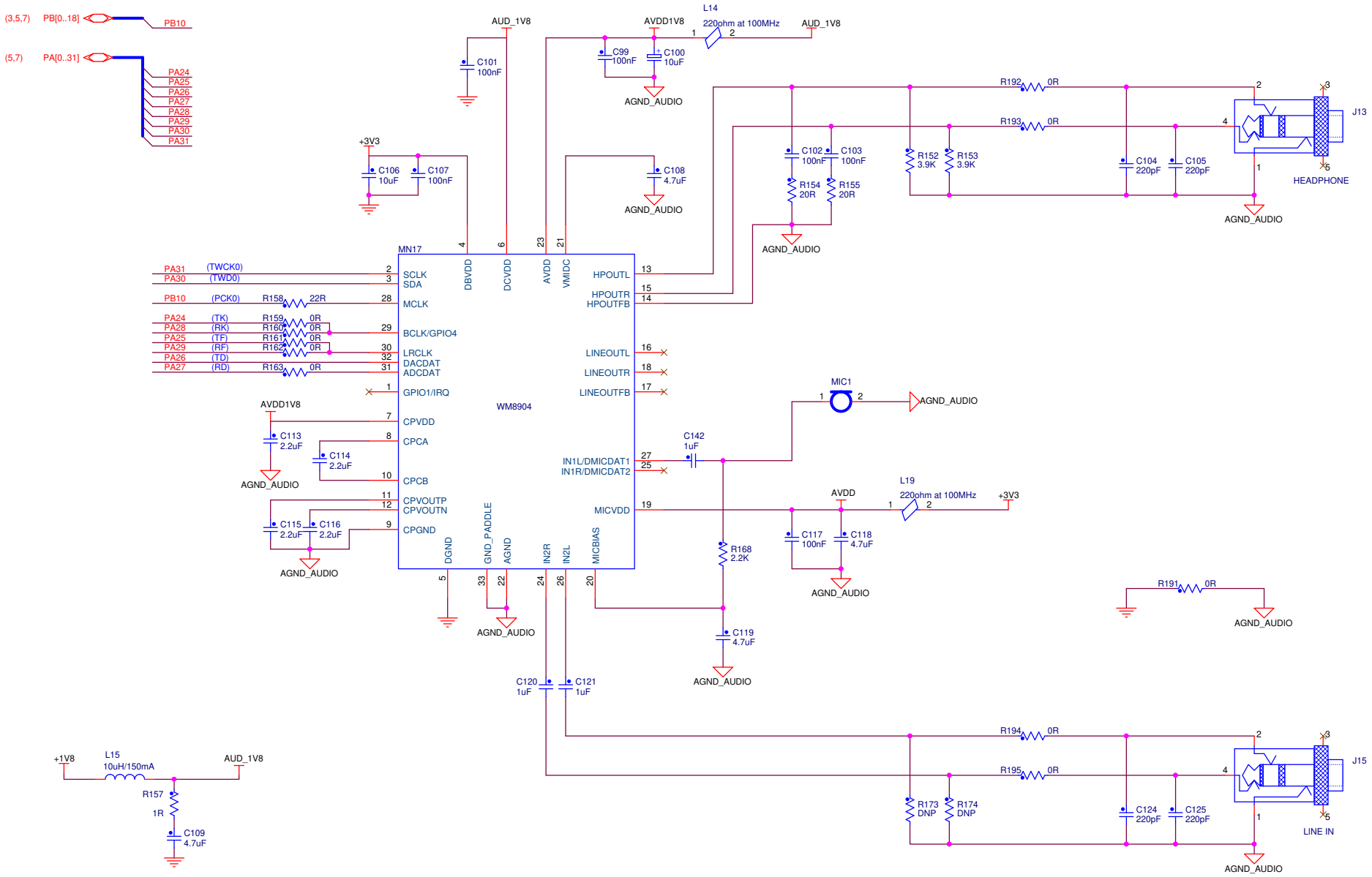
SAM9CN11-EK

SERIAL INTERFACES

SCALE 1/1

REV. A

SHEET 7/9



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REV.	MODIF.	DES.	DATE	VER.	DATE	

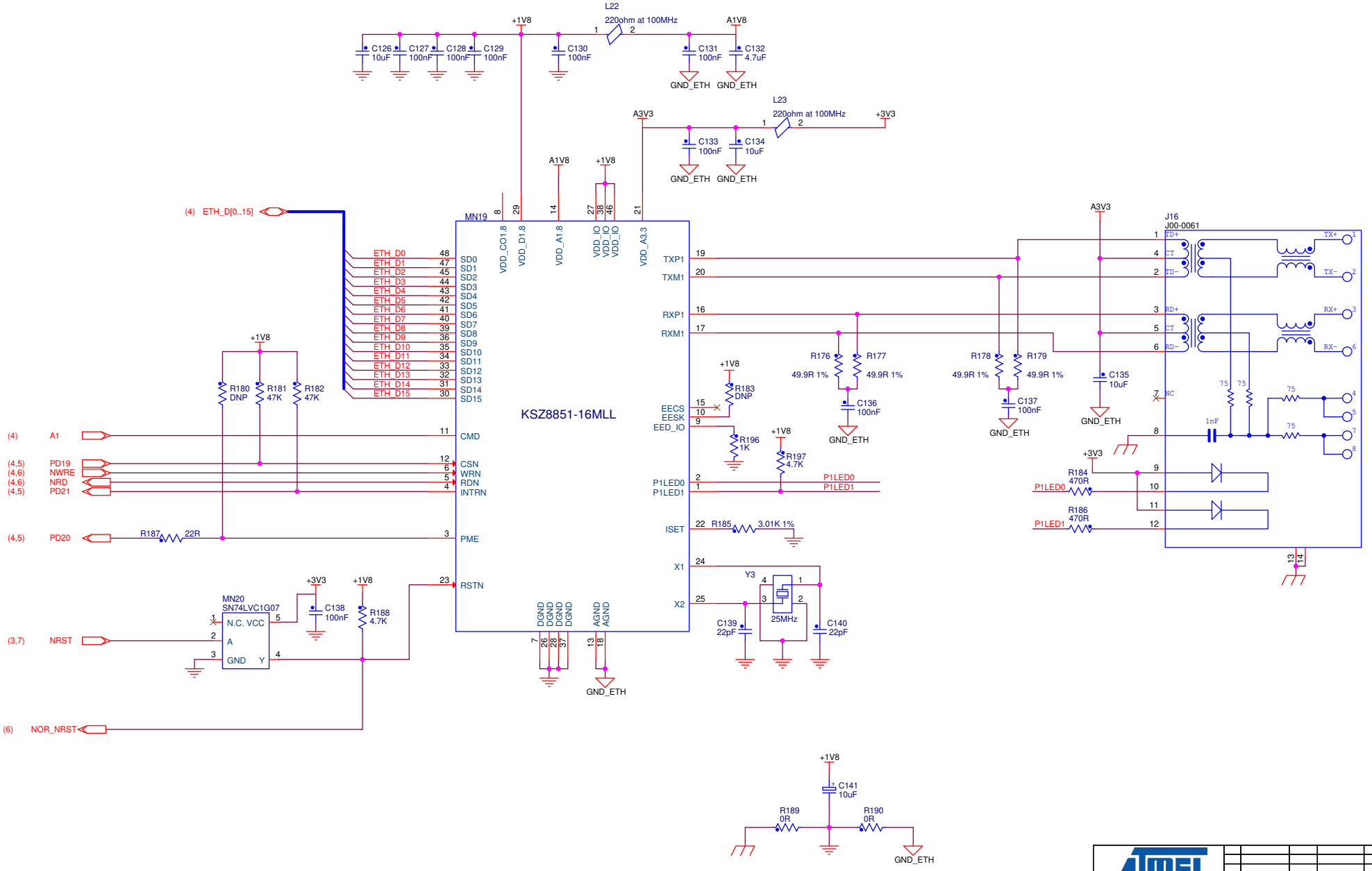
SAM9CN11-EK

AUDIO

SCALE 1/1

REV. A

SHEET 8/9



REV.	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	PP	05-APR-12	PP	05-APR-12

SAM9CN11-EK

ETH

SCALE 1/1

REV. A

SHEET 9/9

Section 6

Display Module Hardware

6.1 Board Overview

SAM9N12/CN11-DM board carries a 4.3” TFT LCD module with touch screen.

The DM board also carries four QTouch pads.

Figure 6-1. DM Board

6.2 Equipment List

Here is the list of the DM board components:

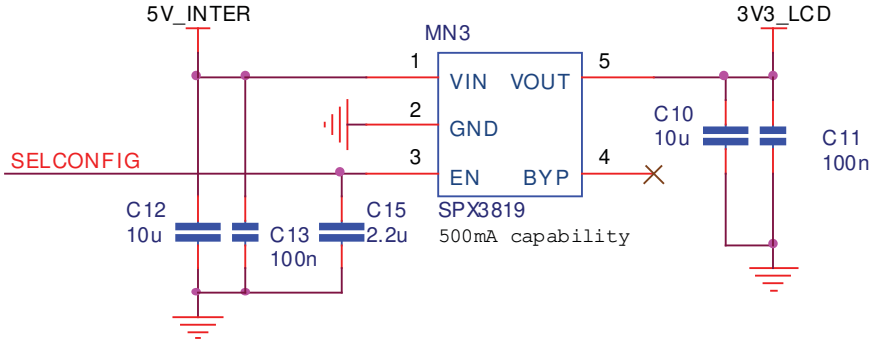
- One 4.3” TFT LCD module
- LCD Back light driver
- 3.3V regulator
- QTouch device
- 1-Wire device

6.3 Function Blocks

6.3.1 3.3V Regulator

The SAM9N12/CN11-DM board features its own LDO for local power regulation. It accepts DC 5V power from a 500 mA power switch on the EK and outputs a regulated +3.3V to most other circuits on the board.

Figure 6-2. DM Board Power Supply



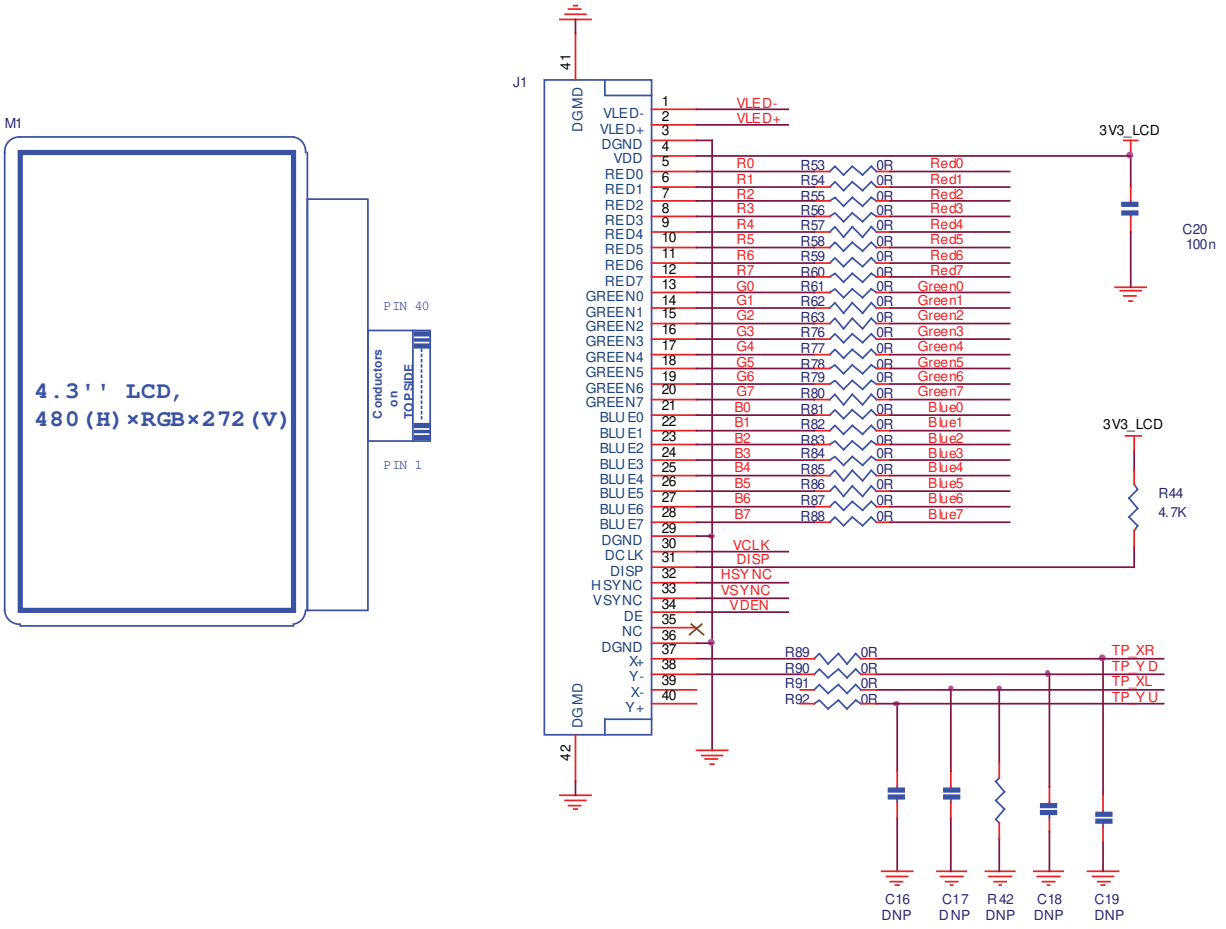
6.3.2 TFT LCD with Touch Panel

The SAM9N12/CN11-DM board features an LCD controller. The 4.3" 480x272 LCD provides the DM with a low power LCD display feature, back light unit and a touch panel, similar to that used on commercial PDAs.

Graphics and text can be displayed on the dot matrix panel with up to 16 million colors by supplying 24-bit data signals (8 bit x RGB by default). This allows the user to develop graphical user interfaces for a wide variety of end applications.

Warning: Never connect/disconnect the LCD display from the board while the power supply is on. Doing so may damage both units.

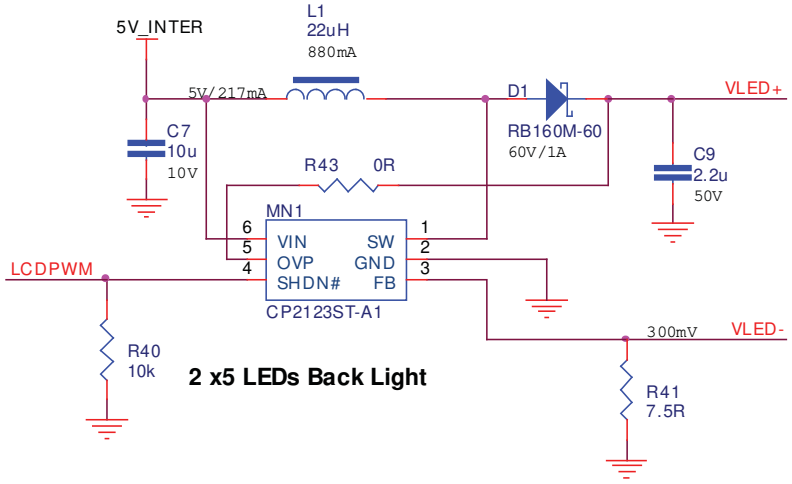
Figure 6-3. LCD with Touch Panel



6.3.3 Back Light

The back light voltage is generated from a CP2122ST boost converter. It is powered directly by the DC 5 V from the EK board. The back light level is controlled by a PWM signal generated from the SAM9N12/CN11 processor.

Figure 6-4. Back Light Control

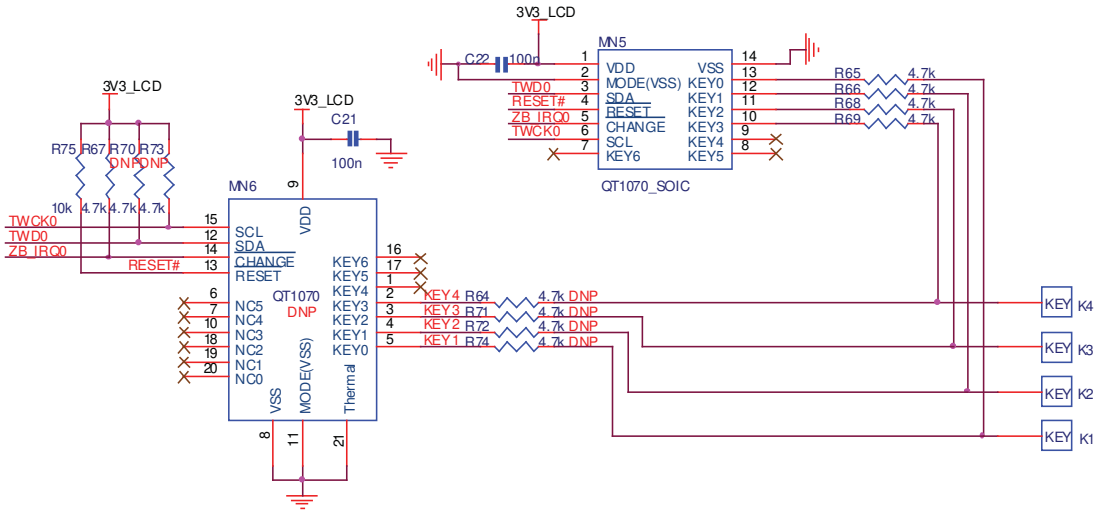


6.3.4 QTouch

The SAM9N12/CN11-DM board carries a QTouch device piloted through a TWI interface. It manages four capacitive touch buttons directly printed on the PCB.

There are dual footprints for the QTouch device, and SOIC is the default mounted one.

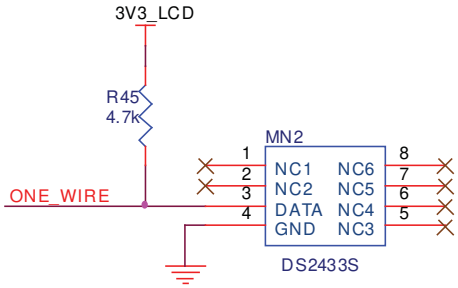
Figure 6-5. QTouch



6.3.5 1-Wire

The DM board also uses 1-Wire device as “soft label” to store the information such as chip type, manufacture name, production date, etc.

Figure 6-6. 1-Wire on DM



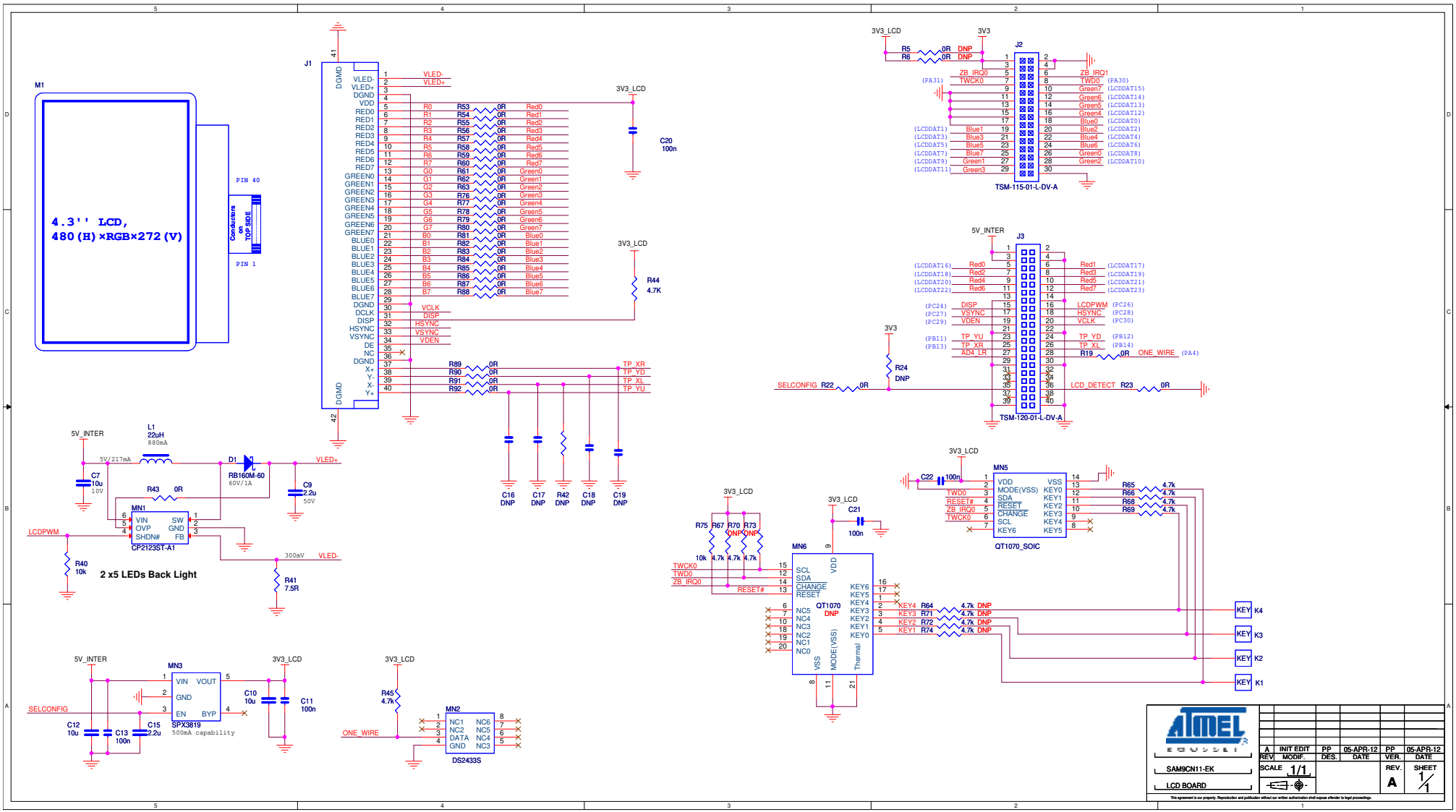
Section 7

DM Schematics

7.1 DM Board Schematics

This section contains the following schematic:

- LCD Board


M1
4.3'' LCD,
480 (H) ×RGB×272 (V)
PIN 40
PIN 1
Conductors on TOP SIDE
J1
DGMD
VLED-
VLED+
DGND
VDD
RED0
RED1
RED2
RED3
RED4
RED5
RED6
RED7
GREEN0
GREEN1
GREEN2
GREEN3
GREEN4
GREEN5
GREEN6
GREEN7
BLUE0
BLUE1
BLUE2
BLUE3
BLUE4
BLUE5
BLUE6
BLUE7
DCLK
DISP
HSYNC
VSYNC
VDEN
NC
X+
Y-
X-
Y+
3V3_LCD
C20
100n
R44
4.7K
TP_XR
TP_YD
TP_XL
TP_YU
C16 DNP
C17 DNP
R42 DNP
C18 DNP
C19 DNP
5V_INTER
L1
22uH
880mA
5V/217mA
D1
RB160M-60
60V/1A
VLED+
C7
10u
10V
C9
2.2u
50V
R43
0R
MN1
CP2123ST-A1
LCDPWM
R40
10k
2 x5 LEDs Back Light
300mV
VLED-
R41
7.5R
J2
TSM-115-01-L-DV-A
3V3_LCD
3V3
R5
R6
0R DNP
ZB_IRQ0
TWCK0
ZB_IRQ1
TWD0
Green7
Green6
Green5
Green4
Blue0
Blue2
Blue4
Blue6
Green0
Green2
Blue1
Blue3
Blue5
Blue7
Green1
Green3
J3
TSM-120-01-L-DV-A
5V_INTER
Red0
Red2
Red4
Red6
Red1
Red3
Red5
Red7
DISP
VSYNC
VDEN
LCDPWM
HSYNC
VCLK
TP_YU
TP_XR
AD4_LR
TP_YD
TP_XL
R19
0R
ONE_WIRE
R24
DNP
SELCONFIG R22
0R
LCD_DETECT R23
0R
MN5
QT1070_SOIC
C22
100n
R65
R66
R68
R69
4.7k
MN6
QT1070
DNP
C21
100n
R75
R67
R70
R73
10k
4.7k
TWCK0
TWD0
ZB_IRQ0
RESET#
KEY6
KEY5
KEY4
KEY3
KEY2
KEY1
KEY0
R64
R71
R72
R74
4.7k DNP
K4
K3
K2
K1
MN3
SPX3819
500mA capability
C10
10u
C11
100n
C12
10u
C13
100n
C15
2.2u
R45
4.7k
MN2
DS2433S
ONE_WIRE
ATMEL
SAM9CN11-EK
LCD BOARD
SCALE 1/1
REV. A
SHEET 1/1
A INIT EDIT PP 05-APR-12
REV. MODIF. DES. DATE
PP 05-APR-12
VER. DATE

Section 8

Revision History

8.1 Revision History

Table 8-1.

Document	Comments	Change Request Ref.
11186A	First issue.	

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