



# STL9N3LLH5

N-channel 30 V, 0.015  $\Omega$  typ., 9 A STripFET™ V Power MOSFET in a PowerFLAT™ (3.3x3.3) package

Datasheet — production data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STL9N3LLH5	30 V	< 0.019 $\Omega$	9 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

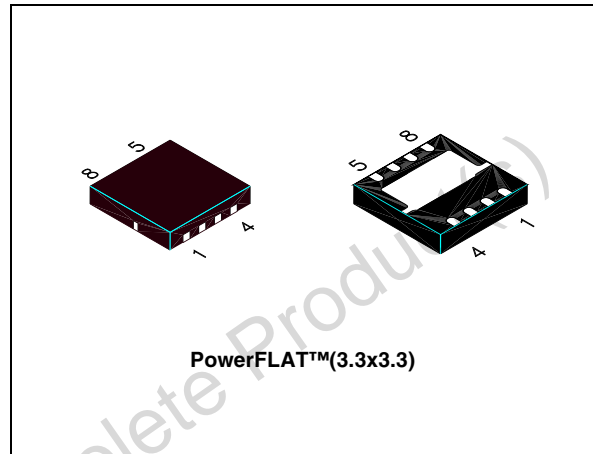


Figure 1. Internal schematic diagram

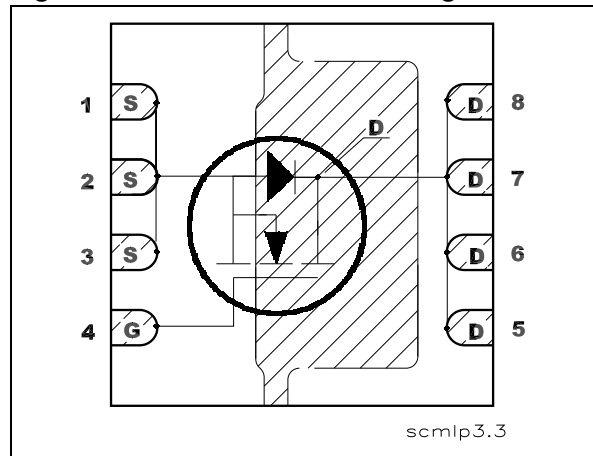


Table 1. Device summary

Order code	Marking	Package	Packaging
STL9N3LLH5	9N3L	PowerFLAT™ (3.3x3.3)	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$T_J$ $T_{stg}$	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The value is rated according  $R_{thj-c}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$
2. Steady state

**Table 4. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}^{(1)}$	Not-repetitive avalanche current	7.5	A
$E_{AS}^{(2)}$	Thermal resistance junction-pcb	150	mJ

1. Pulse width limited by  $T_{Jmax}$ .
2. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AV}$ ,  $V_{DD} = 21\text{ V}$

## 2 Electrical characteristics

( $T_{CASE}=25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 4.5\text{ A}$		15 19	19 22	$\text{m}\Omega$ $\text{m}\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		724	900 <sup>(1)</sup>	pF
$C_{oss}$	Output capacitance			132	165 <sup>(1)</sup>	pF
$C_{rss}$	Reverse transfer capacitance			20	25 <sup>(1)</sup>	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 9\text{ A}$		5	6 <sup>(1)</sup>	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5\text{ V}$		2	2.5 <sup>(1)</sup>	nC
$Q_{gd}$	Gate-drain charge	(see Figure 14)		2	2.5 <sup>(1)</sup>	nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV Open drain			3.3	$\Omega$

1. Max values not tested

**Table 7. Switching times <sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 4.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13)		4	5	ns	
$t_r$	Rise time			4.2	5.2	ns	
$t_{d(off)}$	Turn-off delay time				21	26	ns
$t_f$	Fall time				3.5	4.25	ns

1. Max values not tested

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD}=9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 18)</i>	-	21		ns
$Q_{rr}$	Reverse recovery charge			10		nC
$I_{RRM}$	Reverse recovery current			1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

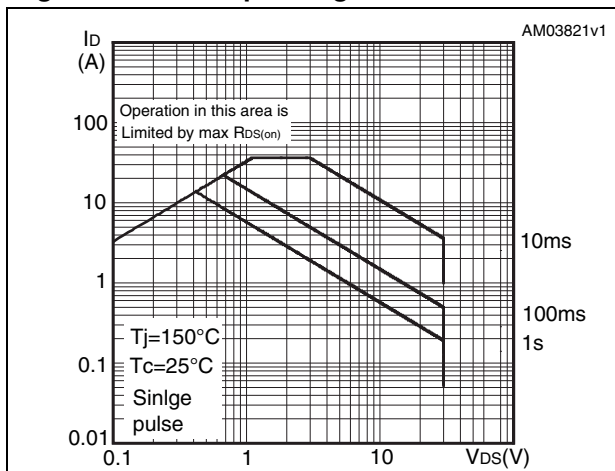


Figure 3. Thermal impedance

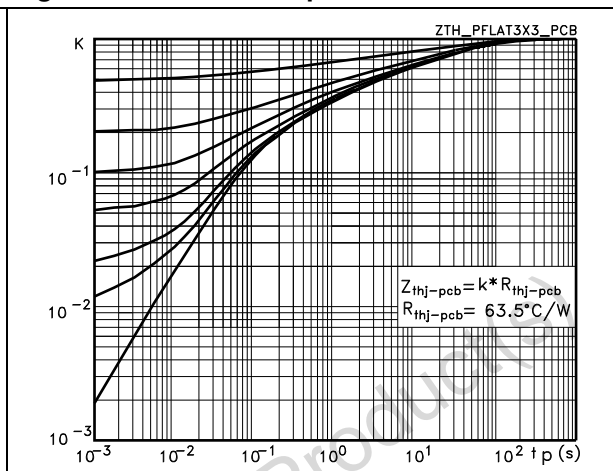


Figure 4. Output characteristics

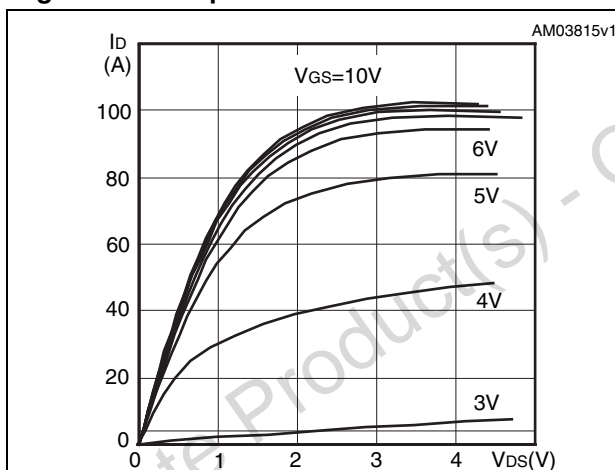


Figure 5. Transfer characteristics

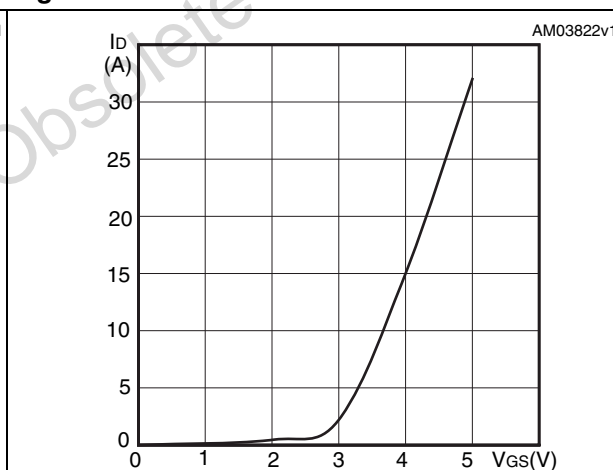


Figure 6. Normalized  $B_{VDS}$  vs temperature

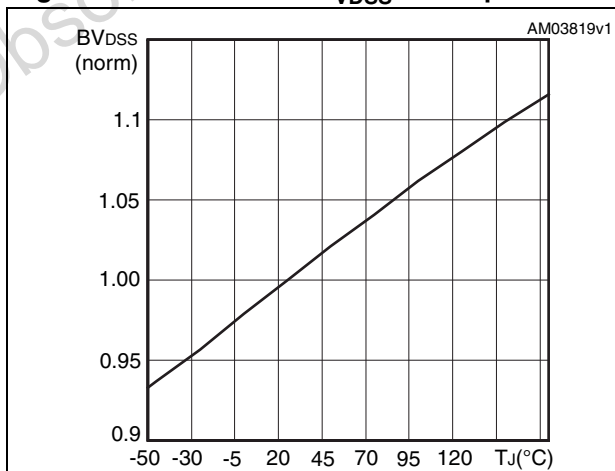


Figure 7. Static drain-source on-resistance

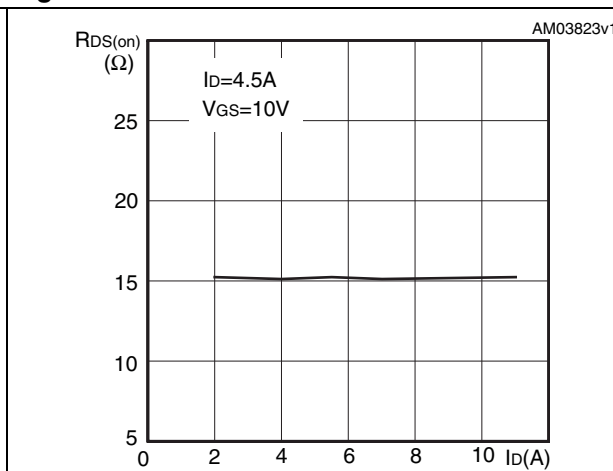


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

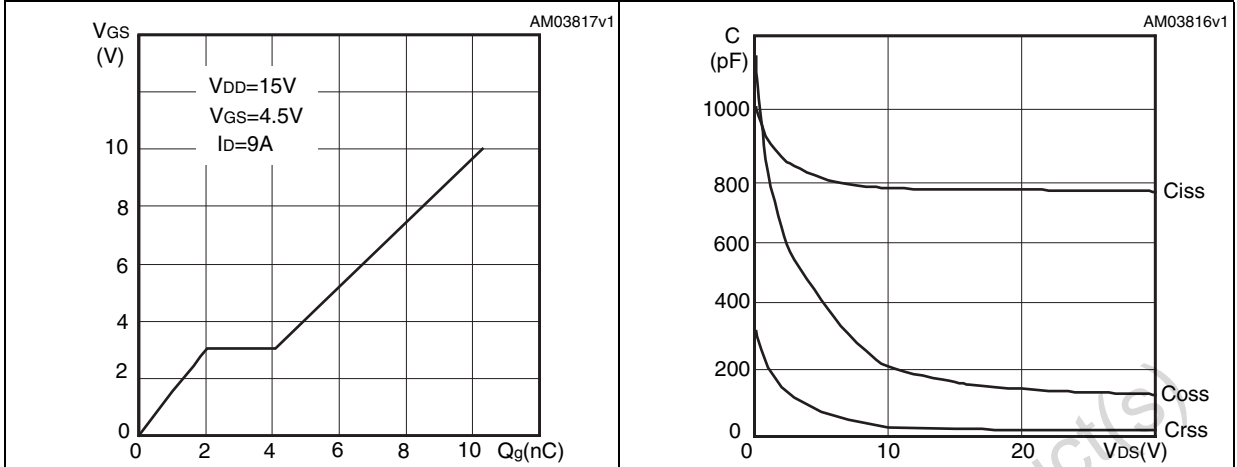


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

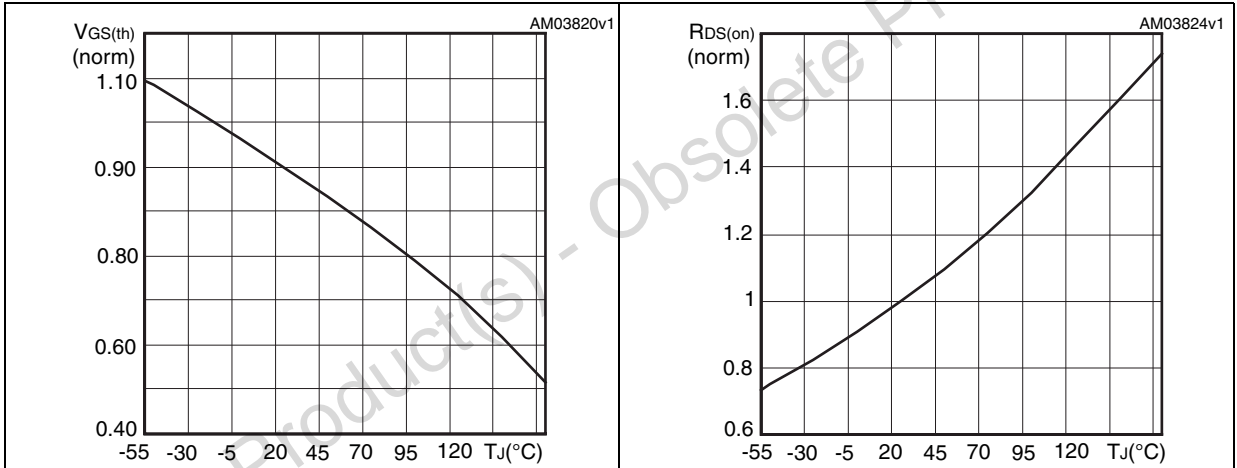
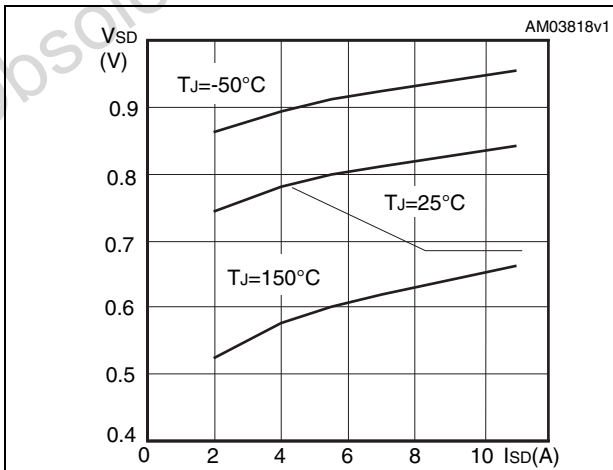
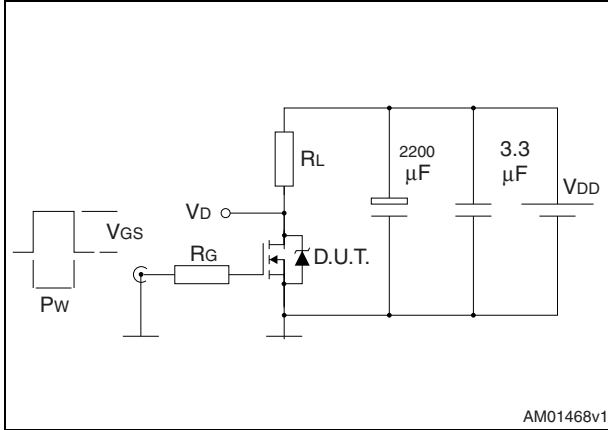


Figure 12. Source-drain diode forward characteristics

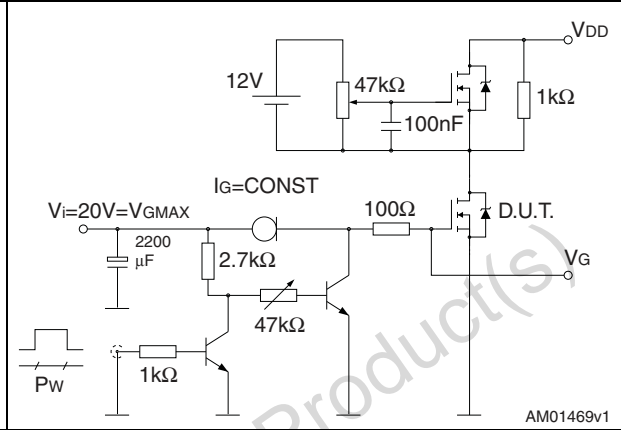


### 3 Test circuits

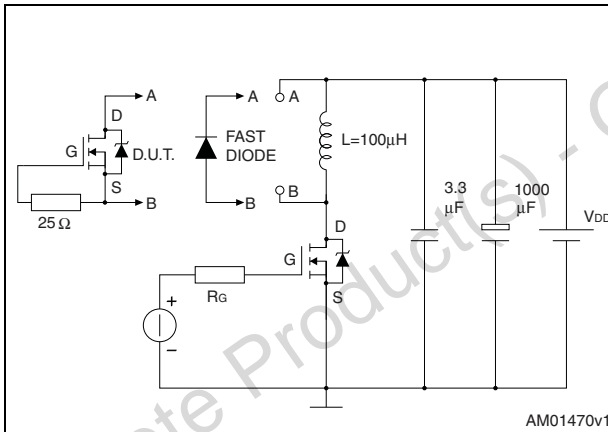
**Figure 13. Switching times test circuit for resistive load**



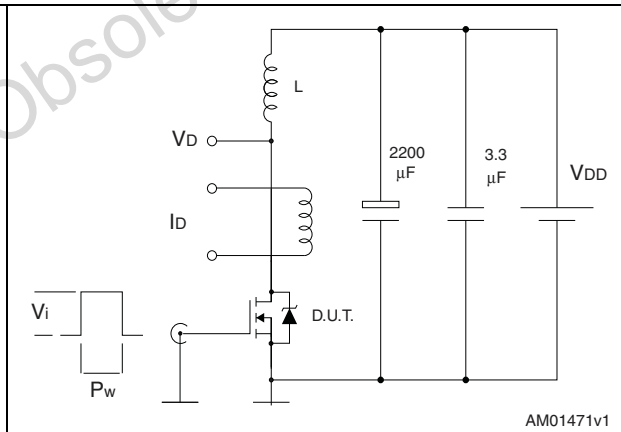
**Figure 14. Gate charge test circuit**



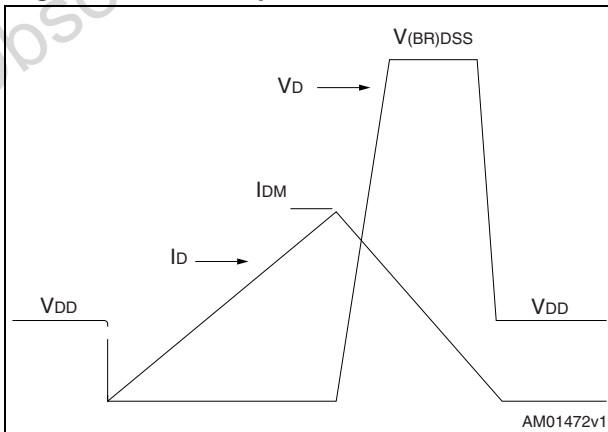
**Figure 15. Test circuit for inductive load switching and diode recovery times**



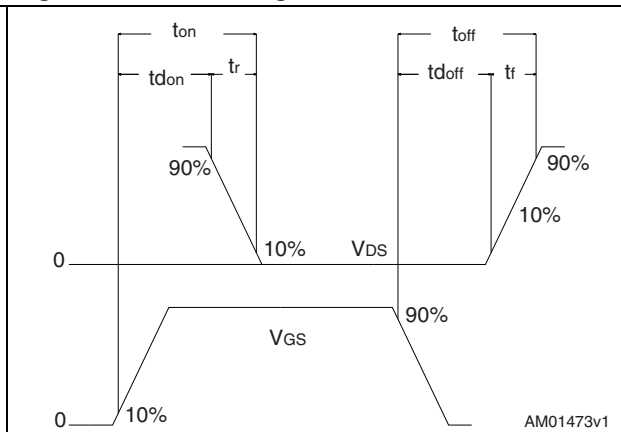
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 9. PowerFLAT™ 3.3 x 3.3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A3		0.20	
b	0.23		0.38
D	3.20	3.30	3.40
D2	2.50		2.75
E	3.20	3.30	3.40
E2	1.25		1.50
e		0.65	
L	0.30		0.50

Figure 19. PowerFLAT™ 3.3 x 3.3 drawing

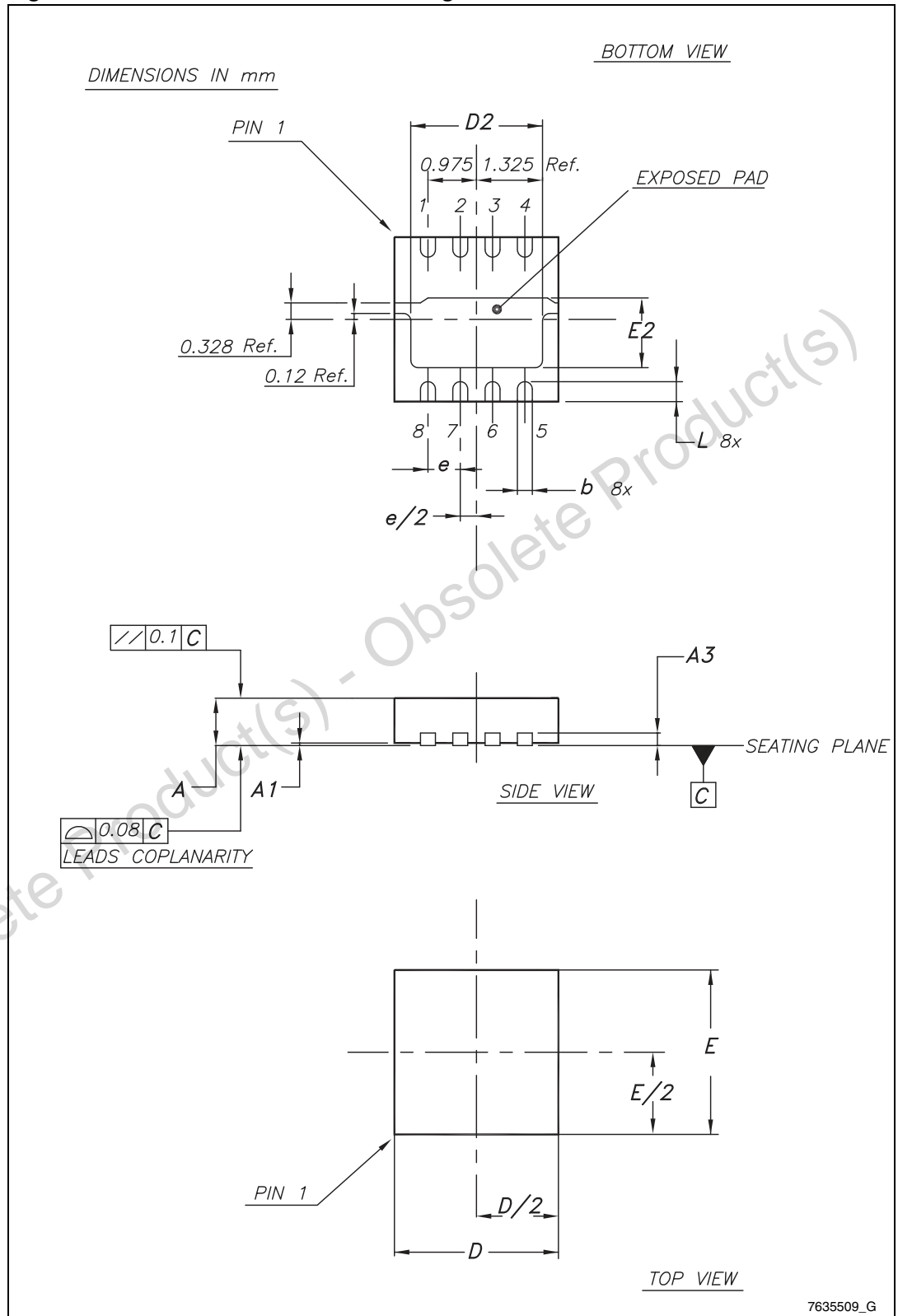
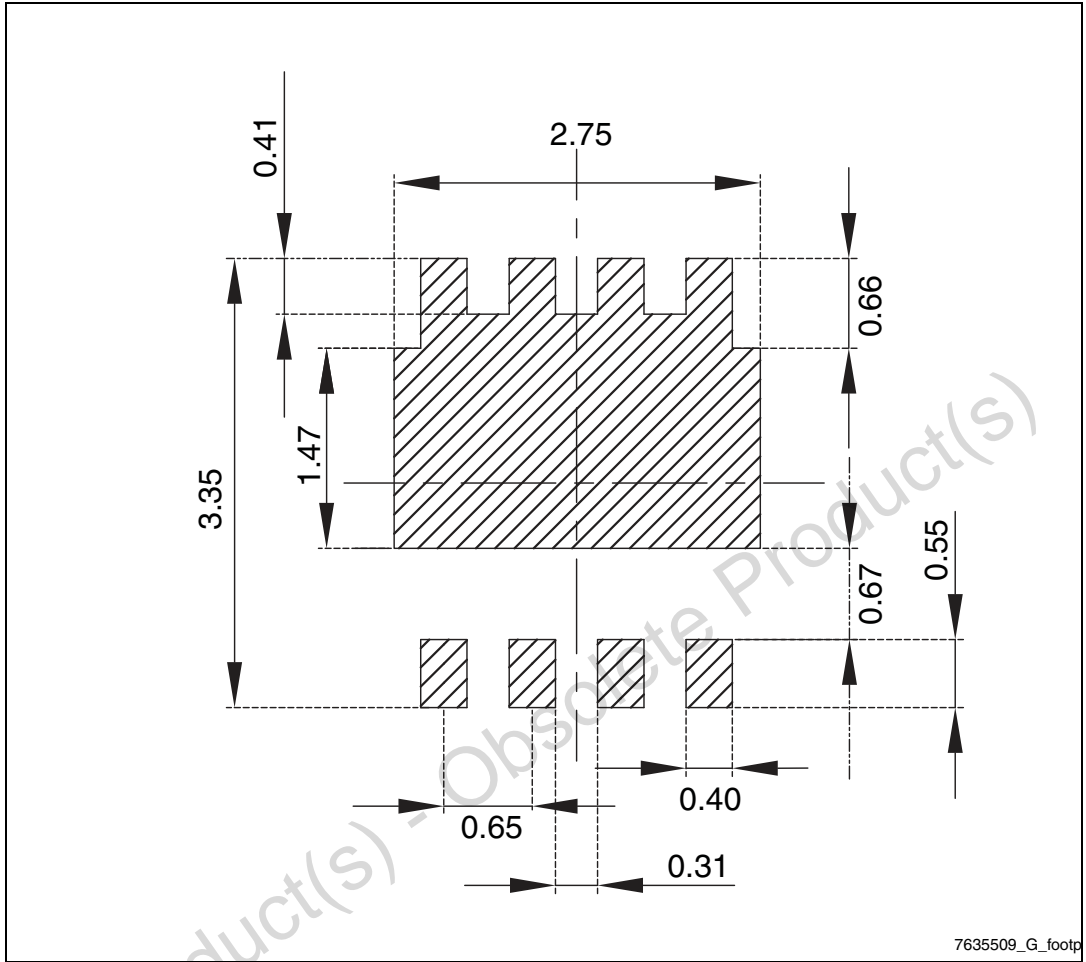


Figure 20. PowerFLAT™ 3.3 x 3.3 recommended footprint



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## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Jul-2009	1	First release
01-Oct-2012	2	Updated <a href="#">Section 4: Package mechanical data</a> . Updated <a href="#">Figure 1</a> , title and description on the cover page.

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