BUK7L06-34ARC

TrenchPLUS standard level FET

Rev. 04 — 13 December 2005 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips General-Purpose Automotive (GPA) TrenchMOS technology.

1.2 Features

- ESD and clamping diodes
- 175 °C rated
- Q101 compliant
- Internal gate resistor

1.3 Applications

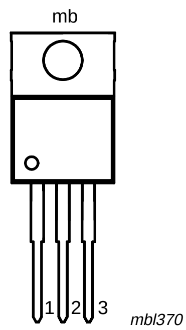
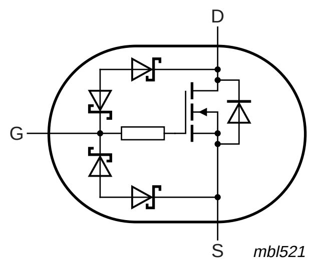
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V loads

1.4 Quick reference data

- $E_{DS(CL)S} \leq 1.0$ J
- $I_D \leq 75$ A
- $R_{DSon} = 5.1$ mΩ (typ)
- $P_{tot} \leq 250$ W

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain (D)	SOT78C (TO-220)	

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BUK7L06-34ARC	3-lead TO-220	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-leads	SOT78C

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

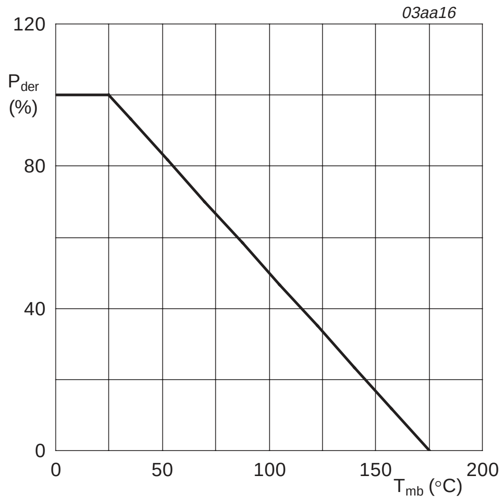
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)		[1]	-	34	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ	[1]	-	34	V
V_{GS}	gate-source voltage (DC)			-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	[2] [4]	-	147	A
			[3]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	[3]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3		-	590	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	250	W
$I_{DG(CL)}$	drain-gate clamping current	t_p = 5 ms; δ = 0.01		-	50	mA
$I_{GS(CL)}$	gate-source clamping current	continuous		-	10	mA
		t_p = 5 ms; δ = 0.01		-	50	mA
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[2] [4]	-	147	A
			[3]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	590	A
Avalanche ruggedness						
$E_{DS(CL)S}$	non-repetitive drain-source clamped energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq 34$ V; V_{GS} = 10 V; starting at T_j = 25 °C		-	1.0	J
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage; all pins	human body model; C = 100 pF; R = 1.5 kΩ		-	8	kV
		human body model; C = 250 pF; R = 1.5 kΩ		-	8	kV

[1] Voltage is limited by clamping

[2] Current is limited by power dissipation chip rating.

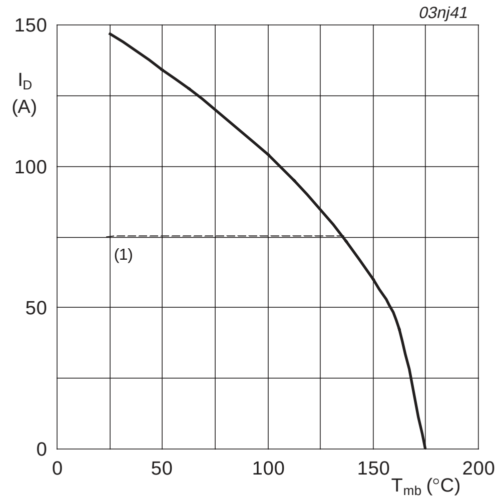
[3] Continuous current is limited by package.

[4] Refer to document *9397 750 12572* for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25\ ^{\circ}C)}} \times 100\ \%$$

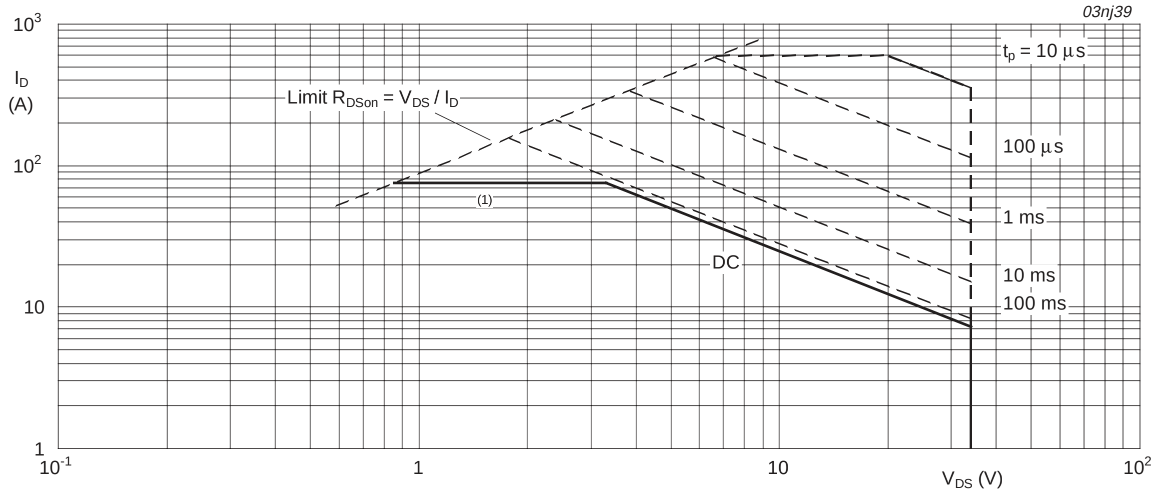
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

(1) Capped at 75 A due to package.

Fig 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25$ °C; I_{DM} is single pulse.

(1) Capped at 75 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.33	0.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W

5.1 Transient thermal impedance

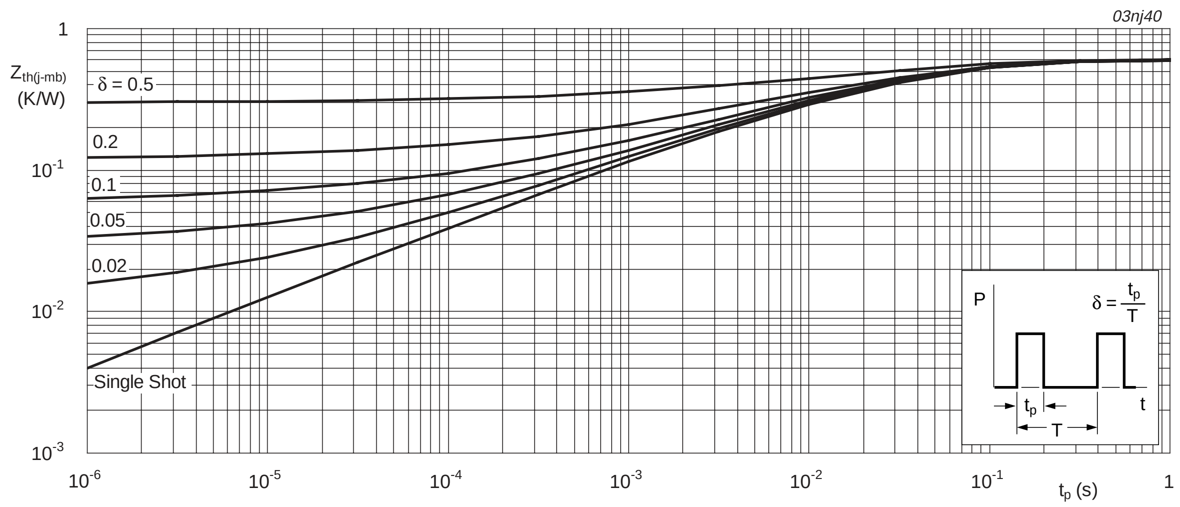


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5: Characteristics

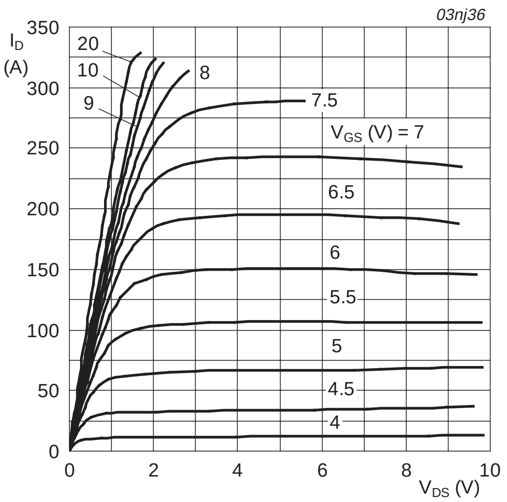
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DG}$	drain-gate zener breakdown voltage	I_D = 2 mA; V_{GS} = 0 V				
		T_j = 25 °C	34	-	45	V
		T_j = –55 °C	34	-	45	V
$V_{DSR(CL)}$	drain-source clamping voltage (DC)	$I_{GS(CL)}$ = –2 mA; I_D = 1 A; Figure 17 and 18	-	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	2.2	3	3.8	V
		T_j = 150 °C	1.5	-	-	V
		T_j = 175 °C	1.2	-	-	V
		T_j = –55 °C	-	-	4.2	V
I_{DSS}	drain-source leakage current	V_{DS} = 16 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.1	2	μA
		T_j = 150 °C	-	5	50	μA
		T_j = 175 °C	-	30	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = ±1 mA; –55 °C < T_j + 175 °C Figure 18 and 19	20	22	-	V
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V				
		T_j = 25 °C	-	5	1000	nA
		T_j = 175 °C	-	-	50	μA
		V_{GS} = 16 V; V_{DS} = 0 V				
		T_j = 175 °C	-	-	150	μA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 30 A; Figure 6 and 8				
		T_j = 25 °C	-	5.1	6	mΩ
		T_j = 175 °C	-	-	11.4	mΩ
		V_{GS} = 16 V; I_D = 30 A	-	4.0	5.3	mΩ
R_G	Internal gate resistor		-	11	-	Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 25 A; V_{DD} = 27 V; V_{GS} = 10 V; Figure 14	-	82	-	nC
Q_{gs}	gate-source charge		-	15	-	nC
Q_{gd}	gate-drain (Miller) charge		-	31	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	3400	4533	pF
C_{oss}	output capacitance		-	1080	1296	pF
C_{rss}	reverse transfer capacitance		-	660	904	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	27	-	ns
t_r	rise time		-	108	-	ns
$t_{d(off)}$	turn-off delay time		-	196	-	ns
t_f	fall time		-	167	-	ns

Table 5: Characteristics *...continued*

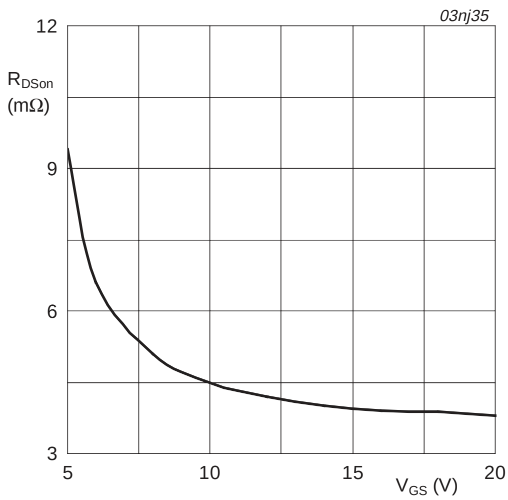
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_d	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die	-	3.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/μs; V_{GS} = 0 V; V_R = 30 V	-	62	-	ns
Q_r	recovered charge		-	44	-	nC



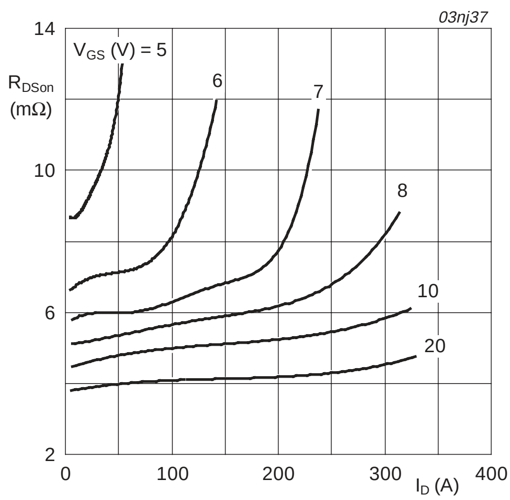
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



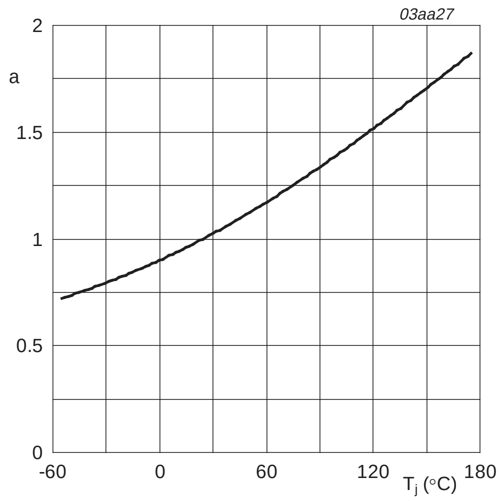
T_j = 25 °C; I_D = 30 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



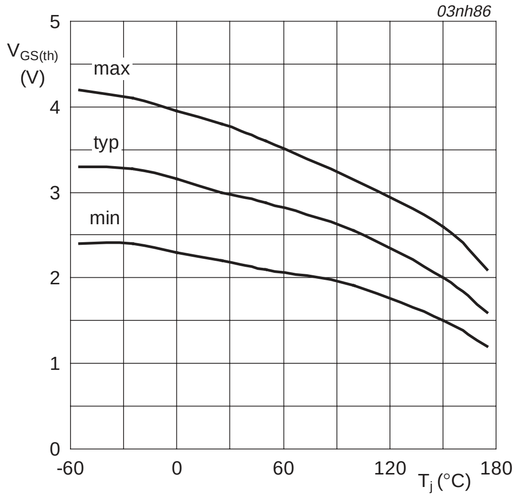
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



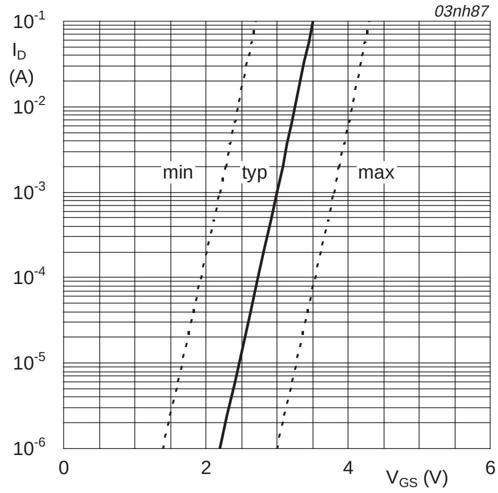
$$a = \frac{R_{DSon}}{R_{DSon(25\ ^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



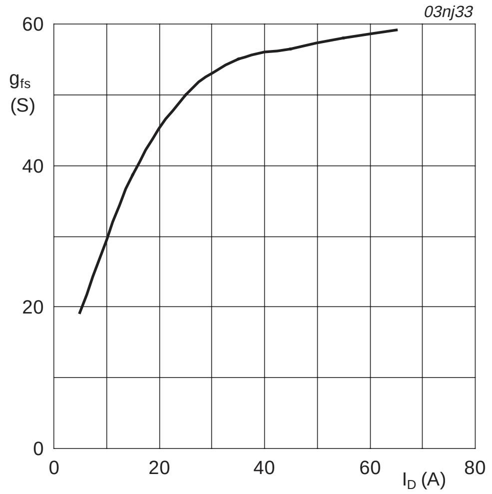
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



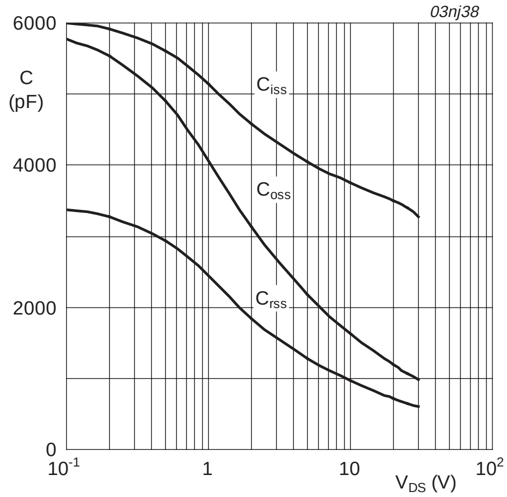
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage



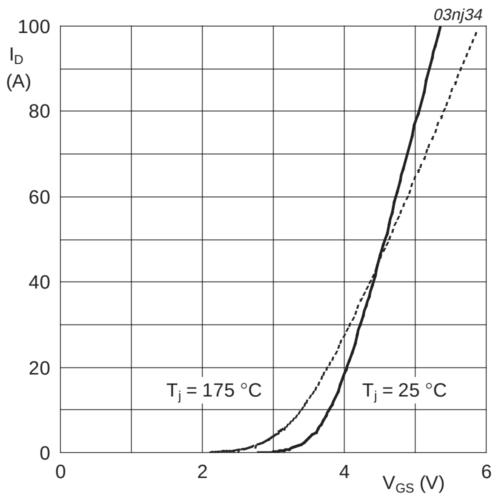
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values



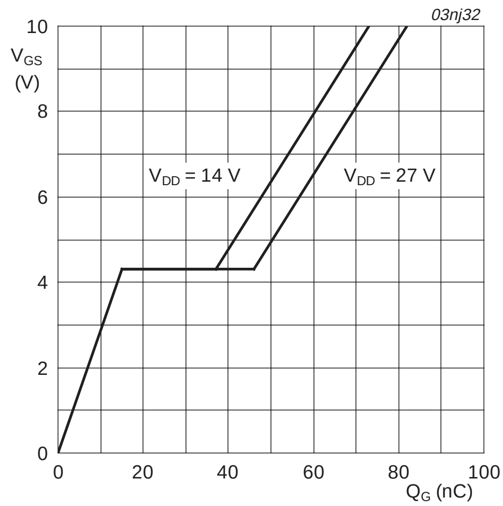
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



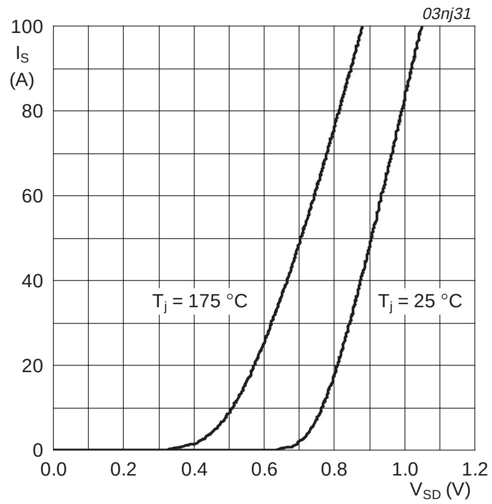
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



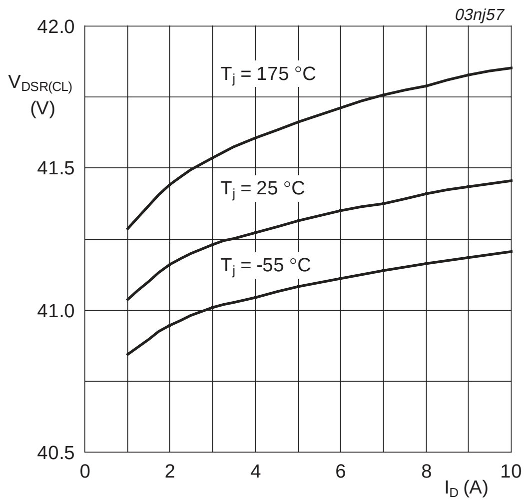
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



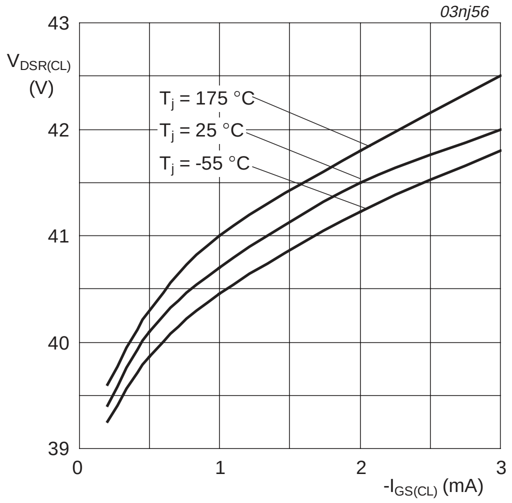
V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$I_{GD(CL)} = -2$ mA

Fig 16. Drain-source clamping voltage as a function of drain current; typical values



$I_D = 10$ A

Fig 17. Drain-source clamping voltage as a function of gate-source clamping current; typical values

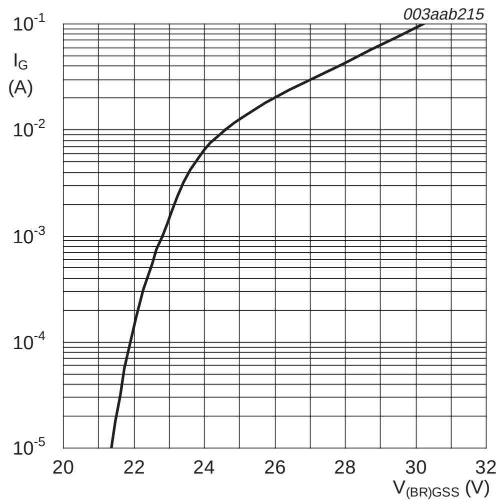
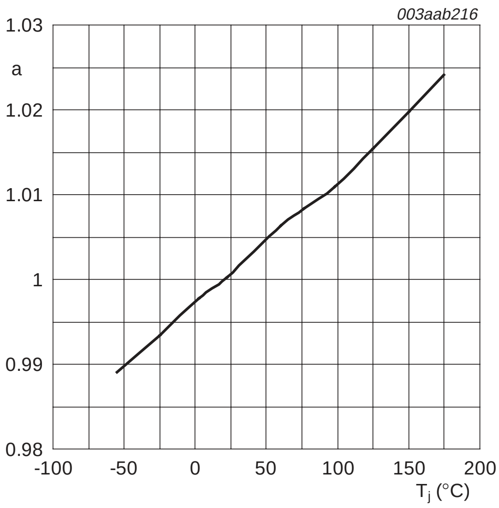


Fig 18. Source-gate clamping current as a function of source-gate clamping voltage; typical values

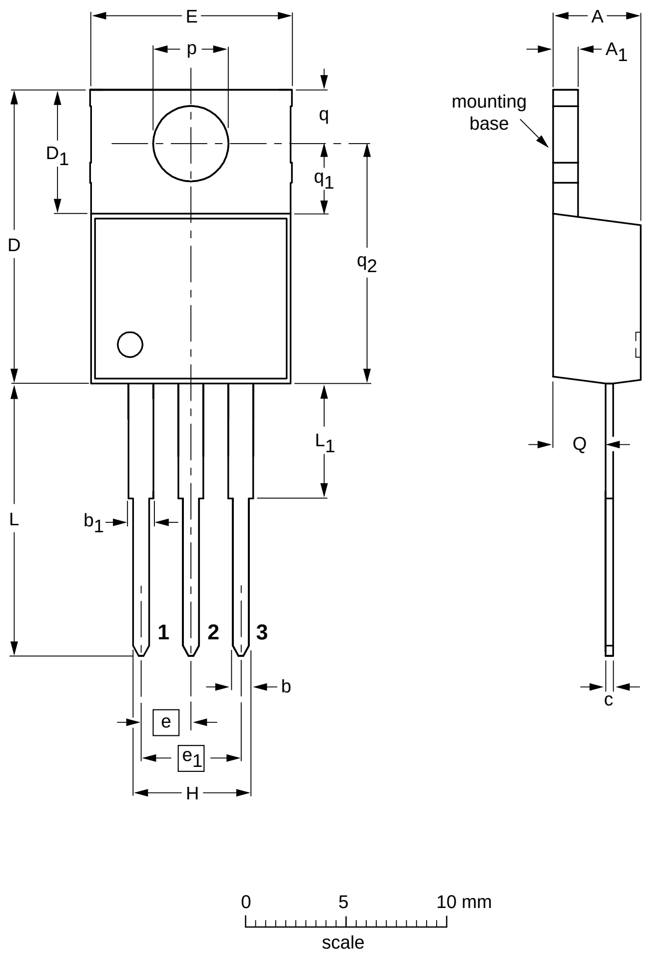


$$a = \frac{V_{(BR)GSS}}{V_{(BR)GSS(25\ ^{\circ}C)}}$$

Fig 19. Normalized source-gate clamping voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads **SOT78C**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	e_1	H	L	L_1	p	Q	q	q_1	q_2
mm	4.58 4.31	1.33 1.21	0.87 0.76	1.33 1.21	0.44 0.33	15.07 14.80	6.47 6.22	10.40 10.00	2.64 2.44	5.16 5.00	6.03 5.76	14.00 13.50	6.10 5.58	3.90 3.78	2.72 2.40	2.95 2.69	3.80 3.42	12.40 12.00

Notes

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78C		3-lead TO-220				~~01-12-11~~ 03-01-21

Fig 20. Package outline SOT78C (TO-220)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BUK7L06-34ARC_4	20051213	Product data sheet	-	-	BUK7L06_34ARC-03
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Figure 18 and Figure 19 added.				
BUK7L06_34ARC-03	20031203	Product data sheet	-	9397 750 12162	BUK7L06_34ARC-02
Modifications:	• Avalanche ruggedness parameter description in limiting values changed from: ‘non-repetitive drain-source avalanche energy’ to ‘non-repetitive drain-source clamp energy’.				
BUK7L06_34ARC-02	20030521	Product data sheet	-	9397 750 11471	BUK7L06_34ARC-01
Modifications:	• Typical values of I_{DSS} added to characteristics table.				
BUK7L06_34ARC-01	20030414	Product data sheet	-	9397 750 11177	

9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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14. Contents

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