

THIS SPEC IS OBSOLETE

Spec No: 38-07522

Spec Title: CY25023 SPREAD SPECTRUM CLOCK GENERATOR 7FOR EMI REDUCTION

Sunset Owner: Christopher Martin (CXQ)

Replaced by: None



CY25023

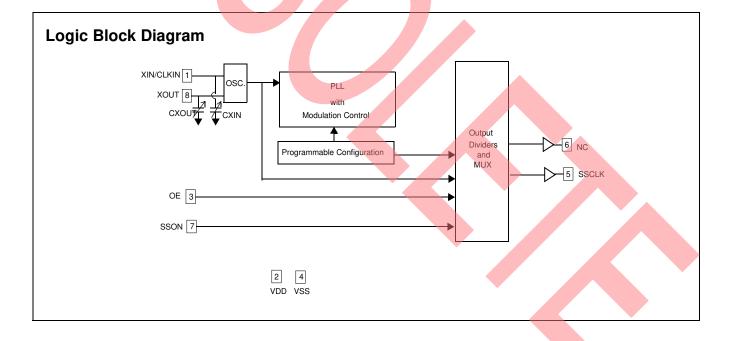
Spread Spectrum Clock Generator for EMI Reduction

Features

- SSCLK frequency: 52.0 MHz
- Spread spectrum output with nominal 31.5 kHz modulation frequency
 Center spread: ±1.0%
- Input frequency
 External clock or crystal: 16.384 MHz
- Integrated phase-locked loop (PLL)
- Low cycle to cycle jitter
- 3.3V operation
- Spread spectrum on and off function
- Output enable function

Benefits

- Services most PC peripherals, networking, and consumer applications.
- Provides electromagnetic interference (EMI) reduction, to meet regulatory agency electromagnetic compliance (EMC) requirements.
- Eliminates the need for expensive and difficult to use overtone crystals.
- Internal PLL to generate up to 200 MHz output. Able to generate custom frequencies from an external crystal or a driven source.
- Suitable for most PC, consumer, and networking applications.
- Application compatibility in standard and low power systems.
- Provides ability to enable or disable spread spectrum with an external pin.
- Enables output clocks to High-Z state.



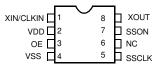
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Pin Configurations

Figure 1. CY25023, 8-Pin SOIC



Pin Description

Pin	Name	Description		
1	XIN/CLKIN	Reference Crystal or Clock Input (16.384 MHz)		
2	VDD	3.3V Voltage Supply		
3	OE	Dutput Enable Pin: Active High. If OE = 1, SSCLK is enabled.		
4	VSS	GND		
5	SSCLK	Spread Spectrum Clock Output (52.0 MHz, ±1.0% center spread)		
6	NC	No Connect		
7	SSON	Spread Spectrum Control. 1 = spread on, 0 = spread off.		
8	XOUT	Crystal Output. Leave this pin floating if external clock is used.		

Table 1. Spread Spectrum Table

Part Number		Spread Percentage
CY25023SC-1		±1.0%



Absolute Maximum Condition

Supply Voltage (VDD)	0.5 to +7.0V
DC Input Voltage	. –0.5V to V _{DD} +0.5
Storage Temperature (Non-Condensing)	–55°C to +125°C
Junction Temperature	. –40°C to +125°C

Data Retention at Tj=125°C	.>10 years
Package Power Dissipation	350 mW
Static Discharge Voltage (per MIL-STD-883, Method 3015)	<u>></u> 2000V

Recommended Operating Conditions

Parameter	Description	Min	Тур	Max	Unit
V _{DD}	Supply Voltage	3.13	3.30	3.45	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance at Pin 6			15	pF
XIN/CLKIN	External Reference, Crystal or Clock Input		16.384		MHz
F _{SSCLK}	SSCLK Output Frequency, C _{LOAD} = 15 pF		52.0		MHz
SS%	Spread Spectrum, CY25023SC-1		±1.0		%
T _{PU}	Power Up Time—for all VDDs to reach minimum specified voltage (power ramp must be monotonic)	0.05		500	ms

DC Electrical Specifications

rrent age ge ent, pins	$\begin{split} & V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V \text{ (source)} \\ & V_{OL} = 0.5, V_{DD} = 3.3V \text{ (sink)} \\ & \text{CMOS levels, 70% of } V_{DD} \\ & \text{CMOS levels, 30\% of } V_{DD} \\ & V_{in} = V_{DD} \end{split}$	12 12 0.7V _{DD}	24 24	0.3V _{DD}	mA mA V V
age ge ent, pins	CMOS levels, 70% of V _{DD} CMOS levels, 30% of V _{DD}	. –	24		V
ge ent, pins	CMOS levels, 30% of V _{DD}	0.7V _{DD}			
ent, pins					V
pins	V _{in} =V _{DD}			1.0	
ant				10	μA
ent, pins	V _{in} =V _{SS}			10	μA
e Current	Three-state output, OE = 0	-10		10	μA
Pin 1 and Pin 8			22		pF
ice at Pin 3 and	Input pins excluding XIN and XOUT		5	7	pF
	$V_{DD} = 3.45V$, Fin = 16.384 MHz, SSCLK = 52.0 MHz, $C_{LOAD} = 15 \text{ pF}$, OE = SSON = V_{DD}		30	40	mA
		V _{DD} = 3.45V, Fin = 16.384 MHz, SSCLK = 52.0 MHz, C _{LOAD} = 15 pF, OE = SSON = V _{DD}	$V_{DD} = 3.45V$, Fin = 16.384 MHz, SSCLK = 52.0 MHz, C _{LOAD} = 15 pF, OE = SSON = V _{DD}	V _{DD} = 3.45V, Fin = 16.384 MHz, SSCLK = 52.0 MHz, C _{LOAD} = 15 pF, OE =	$V_{DD} = 3.45V, Fin = 16.384 \text{ MHz}, \\ SSCLK = 52.0 \text{ MHz}, C_{LOAD} = 15 \text{ pF}, OE = \\ SSON = V_{DD}$

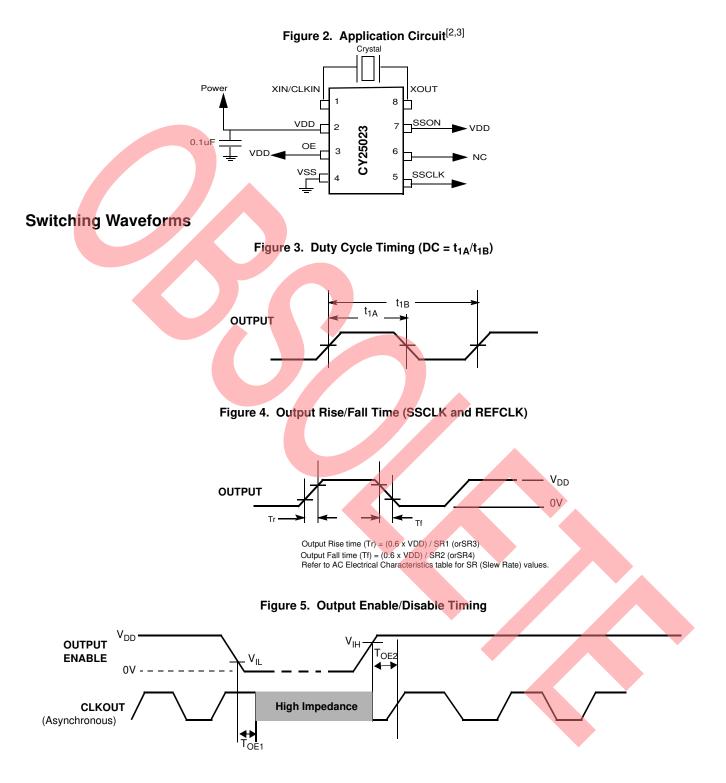
AC Electrical Specifications^[1]

Parameter	Description	Condition	Min	Тур	Max	Unit
DC	Output Duty Cycle	SSCLK, measured at VDD/2	45	50	55	%
SR1	Rising Edge Slew Rate	SSCLK from 20% to 80% of V _{DD}	0.7	1.1	1.5	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 80% to 20% of V _{DD}	0.7	1.1	1.5	V/ns
F _{MOD}	Frequency Modulation	SSON = 1	30.0	31.5	33.0	kHz
tj1	Peak Cycle to Cycle Jitter. SSCLK pin.	SSCLK = 52.0 MHz. Spread on		100	200	ps
T ₁₀	PLL Lock Time	Time from VDD minimum voltage to valid output frequencies		3	5	ms
T _{OE1}	Output Disable time (pin3 = OE)	Time from falling edge on OE to stopped outputs, (Asynchronous)		150	300	ns
T _{OE2}	Output Enable Time (pin3 = OE)	Time from rising edge on OE to outputs at a valid frequency, (Asynchronous)		150	300	ns

Note

1. Guaranteed by Characterization, not 100% tested.





Notes

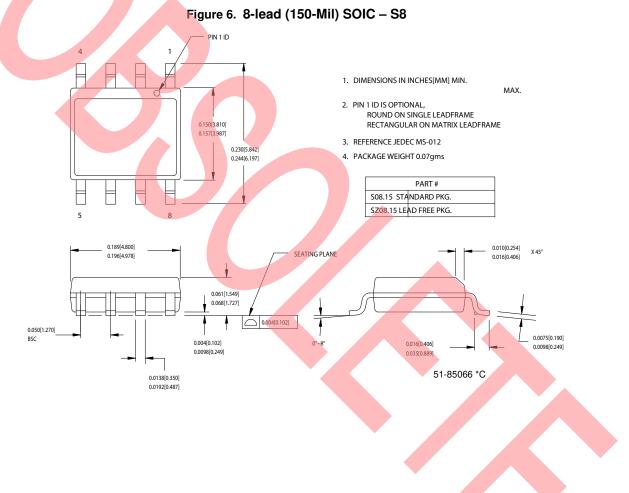
- IF an external clock is used, apply the clock to CLKIN(pin1) and leave XOUT(pin8) floating (unconnected).
 If SSON(pin7) is LOW(V_{SS}), the frequency modulation will be stopped on SSCLK pin(pin5)



Ordering Information

Part Number	Package Type	Product Flow
CY25023SXC-1 ^[4]	8-pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25023SXC-1T ^[4]	8-pin Small Outline Integrated Circuit (SOIC) – Tape and Reel	Commercial, 0 to 70°C
CY25023KSXC-1	8-pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25023KSXC-1T	8-pin Small Outline Integrated Circuit (SOIC) – Tape and Reel	Commercial, 0 to 70°C

Package Drawing and Dimensions





Document History Page

Document Title: CY25023 Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07522						
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change		
**	124268	CKN	See ECN	New Data Sheet		
*A	2505007	AESA	See ECN	Updated template and package diagram. In ordering information table, replaced non-Pb-free part numbers CY25023SC-1 and CY25023SC-1T with Pb-free part numbers CY25023SXC-1 and CY25023SXC-1T. Added Note "Not recommended for new designs." Added part number CY25023KSXC-1, and CY25023KSXC-1T.		
*В	2908854	CDQ	04/08/10	Inactive parts. Obsolete datasheet.		

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