OPT8320 3D Time-of-Flight Sensor

1 Features

- Imaging Array:
  - 80 × 60 Array
  - 1/6” Sensor Format
  - Pixel Pitch: 30 µm
  - Frame Rate: Scalable Up to 1000-FPS Depth Output Rate with an Internal Raw Rate of 4000 FPS
- Optical Properties:
  - Responsivity: 0.35 A/W at 850 nm
  - Demodulation Contrast: 70% at 50 MHz
  - Demodulation Frequency: 10 MHz to 100 MHz
- Output Interface:
  - Digital Video Port (DVP): 8 Data Lanes, HD and VD Pins, and Clock
  - Synchronous Serial Interface (SSI): 1 Data Lane, Clock, and Chip Select
- Timing Generator:
  - Sensor Addressing Engine
  - Modulation Control
  - De-Aliasing
  - Master, Slave Sync Operation
  - High Dynamic Range Operation
- Depth Engine:
  - Pixel Binning
  - De-Aliasing
  - Histogram
  - Calibration
- Power Supply:
  - 3.3-V I/O, Analog
  - 1.8-V Analog, Digital, I/O
  - 1.8-V Demodulation (Typical)
- Optimized Optical Package (COG-56):
  - 8.03 mm × 5.32 mm × 0.745 mm
  - Integrated Optical Band-Pass Filter (830 nm to 867 nm)
  - Optical Fiducials for Easy Alignment
- Built-In Illumination Driver for Low-Power Applications
- Operating Temperature: 0°C to 70°C

2 Applications

- Depth Sensing:
  - Location and Proximity Sensing
  - 3D Scanning
  - 3D Machine Vision
  - Security and Surveillance
  - Gesture Controls
  - Augmented and Virtual Reality

3 Description

The OPT8320 time-of-flight (ToF) sensor is part of the TI 3D ToF image sensor family. The device is a high-performance, highly-integrated, complete system-on-chip (SoC) for array depth sensing, consisting of a versatile timing generator (TG), an optimally designed analog-to-digital converter (ADC), a depth engine, and an illumination driver.

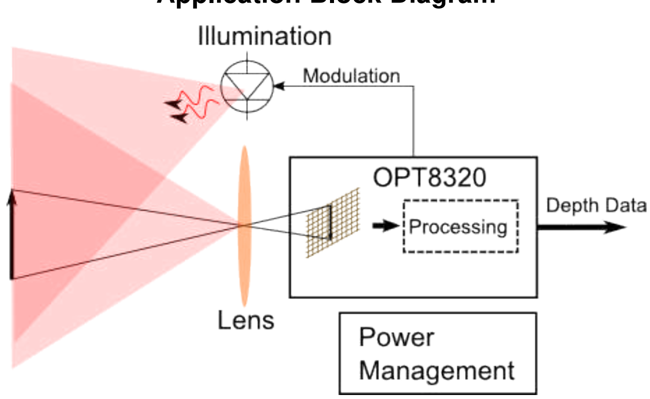
The programmability of the built-in TG offers the flexibility to optimize for various depth-sensing performance metrics [such as power, motion robustness, signal-to-noise ratio (SNR), and ambient cancellation]. The built-in depth engine computes the depth data from the digitized sensor data. In addition to the phase data, the depth engine provides auxiliary information consisting of amplitude, ambient, and flags for each pixel and the full-array statistical information in the form of a histogram.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT8320	COG (56)	8.03 mm x 5.32 mm x 0.745 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Block Diagram



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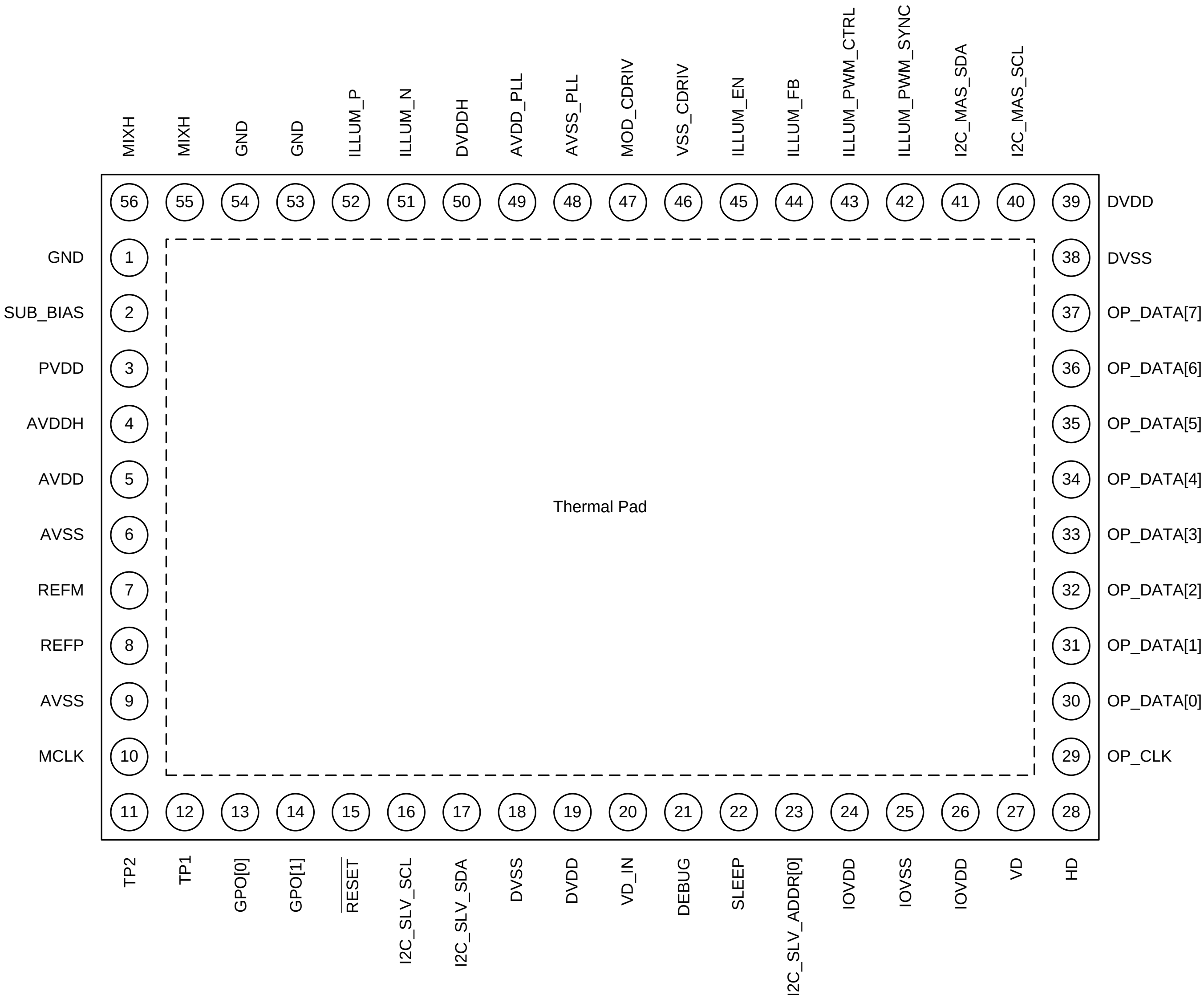
4 Revision History

DATE	REVISION	NOTES
December 2015	*	Initial release.

5 Pin Configuration and Functions

NBP Package
56-Pin COG
Top View, Not to Scale



Pin Functions

PIN		I/O	I/O VOLTAGE DOMAIN	DESCRIPTION
NAME	NO.			
AVDD	5	Power	—	Analog 1.8-V supply
AVDD_PLL	49	Power	—	Analog 1.8-V PLL supply
AVSS_PLL	48	Power	—	Analog PLL ground
AVDDH	4	Power	—	Analog 3.3-V supply
AVSS	6, 9	Power	—	Analog ground
DEBUG	21	Bidirectional	IOVDD	Debug port. Pullup to IOVDD with a 10-kΩ resistor.
DVDD	19, 39	Power	—	Digital 1.8-V supply
DVDDH	50	Power	—	Digital 3.3-V supply
DVSS	18, 38	Power	—	Digital ground
GND	1, 53, 54	Power	—	Connect to ground
GPO[0]	13	Output	IOVDD	General-purpose output 0
GPO[1]	14	Output	IOVDD	General-purpose output 1
HD	28	Output	IOVDD	Indicates the row boundary
I2C_MAS_SCL	40	Output	IOVDD	Host I^2C clock output
I2C_MAS_SDA	41	Bidirectional	IOVDD	Host I^2C data
I2C_SLV_ADDR[0]	23	Input	IOVDD	I^2C address bit 0
I2C_SLV_SCL	16	Input	IOVDD	Slave I^2C interface clock input
I2C_SLV_SDA	17	Bidirectional	IOVDD	Slave I^2C Interface data
ILLUM_EN	45	Output	DVDDH	Illumination enable
ILLUM_FB	44	Input	DVDDH	Feedback signal for illumination power control
ILLUM_N	51	Bidirectional	DVDDH	Illumination modulation signal
ILLUM_P	52	Bidirectional	DVDDH	Illumination modulation signal
ILLUM_PWM_CTRL	43	Output	DVDDH	PWM signal for illumination power control
ILLUM_PWM_SYNC	42	Output	DVDDH	PWM signal for illumination power control
IOVDD	24, 26	Power	—	IO voltage 1.8 V, 3.3 V
IOVSS	25	Power	—	IO ground
MCLK	10	Input	IOVDD	Main clock input for the device
MIXH	55, 56	Power	—	Modulation voltage power pin
MOD_CDRIV	47	Output	—	Illumination current driver
OP_CLK	29	Output	IOVDD	CMOS data bus clock output
OP_DATA[0]	30	Output	IOVDD	CMOS data out bit 0
OP_DATA[1]	31	Output	IOVDD	CMOS data out bit 1
OP_DATA[2]	32	Output	IOVDD	CMOS data out bit 2
OP_DATA[3]	33	Output	IOVDD	CMOS data out bit 3
OP_DATA[4]	34	Output	IOVDD	CMOS data out bit 4
OP_DATA[5]	35	Output	IOVDD	CMOS data out bit 5
OP_DATA[6]	36	Output	IOVDD	CMOS data out bit 6
OP_DATA[7]	37	Output	IOVDD	CMOS data out bit 7
PVDD	3	Power	—	Pixel 3.3-V supply
REFM	7	Analog input	—	Connect REFM to GND
REFP	8	Analog output	—	ADC reference. Connect a 10-nF capacitor between REFP and REFM.
$\overline{\text{RESET}}$	15	Input	IOVDD	Reset; active low
SLEEP	22	Input	IOVDD	Power-down pin
SUB_BIAS	2	Power	—	Negative bias voltage
Thermal pad		Power	—	Exposed thermal pad. Do not solder.

Pin Functions (continued)

PIN		I/O	I/O VOLTAGE DOMAIN	DESCRIPTION
NAME	NO.			
TP1	12	Passive	IOVDD	Test point 1
TP2	11	Passive	IOVDD	Test point 2
VD	27	Output	IOVDD	Indicates the frame boundary
VD_IN	20	Input	IOVDD	External sync input
VSS_CDRIV	46	Power	—	Illumination current driver ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
IOVDD	Digital I/O supply	–0.3	4.0	V
AVDDH	Analog supply	–0.3	4.0	V
DVDDH	Digital I/O supply	–0.3	4.0	V
PVDD	Pixel supply	–0.3	4.0	V
AVDD	Analog supply	–0.3	2.2	V
VMIXH	Mix supply	–0.3	2.5	V
DVDD	Digital supply	–0.3	2.2	V
AVDD_PLL	PLL supply	–0.3	2.2	V
V_I	Input voltage at input pins	–0.3	VCC + 0.3[2]	V
T_J	Operating junction temperature	0	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VCC refers to the I/O bank voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IOVDD	Digital I/O supply	1.7	1.8 to 3.3	3.6	V
AVDDH	Analog supply	3.0	3.3	3.6	V
DVDDH	Digital I/O supply	3.0	3.3	3.6	V
PVDD	Pixel supply	2.4	3.3	3.6	V
AVDD	Analog supply	1.7	1.8	1.9	V
VMIXH	Mix supply	0.8	1.5	2.0	V
DVDD	Digital supply	1.7	1.8	1.9	V
AVDD_PLL	PLL supply	1.7	1.8	1.9	V
V_{DRV}	MOD_CDRIV pin voltage	0.7		3.3	V
T_A	Operating ambient temperature	0		70	°C

6.4 Thermal Information

THERMAL METRIC[1]			OPT8320 NBP (COG) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Without underfill	93.4	°C/W
		With underfill	44.0	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		61.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter		7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	Without underfill	61.4	°C/W
		With underfill	11.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

all specifications at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.8 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 20%, system clock frequency = 24 MHz, V_{IOVDD} = 1.8 V, modulation frequency = 48 MHz, quads = 4, sub-frames = 4, frame-rate = 30 FPS, and 850-nm illumination (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SENSOR						
V	Rows				60	Rows
H	Columns				80	Columns
P_P	Pixel pitch			30		µm
ILLUMINATION DRIVER						
I_{DRV}	Max built-in illumination driver current			150		mA
f_{DRV}	Max Built-in illumination driver frequency			100		MHz
ILLUMINATION POWER CONTROL						
	Minimum pulse duration			10.4		ns
	Starting duty cycle			50%		
POWER (Normal Operation)						
I_{AVDD_PLL}	PLL supply current			4		mA
I_{AVDD}	Analog supply current	Without dynamic power-down		20.7		mA
		With dynamic power-down		6.7		
I_{DVDDH}	3.3-V digital supply current			0.3		mA
I_{AVDDH}	3.3-V analog supply current	Without dynamic power-down		5.5		mA
		With dynamic power-down		1.5		
I_{PVDD}	Pixel VDD current			0.5		mA
I_{VMIXH}	Demodulation current	10% integration duty cycle		56		mA
		100% integration duty cycle		560		
I_{IOVDD}	I/O supply current (CMOS mode)			4.2		mA
I_{DVDD}	Digital supply current			19.7		mA
POWER (Standby)						
I_{IOVDD}	I/O supply current			1		mA
I_{AVDD_PLL}	PLL supply current			100		µA
I_{AVDD}	Analog supply current			1		mA
I_{DVDD}	Digital supply current			4		mA
I_{DVDDH}	3.3-V digital supply current			50		µA
I_{AVDDH}	3.3-V analog supply current			200		µA
I_{VMIXH}	Demodulation current			0		mA
I_{PVDD}	Pixel VDD current			100		µA

Electrical Characteristics (continued)

all specifications at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.8 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 20%, system clock frequency = 24 MHz, V_{IOVDD} = 1.8 V, modulation frequency = 48 MHz, quads = 4, sub-frames = 4, frame-rate = 30 FPS, and 850-nm illumination (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INPUTS/OUTPUTS						
V_{IH}	Input high-level threshold		0.7 × VCC (1)			V
V_{IL}	Input low-level threshold				0.3 × VCC (1)	V
V_{OH}	Min Output high level	I_{OH} = –2 mA		VCC (1) – 0.45		V
		I_{OH} = –8 mA		VCC (1) – 0.5		
V_{OL}	Max Output low level	I_{OL} = 2 mA		0.35		V
		I_{OL} = 8 mA		0.65		
I_I	Input pin leakage current	Pins with pullup, pulldown resistor			±50	µA
		Pins without pullup, pulldown resistor			±10	
C_I	Input capacitance			5		pF
I_{OH}	Max output current high level			10		mA
I_{OL}	Max output current low level			10		mA

(1) VCC is equal to IOVDD or DVDDH, based on the I/O bank listed in the table.

6.6 Timing Requirements

	MIN	NOM	MAX	UNIT
MCLK duty cycle	48%		52%	
MCLK frequency		24		MHz
VD_IN pulse duration	2 × MCLK period			
$\overline{\text{RESET}}$ low pulse duration (reset)	100			ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted); V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, and V_{IOVDD} = 1.8 V

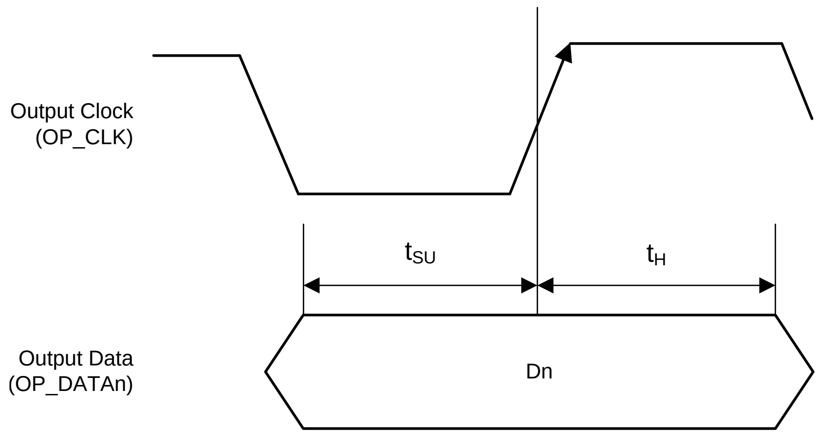
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARALLEL CMOS MODE (V_{IOVDD} = 1.8 V)						
t_{SU}	Data setup time	Data valid to zero crossing of CLKOUT		18.4		ns
t_H	Data hold time	Zero crossing of CLKOUT to data becoming invalid		21.1		ns
t_{FALL}, t_{RISE}	Data fall time, data rise time	Rise time measured from 30% to 70% of IOVDD		1.75		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time measured from 30% to 70% of IOVDD		1.72		ns
PARALLEL CMOS MODE (V_{IOVDD} = 3.3 V)						
t_{SU}	Data setup time	Data valid to zero crossing of CLKOUT		18.3		ns
t_H	Data hold time	Zero crossing of CLKOUT to data becoming invalid		21.4		ns
t_{FALL}, t_{RISE}	Data fall time, data rise time	Rise time measured from 30% to 70% of IOVDD		1.32		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time	Rise time measured from 30% to 70% of IOVDD		1.39		ns

6.8 Optical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Glass side			Top		Side
	Passband (50% relative transmittance[1])	0° incident angle		813 to 893		nm
		30° incident angle		798 to 877		nm
	Passband (90% relative transmittance[1])	0° incident angle		830 to 881		nm
		30° incident angle		838 to 867		nm
AOI	Recommended angle of incidence		0		35	Degrees
	Maximum absolute transmittance	0° incident angle		87.34% at 863		nm
		30° incident angle		81.89% at 855		nm

(1) Relative transmittance is a ratio of transmittance to maximum absolute transmittance at the same angle of incidence.



NOTE: In SSI output mode, clock polarity is inverted when compared to DVP mode.

Figure 1. Output Block Timing Diagram

6.9 Typical Characteristics

all specifications at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.8 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 20%, system clock frequency = 24 MHz, modulation frequency = 48 MHz, quads = 4, sub-frames = 4, frame-rate = 30 FPS, and 850-nm illumination (unless otherwise noted)

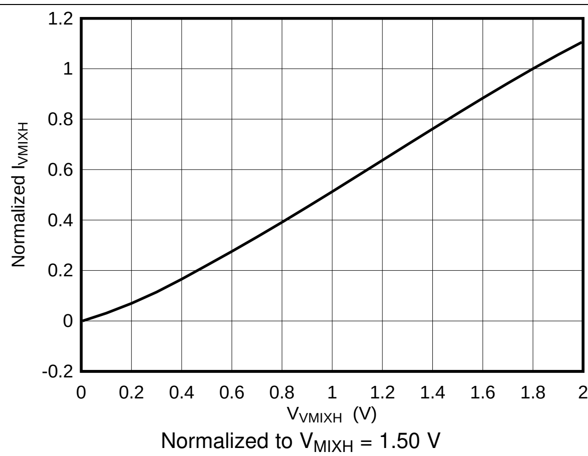


Figure 2. Normalized V_{MIXH} Supply Current vs V_{MIXH} Supply Voltage

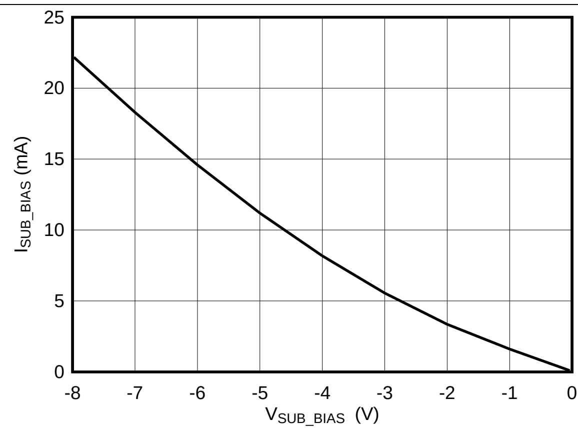


Figure 3. V_{SUB_BIAS} Supply Current vs V_{SUB_BIAS} Supply Voltage

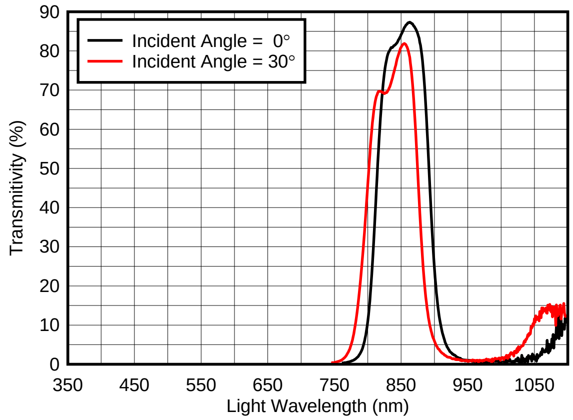


Figure 4. Optical Transitivity vs Wavelength

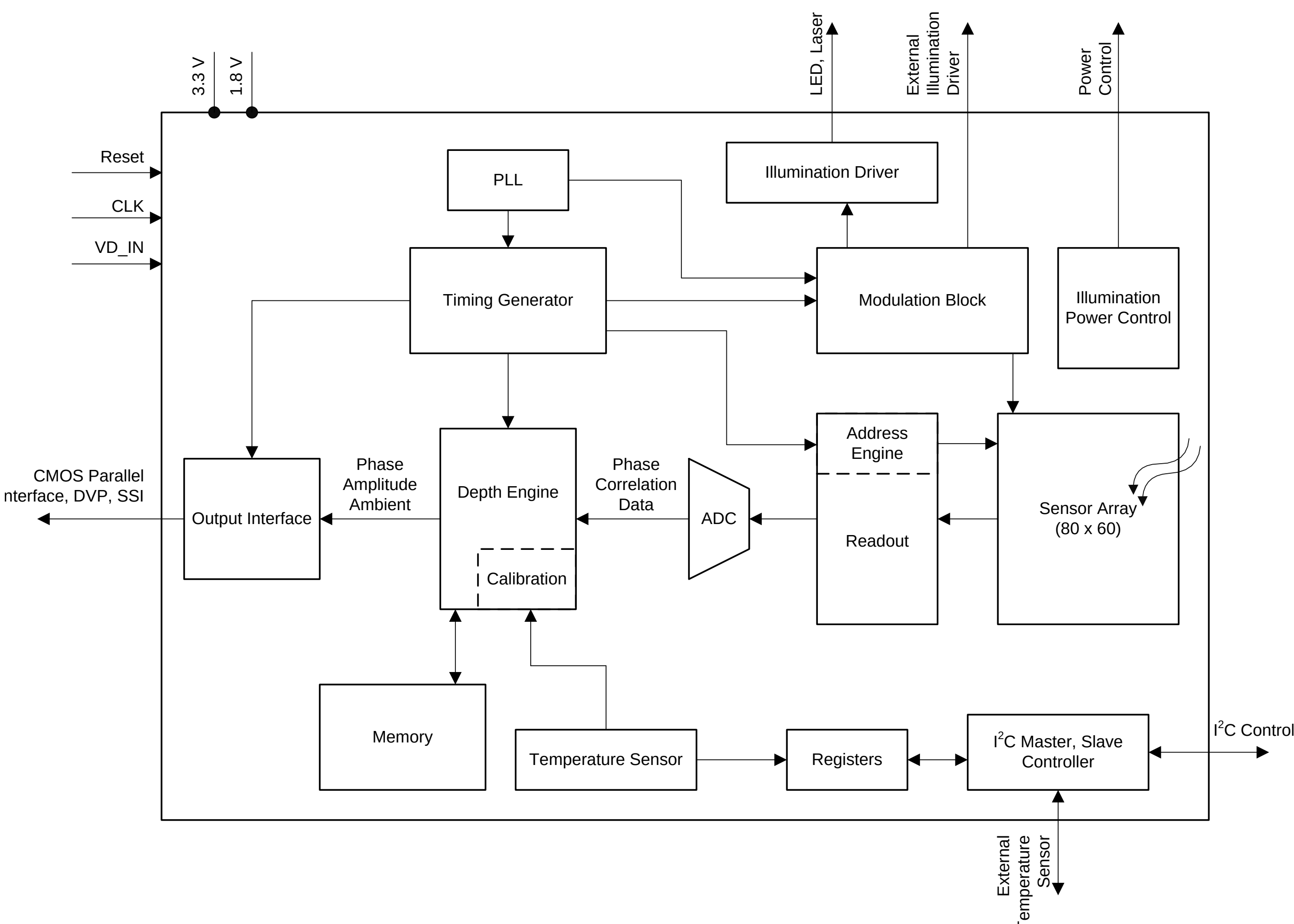
7 Detailed Description

7.1 Overview

The OPT8320 system-on-chip (SoC) has the following blocks:

- Timing generator: generates the sequencing signals for the sensor, illumination, and depth processor
- Sensor: the pixel array
- Addressing engine
- Analog-to-digital converter (ADC)
- Modulation block
- Illumination driver
- Depth engine: calculates phase and amplitude
- Internal memory for depth computation
- Illumination power control
- Output data interface module
- I²C slave for configuring the device registers via the host processor
- I²C master for temperature sensing

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Timing Generator

The timing generator (TG) generates the timing sequence for each frame. The TG includes frame rate control, quad sequencing, and integration time control.

7.3.1.1 Basic Frame Structure

Each frame is divided into sub-frames used for internal averaging, as shown in Table 1.

Table 1. Frame Structure

FRAME				
Sub-frame 1	Sub-frame 2	…	Sub-frame n	Frame dead time

Each sub-frame is divided into quads, as shown in Table 2. Each quad can have a different phase between the illumination and sensor modulation signals.

Table 2. Sub-Frame Division

SUB-FRAME				
Quad 1	Quad 2	Quad 3	…	Quad n

Each quad is further split into four stages, as shown in Table 3. These stages are described in Table 3.

Table 3. Quad Stages

QUAD			
Reset	Integration	Readout	Quad dead time

The description of the quad stages is given in Table 4.

Table 4. Quad Stage Descriptions

QUAD STAGE	DESCRIPTION
Reset	The sensor is reset to clear the accumulated signal
Integration	The pixel array and illumination are modulated by the modulation block. The sensor captures the raw time-of-flight (ToF) signal.
Readout	The raw pixel data in the selected region of interest is readout from the sensor on to the ADC and then by the depth engine.
Dead	The sensor is inactive. The ADC enters a low-power mode.

7.3.1.2 System Clock

The input clock to the system must be 24 MHz. By default, the TG functions at the same frequency as the input frequency. Therefore, the system clock frequency (SYS_CLK_FREQ) is equal to the input frequency at the MCLK pin.

7.3.1.3 Frame Rate Control and Sub-Frames

The OPT8320 supports master and slave modes of operation for the start of frame timing. The parameters shown in Table 5 control the master and slave behavior.

Table 5. Master and Slave Parameters

PARAMETER	DEFAULT	DESCRIPTION
TG_EN	0	Start the timing generator and, thus, the full chipset operation. 0 = Disable the timing generator 1 = Enable the timing generator
SLAVE_MODE	0	Puts the timing controller in slave mode. The timing controller waits for an external sync through the VD_IN pin for the start of frames. By default, the timing controller is in master mode.
SYNC_MODE	0	Puts the timing controller in SYNC_MODE. The timing controller synchronizes with an external input through the VD_IN pin for the start of frames, but does not depend on the input. If both SLAVE_MODE and SYNC_MODE are enabled, SYNC_MODE takes higher priority. By default, this mode is disabled.
FRAME_SYNC_DELAY	1	The programmable delay between the external VD_IN pulse and the internal start of frame. The delay must be at least one cycle.

In slave mode or sync mode, a positive pulse on the VD_IN pin can be used for synchronization. The pulse must be a minimum of two system clocks cycles wide in order to be recognized correctly, as shown in Figure 5. In slave mode, if another pulse is received before the end of the previous frame, the pulse is ignored. In sync mode, because a pulse can be received by the OPT8320 anytime within a frame, the frame during which the pulse is received is aborted and therefore disruption of output data is possible, resulting in a loss of information.

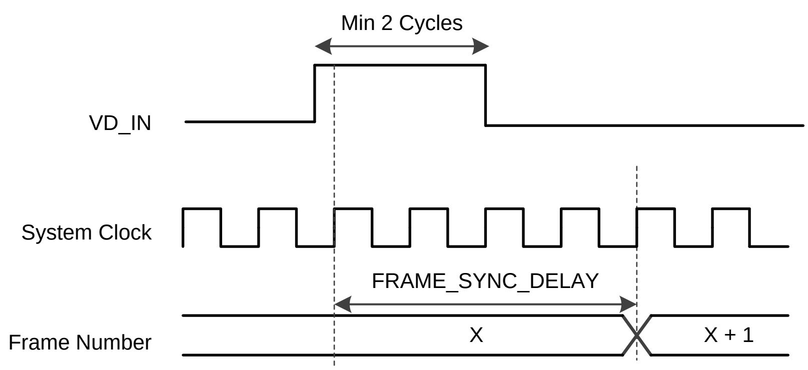


Figure 5. VD_IN Timing Diagram

When the OPT8320 is operated in master mode or sync mode, the frame rate is controlled using the parameters shown in Table 6. In the OPT8320, the number of quads (QUAD_CNT_MAX) are fixed to four. Using the functionality of alternate frames, two kinds of frames are possible with a different set of sub-frames, integration duty cycle, and modulation frequency. The resulting information can be also combined to give out a single de-aliased frame. When alternate frames are enabled, every alternate frame with the different set of timing parameters is called the supplementary frame.

Table 6. Frame Rate Parameters

PARAMETER	DEFAULT	DESCRIPTION
ALT_FRM_EN	0	When set to 1, enables alternate frames with a different set of sub-frames, integration duty cycle, and frequency.
SUB_FRAME_CNT_MAX1	16	Total number of sub-frames in each frame for the base frame. Only values that are powers of 2 are valid. Behavior is unpredictable when set to other values.
SUB_FRAME_CNT_MAX2	4	Total number of sub-frames in each frame for the supplementary frame. Only values that are powers of 2 are valid. Behavior is unpredictable when set to other values.
PIX_CNT_MAX	12500	The number of system clock cycles in one frame divided by the product of QUAD_CNT_MAX and SUB_FRAME_CNT_MAX.
PIX_CNT_MAX_SET_FAILED	0	Read-only flag that indicates if the last setting of the PIX_CNT_MAX value is successful. If the PIX_CNT_MAX is smaller than the minimum size required to accommodate the reset and readout time, PIX_CNT_MAX_SET_FAILED is set.
LUMPED_DEAD_TIME	0	Dead time can be either distributed equally among all quads or can be lumped at the end of each frame. Distributed quad dead time is typically better for phase offset cancellation. Lumped frame dead time is typically better for reducing motion artefacts and power consumption. By default, distributed dead time is used.

Dead time is automatically calculated by the device based on the values of the integration duty cycle and readout time. If LUMPED_DEAD_TIME is set to 0, the dead time for each quad in relation to the number of system clocks is given by Equation 1:

$$\begin{aligned} &Quad\ Dead\ Time = \\ &PIX\_CNT\_MAX \times (1 - Integration\ Duty\ Cycle) - (Sensor\ Reset\ Time + Readout\ Time) \end{aligned} \tag{1}$$

If LUMPED_DEAD_TIME is set to 1, then the dead time for each frame in relation to the number of system clocks is given by Equation 2:

$$\begin{aligned} &Frame\ Dead\ Time = SUB\_FRAME\_CNT\_MAX \times QUAD\_CNT\_MAX \times \\ &\left[PIX\_CNT\_MAX \times (1 - Integration\ Duty\ Cycle) - (Sensor\ Reset\ Time + Readout\ Time)\right] \end{aligned} \tag{2}$$

Sensor reset time is equal to 720 system clock cycles. The readout time is given by Equation 9.

The calculation of PIX_CNT_MAX for when ALT_FRM_EN is 0 is given by Equation 3:

$$PIX\_CNT\_MAX = \frac{SYS\_CLK\_FREQ}{FRAME\_RATE \times QUAD\_CNT\_MAX \times SUB\_FRAME\_CNT\_MAX} \tag{3}$$

When ALT_FRM_EN is set to 1, alternate frames can have different frame times depending on the number of sub-frames (parameters are described in Table 6). Also, in most cases alternate frames are combined to form a single frame either internally or externally. In such cases, the frame rate is given by Equation 4:

$$De\text{-}Aliasing\ Frame\ Rate = SET\_FRAME\_RATE \times \left(\frac{SUB\_FRM\_CNT\_MAX1}{SUB\_FRM\_CNT\_MAX1 + SUB\_FRM\_CNT\_MAX2}\right) \tag{4}$$

7.3.1.4 Integration Time

Integration time is the time that the sensor demodulation and the illumination modulation are active. The configurable parameters are listed in Table 7.

Table 7. Integration Time Parameters

PARAMETER	DEFAULT	DESCRIPTION
INTG_DUTY_CYCLE	13	This parameter controls the ratio of integration time to total frame time.
INTG_DUTY_CYCLE_ SET_FAILED	0	This flag indicates if the INTG_DUTY_CYCLE setting has taken effect. If the INTG_DUTY_CYCLE is not feasible for a given set of conditions, this flag is set. This flag is cleared when a feasible value of INTG_DUTY_CYCLE is programmed. If this flag is set, a lower value of INTG_DUTY_CYCLE must be programmed and the value of the flag checked again. This process must be repeated until the flag clears.

The INTG_DUTY_CYCLE registers allows 64 settings from 0 to 63. The relationship between effective integration duty cycle of the base frame and the register value is given by Equation 5:

$$INTG\_DUTY\_CYCLE = \frac{Integration\ Duty\ Cycle \times 64}{100} \tag{5}$$

Internally, the INTG_DUTY_CYCLE value is clamped to a minimum of 1. Maximum integration duty cycle is given by Equation 6:

$$Maximum\ Integration\ Duty\ Cycle = \frac{PIX\_CNT\_MAX - (Reset\ Time + Readout\ Time)}{PIX\_CNT\_MAX} \tag{6}$$

The INTG_DUTY_CYCLE parameter must be reprogrammed whenever any of the registers related to frame rate control or region of interest are programmed. The related registers are:

- SUB_FRAME_CNT_MAX1
- SUB_FRAME_CNT_MAX2
- PIX_CNT_MAX
- LUMPED_DEAD_TIME
- ROW_START
- COL_START
- ROW_END
- COL_END

When the OPT8320 is in slave mode, the duty cycle still corresponds to the frame length calculated as per the internal registers and not as per the period of the external sync signal. The sync signal period must be large enough to make sure that the frame data are streamed successfully. When the sync signal period is larger than the internal frame period, the actual integration duty cycle is less than the programmed value.

7.3.1.4.1 High Dynamic Range Functionality

When frame alternation is enabled, alternate frames can use different integration times. The supplementary frame integration time is scaled down as compared to the base frame by a factor. The relevant parameters are listed in Table 8.

Table 8. High Dynamic Range Functionality Parameter

PARAMETER NAME	DEFAULT	DESCRIPTION
SUP_FRM_INTG_SCALE	63	Denotes the percentage of INTG_PHASE in the supplementary frame in terms of the base frame. INTG_DUTY_CYCLE2 = INTG_DUTY_CYCLE1 × (SUP_FRM_INTG_SCALE + 1) / 64.

The supplementary frame integration time is given in Equation 7:

$$Supplementary\ Frame\ Integration\ Time = Base\ Frame\ Integration\ Time \times \frac{SUP\_FRM\_INTG\_SCALE + 1}{64} \tag{7}$$

7.3.2 Pixel Array

The pixel array consists of 80 × 60 demodulating pixels. With a 30-µm × 30-µm pixel size, the pixels exhibit excellent dynamic range. The pixels also have a built-in shutter feature that helps in achieving higher ambient robustness. For convenience, either the entire or part of the pixel array can be readout through register configurations.

7.3.2.1 Region of Interest (ROI)

A subset of the sensor array can be readout to enhance frame rate or to reduce the power consumption of the ToF system. An ROI is comprised of a set of row and column limits. The row and column counts start from zero. Both row and column limits can be any of the valid row numbers for the given sensor size. The relevant parameters are listed in Table 9.

Table 9. ROI Parameters

PARAMETER	DEFAULT	DESCRIPTION
ROW_START	0	Start address for the row address bus
COL_START	0	Start address for the column address bus
ROW_END	59	End address for the row address bus
COL_END	79	End address for the column address bus

Sensor readout time is affected by ROI. A minimum row-to-row switching time of half the row readout time is enforced internally. Thus, reducing the column count to less than half of the total number of columns for a given sensor does not lead to a reduction in sensor readout time. For a number of columns greater than the total number of columns divided by 2, use Equation 8:

$$Readout\ Time = Preparation\ Time + \left[(Rows + 1)\times(Cols + 1)\right]$$
$$(Measured\ in\ System\ Clock\ Cycles) \quad (8)$$

For a number of columns less than half of the total number of columns, use Equation 9:

$$Readout\ Time = Preparation\ Time + \left[(Rows + 1)\times(Total\ Cols/2 + 1)\right]$$
$$(Measured\ in\ System\ Clock\ Cycles)$$

where:
- Preparation time = 100 clock cycles (9)

7.3.2.2 Readout Sequence

The readout sequence can be controlled to achieve mirroring along horizontal or vertical axis. The programmable parameters are listed in Table 10.

Table 10. Readout Sequence Parameters

PARAMETER	DEFAULT	DESCRIPTION
ROW_RDOUT_DIR	0	0 = Vertical inversion disabled
		1 = Vertical inversion enabled
COL_RDOUT_DIR	0	0 = Horizontal inversion disabled
		1 = Horizontal inversion enabled

7.3.2.3 Shutter Operation

Shutter operation can be used to control the exposure to ambient light. The shutter switch separates the charge storage node from the pixel charge collection node. The shutter can be programmed to become inactive (switch is on) at the start of integration and become active (switch is off) at the end of integration time to avoid collection of unwanted ambient light during the sensor readout. The behavior of the shutter switch is shown in Table 11.

Table 11. Shutter Operation

OPERATION	QUAD STATE			
	RESET	INTEGRATION	READOUT	QUAD DEAD TIME
State of the shutter software with the shutter operation enabled (default)	On	On	Off	Off
State of the shutter software with the shutter operation disabled	On	On	On	On

The SHUTTER_EN parameter enables or disables the shutter operation. The SHUTTER_EN description is given in Table 12.

Table 12. Shutter Operation Registers

PARAMETER	DEFAULT	DESCRIPTION
SHUTTER_EN	0	Set to 1 to enable shutter operation.

7.3.3 Modulation Block

The OPT8320 modulation block provides the high-frequency demodulation to the pixels as well as the illumination module. The modulation block controls the phase between the modulation signals connected to the pixels and the illumination module from quad to quad.

7.3.3.1 Sensor Output Signals

The phase between illumination modulation and the sensor demodulation signals is stepped automatically as per the quad number illustrated in Figure 6. Because the OPT8320 uses four quads per modulation frequency, the phase is typically stepped between 0º, 90º, 180º, and 270º. The phase stepping sequence of the sensor is programmable through the OPT8320 registers. A different sequence can be enabled for odd and even sub-frames. Also, the phase registers for the base frequency and de-aliasing frequency are separately programmable. The OPT8320 output signals are listed in Table 13.

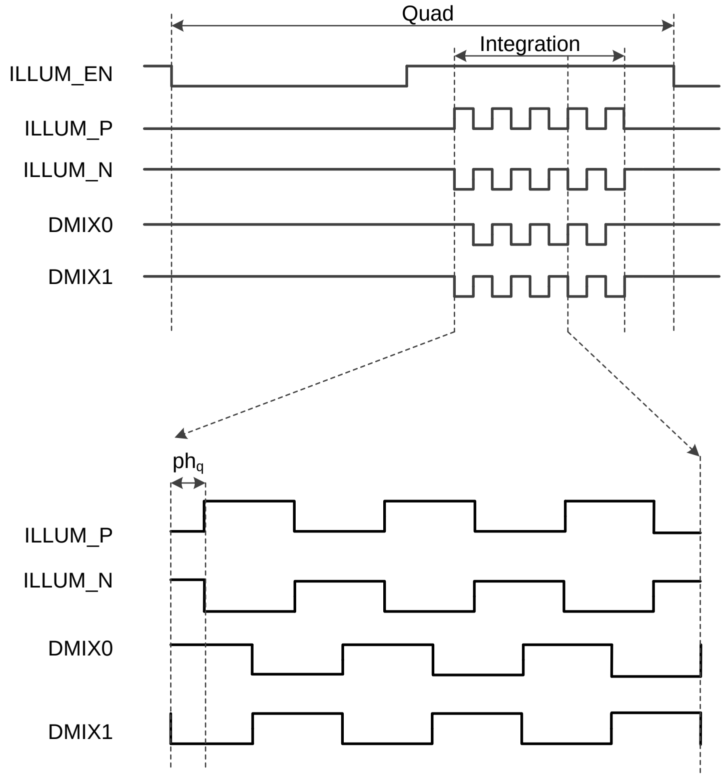


Figure 6. Integration Timing Diagram

Table 13. Sensor Output Signals

PIN NAME	DESCRIPTION
ILLUM_P	High-frequency input to the illumination driver, noninverting. Modulates during integration time. Held low by default during rest of the time.
ILLUM_N	High-frequency input to the illumination driver, inverting. Modulates during integration time. Held high by default during rest of the time.
ILLUM_EN	If an external driver is used for driving the illumination current, this signal can be used to switch the driver between active and standby mode. Normally, this signal is active high just before the integration time and goes low just after the integration time.

The programmable parameters are listed in Table 14 and Table 15.

Table 14. Pin Programmability

PARAMETER	DEFAULT	DESCRIPTION
MODULATION_HOLD	0	Disable modulation during the integration period. Set to 0 for normal operation.
DEMOD_STATIC_POL	0	DC state of illumination pins during the integration period if MODULATION_HOLD = 1.
ILLUM_STATIC_POL	0	DC state of illumination pins during the integration period if MODULATION_HOLD = 1. ILLUM_P = ILLUM_STATIC_POL, ILLUM_N = not (ILLUM_STATIC_POL).
ILLUM_EN_EARLY	0	Activates the illumination enable signal 15 µs before the integration period starts when set to 1.
ILLUM_DC_CORR_DIR	0	Sets the direction of the duty cycle correction for illumination output waveforms. Note that when duty cycle is increased, the ILLUM_P duty cycle increases and the ILLUM_N duty cycle decreases. 0 = Increases duty cycle 1 = Reduces duty cycle
ILLUM_DC_CORR	0	The illumination duty cycle can be corrected in steps of approximately 450 ps. The maximum value of this register is 11 (0Bh), resulting in a total correction of approximately ±5 ns.

Table 15. Phase Sequence Programmability

PARAMETER	DEFAULT	DESCRIPTION
QUAD_HOP_EN	0	Enables a different sequence of quads for odd and even sub-frames
QUAD_HOP_OFFSET	0	The offset of the quad sequence for alternate sub-frames

The relative phase of the illumination modulation with respect to sensor modulation (Ph_q for any quad) can be calculated as shown in Equation 10:

$$Ph_q = 360 \times \frac{Quad\ Number}{QUAD\_CNT\_MAX} \quad (10)$$

Note that the quad number is offset by the quad hop offset for that sub-frame.

The effective quad number = quad number + quad hop offset.

7.3.3.2 Modulation Frequency

The OPT8320 sensor has an internal PLL for generating the base modulation frequency (MOD_F) and the supplementary frame frequency. The formula for calculating the modulation frequency is given in Equation 11:

$$MOD\_F = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N-1)} \times QUAD\_CNT\_MAX \times (1 + MOD\_PS)} \quad (11)$$

The internal VCO frequency is given by Equation 12:

$$VCO\_FREQ = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N-1)}} \quad (12)$$

MOD_M and MOD_N must be chosen to meet the internal VCO frequency range limitation. The internal VCO can operate between 300 MHz and 600 MHz. The PLL block diagram is shown in Figure 7.

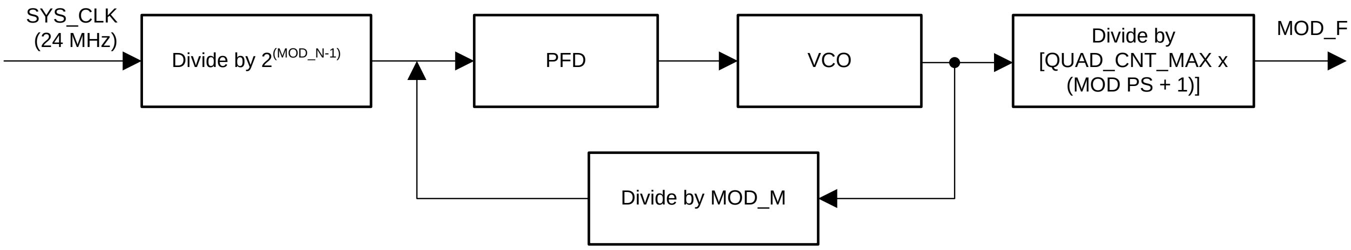


Figure 7. Modulation PLL Block Diagram

To enable accurate setting of the desired modulation frequency, MOD_M is split into an integer and a fractional part. The effective MOD_M is given by Equation 13:

$$Effective\ MOD\_M = MOD\_M + \frac{MOD\_M\_FRAC}{2^{16}} \quad (13)$$

The programmable parameters are listed in Table 16. The default base modulation frequency on start-up is 48 MHz.

Table 16. Programmable Parameters

PARAMETER	DEFAULT	DESCRIPTION
MOD_M	16	VCO multiplier
MOD_M_FRAC	0	VCO multiplier
MOD_N	1	VCO divider
MOD_PS	1	Divider for generation of the base modulation frequency
MOD_PLL_UPDATE	0	Set this bit to 1 and back to 0 for updating any modulation frequency setting.

7.3.4 Depth Engine

The depth engine calculates the phase and amplitude information using the digitized data obtained from the sensor block. The depth engine uses an internal RAM to temporarily store the data obtained and to process data. The data engine has the following features:

- Phase, amplitude calculation
- Binning
- De-aliasing
- Histogram computation
- Phase offset correction
- Temperature correction
- Nonlinearity correction

7.3.4.1 Phase Data

The computed phase for each pixel is proportional to the distance of the corresponding object in the scene. For a phase varying from 0 π to 2 π, the distance varies from 0 to R, where R is the unambiguous range. The equations describing the relationship between phase and distance are given in Equation 14 and Equation 15.

$$d = \frac{Phase \times R}{2\pi} \quad (14)$$

$$R = \frac{C}{2F}$$

where
- C is the speed of light
- F is the modulation frequency (15)

At the output of the depth processor block, the phase of 2 π is typically represented by a full 12-bit code (that is, 2^{12}). If the application requires the distance (in meters) of the points in the scene, this value must be calculated from the OPT8320 output using Equation 16:

$$d = \frac{Phase \times R}{2^{12}} \quad (16)$$

Equation 16 assumes that the phase has no offset. If offset correction is not done within the OPT8320, the formula is as shown in Equation 17:

$$d = \frac{(Phase - Offset) \times R}{2^{12}} \quad (17)$$

7.3.4.2 De-Aliasing

The unambiguous range of a ToF system is defined by the modulation frequency (F). The unambiguous range is given by Equation 18:

$$R = \frac{C}{2F}$$

where
- C is the speed of light in the medium (18)

For example, for a modulation frequency of 50 MHz, R = 3m in open air. If the total range of the application is beyond the unambiguous range for a given modulation frequency, de-aliasing can be enabled to extend the unambiguous range. The OPT8320 employs a dual modulation frequency technique to extend the unambiguous range. Two different frames are used to phase data corresponding to base frequency and supplementary frequency. The supplementary frequency is chosen to be lower than the base frequency and sets the unambiguous range. For example, if the base frequency is F, the supplementary frequency is chosen to be F / 4 to increase the unambiguous range by four times. The data from the two frames can then be combined to obtain the unambiguous phase. To provide a full 16-bit phase after range extension, the flag bits in the data stream are replaced by the MSBs of the de-aliased phase automatically when de-aliasing is enabled.

7.3.4.2.1 Procedure for Enabling De-Aliasing Mode

1. Disable the timing generator by setting the TG_EN parameter to 0.
2. Set the ALT_FRM_EN parameter to enable alternate frames.
3. Set the ALT_FREQ_SEL parameter to select the range extension ratio.
4. Set the phase calibration parameters for each frequency as described in the *Phase Offset Correction* section.
5. Set SUB_FRAME_CNT_MAX1 and SUB_FRAME_CNT_MAX2 for the base and supplementary frames.
6. Set the PIX_CNT_MAX parameter to meet the frame rate requirements.
7. Set INTG_DUTY_CYCLE and SUP_FRM_INTG_SCALE to set the integration time for the base and supplementary frames.

8. Set the DEALIAS_EN parameter to 1 to combine the frames. Note that if the DEALIAS_EN parameter is not set, the base and supplementary frame data are given out as is. If the DEALIAS_EN parameter is set, the base and supplementary frame data are combined to give out de-aliased data and the effective frame rate must be recalculated as per Equation 4.
9. Enable the timing generator using the TG_ENABLE parameter.

7.3.4.3 Binning

Multiple pixel data can be averaged to form a single large pixel data. This feature is useful in cases where the application requires less pixel resolution but needs better phase noise performance. Rows and columns can be binned in powers of 2. The programmable parameters are listed in Table 17.

Table 17. Binning Parameters

PARAMETER	DEFAULT	DESCRIPTION
ROWS_TO_MERGE	0	number of rows to merge for binning = $2^{ROWS\_TO\_MERGE}$
COLS_TO_MERGE	0	Number of columns to merge for binning = $2^{COLS\_TO\_MERGE}$

7.3.4.4 Auxiliary Depth Data

Amplitude data represents the amplitude of the received signal at each pixel. If the amplitude is higher, signal amplitude is higher and thus the phase SNR is higher. The amplitude output value is given by Equation 19:

$$Amplitude = 4\sqrt{2} \times \left(2^{12} \times Signal\ Amplitude \times 0.825\right) \quad (19)$$

where
- the signal amplitude is the amplitude of the single-ended modulating signal (A or B) generated on the pixel in each quad

When binning is enabled, the signal amplitude is the vector sum of the signals of all the binned pixels divided by the nearest power of 2 that is greater than the number of pixels binned together.

Ambient data are an indicator of the non-modulating component of voltage on the pixels. Ambient data are the sum of the ambient light, pixel offsets, and the non-demodulated component of the ToF illumination. The output ambient data values decrease with increase in voltage. Therefore, near-zero values indicate pixel saturation.

The OPT8320 provides masking of data based on the amplitude and single-ended voltage values in a pixel for the purpose of basic filtering. The related parameters are listed in Table 18.

Table 18. Auxiliary Depth Data Parameters

PARAMETER	DEFAULT	DESCRIPTION
AMPLITUDE_THRESHOLD	0	If the amplitude of the pixel is lower than this number, the pixel phase data are set to 000h
IQ_SCALE	0	Left shifts the acquired sensor data by the configured value. The scaling results in an equivalent scaling in amplitude. Care must be taken to avoid bit overflow in the depth engine because this scaling is done before the computation of phase and amplitude.
IQ_SCALE_EN	0	When set to '1', enable scaling of I and Q according to the iq_scale register
SATURATION_THRESHOLD	0	The saturation flag is set if the ambient value of the pixel is less than or equal to this value. Also, pixel phase data are set to 000h.

Flags[3:0] indicate important pixel data reliability parameters. The flags are described in Table 19.

Table 19. Flag Data

FLAG BIT	DEFAULT	DEALIAS_EN = 1
Flag[3]	0 = No pixel saturation 1 = Pixel is saturated	Phase[15]
Flag[2]	Reserved. Set to 0.	Phase[14]
Flag[1]	Frame counter[1]	Phase[13]
Flag[0]	Frame counter[0]	Phase[12]

When de-aliasing is enabled, an additional option to provide flags instead of ambient data is provided using the MV_FLAGS_TO_AMBIENT parameter.

7.3.4.5 Phase Offset Correction

Time delay between sensor modulation and the illumination modulation manifests as phase offset. The offset must be calibrated individually for each system because this delay can vary from one system to another. The measured offset can be programmed into a PHASE_CORR parameter in the OPT8320 registers. The device adds the PHASE_CORR parameter to the computed phase. The programmable parameters are listed in Table 20.

Table 20. Phase Offset Correction Parameters

PARAMETER	DESCRIPTION
PHASE_CORR_1	Phase offset correction for the base frame
PHASE_CORR_2	Phase offset correction for the supplementary frame
DISABLE_OFFSET_CORR	Disables phase offset correction in the device. Phase offset correction is enabled by default.

System delays in the illumination and sensor modulation path can vary differently as a result of temperature variations. This variation leads to a change in the measured phase. To compensate for phase change versus temperature, the OPT8320 uses two programmable temperature coefficients. The built-in temperature sensor in the OPT8320 is used for measuring the ToF sensor temperature, and an external I^2C interface-based temperature sensor is used for measuring the illumination driver temperature. The programmable parameters are listed in Table 21.

Table 21. Temperature Coefficient Parameters

PARAMETER	DESCRIPTION
TILLUM_CALIB	Illumination driver temperature when PHASE_CORR is measured.
TSENSOR_CALIB	Sensor temperature when PHASE_CORR is measured.
COEFF_ILLUM	Phase versus temperature coefficients for the illumination driver for the base frame.
COEFF_SENSOR	Phase versus temperature coefficients for the sensor for the base frame.
DISABLE_TEMP_CORR	Disables phase offset correction resulting from temperature. (Temperature correction is enabled by default.)
CALIB_PREC	Adjusts the precision of temperature correction. Coefficients are scaled by CALIB_PREC. Internal COEFF = [programmed COEFF << (CALIB_PREC – 8)].

Phase correction resulting from temperature variation is calculated by the OPT8320, and is shown in Equation 20:

$$PHASE\_CORR\_TEMP = \frac{COEFF\_ILLUM \times (TILLUM - TILLUM\_CALIB) + COEFF\_SENSOR \times (TSENSOR - TSENSOR\_CALIB)}{Calibration\ Scale}$$

where

- calibration scale is calculated as per Table 21. (20)

When de-aliasing is not used, the final phase value given out by the OPT8320 is calculated by Equation 21:

$$\text{Corrected Phase} = \text{Computed Phase} + PHASE\_CORR\_1 + PHASE\_CORR\_TEMP \quad (21)$$

When de-aliasing is used, phase correction on individual frequency measurements is applied before combining the phase information to compute the final unambiguous phase. The OPT8320 provides separate correction blocks for measurements using each frequency because individual frequency measurements can have different offsets and temperature coefficients. The temperature coefficients for the supplementary frequency are internally computed using the coefficients for the base frequency. When de-aliasing is used, for the purpose of calibration, streaming of individual frequency data can be enabled in place of de-aliased data by setting the DEALIAS_EN parameter to 0.

7.3.5 Output Data Interface

The OPT8320 has a programmable parallel CMOS output interface module that gives an option to interface the device to a wide variety of host processors. The output signals are shown in Figure 8 and listed in Table 22.

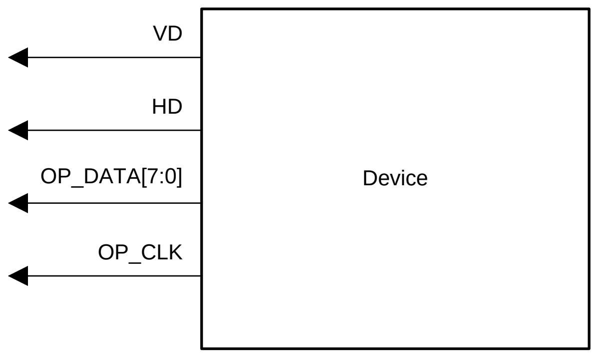


Figure 8. Output Block Diagram

Table 22. Output Interface

PIN NAMES	DESCRIPTION
OP_CLK	Output interface clock. All output interface signals transition on the configured (positive or negative) edge of this clock.
OP_DATA[7:0]	Output CMOS data pins. By default, all pins are used for transfer of data. In 4-lane mode, only DATA[3:0] are used. In 1-lane SSI mode, DATA[3] is used as OP_CS and DATA[4] is used as the data out pin.
HD	This signal is used as the horizontal sync in DVP mode to indicate row data transfer.
VD	Frame sync. This pin is used to indicate the beginning of a new frame.

7.3.5.1 Output Data Format

The depth information can be arranged in various configurations as per the host application requirements using register controls.

7.3.5.1.1 Arrangement of Bytes

Each pixel data are represented using 32 bits of data. This data can be broken down into:

- 12 bits of amplitude (C) data
- 4 bits of ambient (A) data
- 12 bits of phase (P) data
- 4 bits of flags (F) data

The structure of the 32-bit data is shown in Table 23.

Table 23. 4-Byte Mode Word Structure

BYTE 3								**BYTE 2**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS[3:0]				PHASE[11:0]											
BYTE 1								**BYTE 0**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMBIENT[3:0]				AMPLITUDE[11:0]											

Ambient and amplitude information together form a 16-bit word with ambient data in the MSBs. Flags and phase information together form a 16-bit word with flags data in the MSBs. Data are grouped in sets of eight words to enable efficient arithmetic at the host processor. Within the 16-bit words, the least significant byte is output first, as shown in Figure 9.

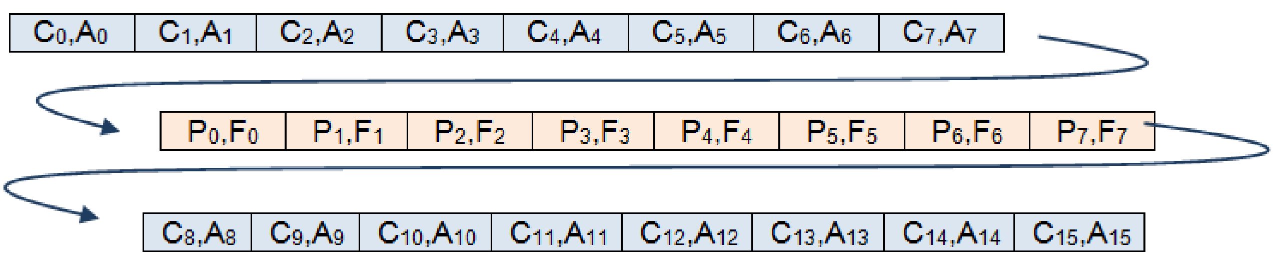


Figure 9. Group-by-8 Mode

7.3.5.2 Data Output Waveforms

The VD output toggles after the end of the last quad readout in every frame. Depending on the configured output mode, the relation of VD with the data output changes. This section describes the output waveforms for the supported output modes.

7.3.5.2.1 8-Lane Mode: DVP

DVP mode outputs the array data row by row. A frame marker and a row marker are used to indicate the frame and row boundaries respectively. Output data order is least significant byte first. The output timing is shown in Figure 10 and Figure 11.

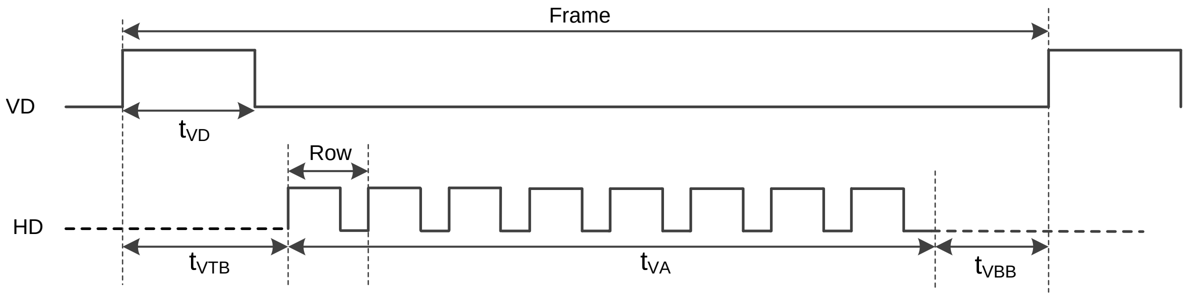


Figure 10. DVP Frame Format

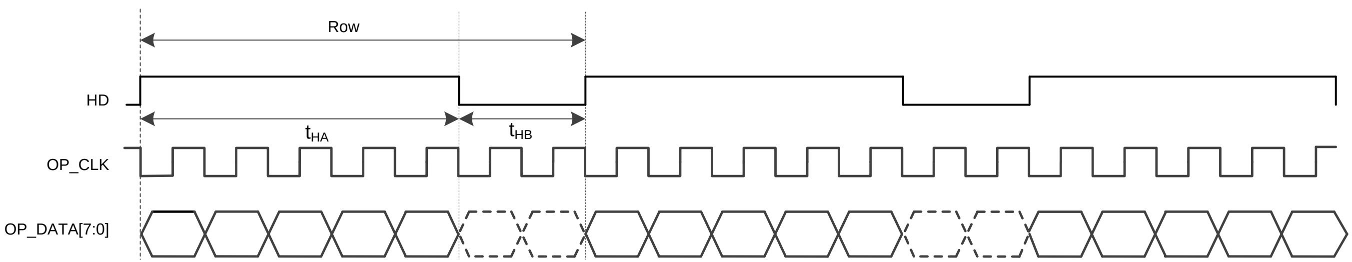


Figure 11. DVP Line Format

The timing notations are listed in Table 24 and the relevant parameters are listed in Table 25.

Table 24. DVP Timing Notations

TIMING NOTATION	DESCRIPTION	PROGRAMMABLE OR CALCULATED
t_{VD}	Vertical sync time	Programmable using the VD_ACTIVE parameter
t_{VTB}	Vertical top blanking time	Programmable using the FRM_BLANK_SIZE and VD_ACTIVE parameters
t_{VA}	Vertical active time	Calculated from ROI and binning settings
t_{VBB}	Vertical bottom blanking time	Internally always set to 0
t_{HA}	Horizontal active time	Calculated from ROI and binning settings
t_{HB}	Horizontal blanking time	Programmable using the LINE_BLANK_SIZE parameter

Table 25. DVP Parameters

PARAMETER	DESCRIPTION
HD_POL	Polarity of the HD signal.
VD_POL	Polarity of the VD signal.
OP_MODE	0 = DVP mode 1 = Serial mode
OP_CS_POL	Polarity of the OP_CS signal. 0 = Active low 1 = Active high
OP_CLK_FREQ	Output clock frequency. 0 = 24 MHz 1 = 12 MHz 2 = 6 MHz 3 = 3 MHz

7.3.5.2.2 1-Lane Mode: SSI

Chip select (OP_CS) indicates the validity of the data presented on the OP_DATAx (where x = 0 to 7) pin. For example, if a block-blanking period of two clocks and a block size of four bytes are programmed, OP_CS remains inactive for two clocks and remains active for 32 clock cycles. The timing for this mode is shown in Figure 12 and Figure 13. The related notations are listed in Table 24. The related register controls are listed in Table 25.

A continuing sequence of bytes containing FFh is inserted in the beginning of each frame to indicate the start of frame in this mode. The valid data of the first pixel are the set of bytes following the last FFh in the beginning of the frame.

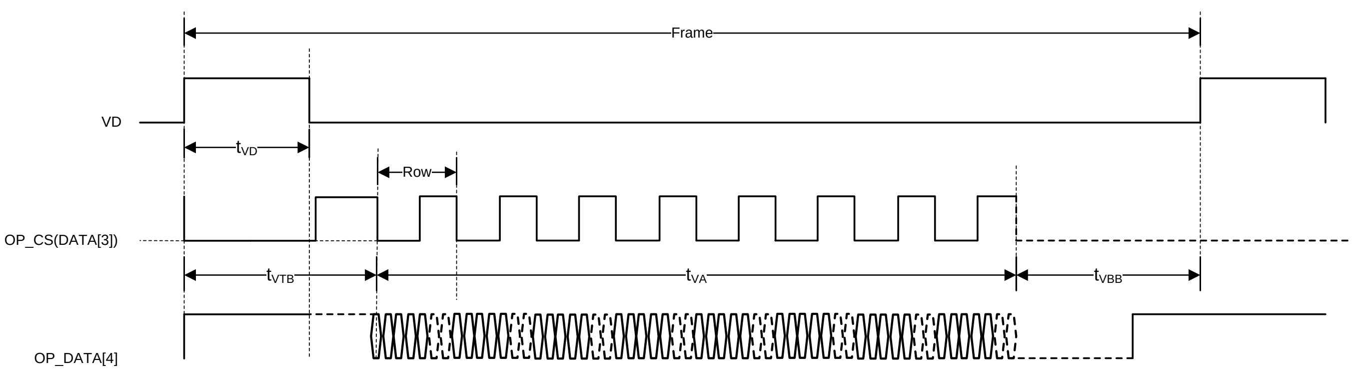


Figure 12. 1-Lane SSI Mode Frame Timing Diagram

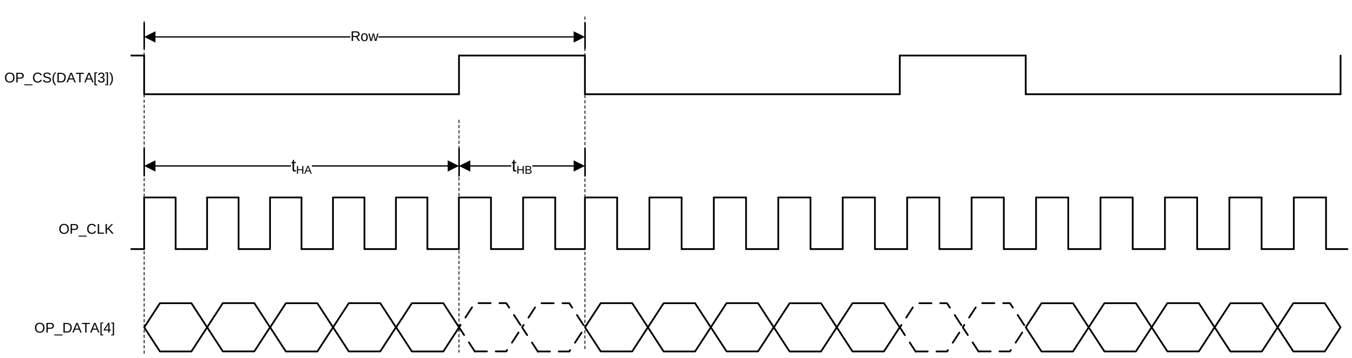


Figure 13. 1-Lane SSI Mode Line Timing Diagram

7.3.5.2.2.1 Serialization Logic in 1-Lane Mode

Each byte of data is serialized and sent out on OP_DATA[4]. Within each byte, the LSB is sent out first. The serialization logic is diagrammatically shown in Figure 14.

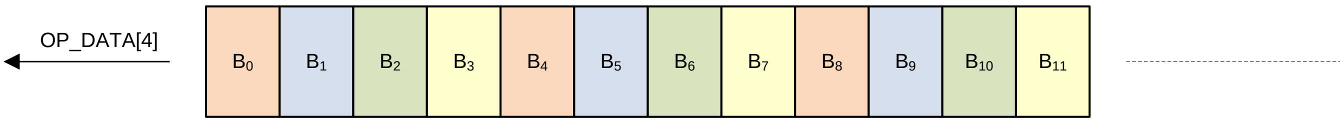


Figure 14. Serialization in 1-Lane SSI Mode

7.3.6 Temperature Sensor

The device has an internal temperature sensor to monitor the temperature of the sensor core. The output of the temperature sensor is accessible from a register (*TEMP_SENSOR*). The sensor temperature can be used for the built-in temperature calibration. Temperature data are automatically updated every frame.

7.3.7 Slave I²C Interface

The sensor can be configured by the host processor through an I²C interface. All registers have update mechanism controls. For example, the registers that affect frame size (such as ROI) are updated only on frame VD. The update control mechanism makes register writes easy because the write operation can happen at any point of time without taking into account the state of the sensor.

The device has two possible slave addresses: 1011000 (58h) and 1011001 (59h) based on the state of the I2C_SLV_ADDR[0] bit. The register access can be a single read/write or continuous read/write with auto-incrementation of the register address. In continuous read/write mode, the appropriate register settings in the I²C control register is necessary.

The individual registers are 24 bits long in this device. However, the register read/write is in chunks of eight bits. After every 8-bit transfer, the slave expects an acknowledgment from the master in the case of a read or gives out an acknowledgment in the case of a write. Figure 15 to Figure 19 explain the I²C format.

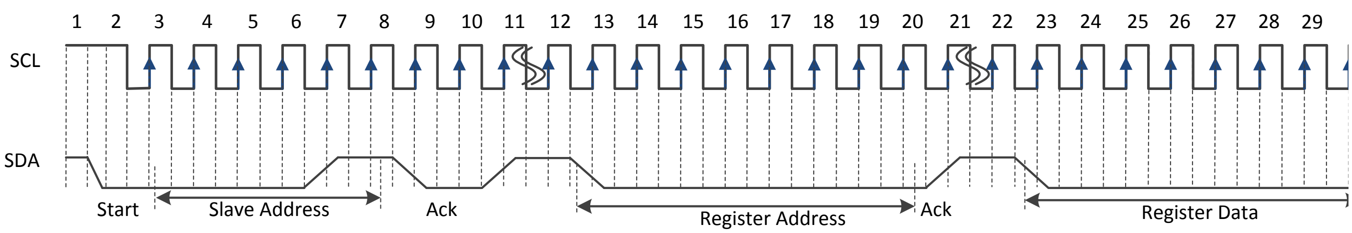


Figure 15. I²C Write Example

Figure 16. I²C Register Write

Start	Slave Addr	W	Ack	Reg Addr	Ack	Reg Data [7:0]	Ack	Reg Data [15:8]	Ack	Reg Data [23:16]	Ack	Stop

For example, to write 654321h to any register, data must be split into three bytes with the byte order as: 21h, 43h, and 65h. The same holds true for the read sequence. The first byte of data received corresponds to bits 7-0, bits 15-8, and finally followed by bits 23-16. In Figure 17 to Figure 19, split up of data (with Ack in between) is shown.

Figure 17. I²C Register Read

Start	Slave Addr	W	Ack	Reg Addr	Ack	Start	Slave Addr	R	Ack	Reg Data [7:0]	Ack	Reg Data [15:8]	Ack	Reg Data [23:16]	Ack	Stop

Figure 18. I²C Register Write (Continuous Mode)

Start	Slave Addr	W	Ack	Reg Addr	Ack	Reg[1] Data	Ack	…	Reg[n] Data	Ack	Stop

Figure 19. I²C Register Read (Continuous Mode)

Start	Slave Addr	W	Ack	Reg Addr	Ack	Start	Slave Addr	R	Ack	Reg[1] Data Read	Ack	…	Reg[n] Data Read	Ack	Stop

7.3.8 I²C Master

The I²C master interface is used for reading the temperature from an off-chip temperature sensor on the board. This sensor can be used for calibrating the system parameters with temperature changes. Usually, the external temperature sensor is used for measuring the illumination module temperature. The temperature readings are used internally for calibrating the phase measurement. The related programmable parameters and status registers are listed in Table 26.

Table 26. External Temperature Sensor

PARAMETER	DESCRIPTION
TILLUM_SLV_ADDR	External temperature sensor's 8-bit slave read address. This temperature sensor is assumed to be near the ToF illumination driver for calibration. TILLUM_SLV_ADDR = (8-bit slave address | 1)
TILLUM	Status registers indicate the temperature readout from the external temperature sensor
TILLUM_EN	When set to 1, enables I²C transactions for reading from the external temperature sensor.

The temperature readings are refreshed every frame. A single byte read operation is performed on each of the temperature sensors to read the corresponding temperature. The temperature sensors are expected to return the temperature in a single unsigned byte. TI's TMP103 series temperature sensors conform to this behavior. For temperature calibration of phase, the value read from the temperature sensor is assumed to be linear with the actual temperature.

7.4 Device Functional Modes

To optimize power, the OPT8320 provides three types of operation:

1. Normal operation
2. Normal operation with dynamic power-down
3. Standby

7.4.1 Normal Operation

The default mode is the normal operation mode. In this mode of operation, no power-save options are available. All sub-systems are operational all the time.

7.4.2 Normal Operation with Dynamic Power-Down

With dynamic power-down enabled, the analog signal chain is powered down at all times except when the sensor readout is being performed. To enable dynamic power-down, the EN_DYN_PDN parameter must be set to 1.

7.4.3 Standby

During standby mode, the TG is stopped and all pins are placed in reset state. Therefore, all sequencing operations come to a halt. I²C transactions remain enabled. To place the OPT8320 in standby mode, the standby input pin must be pulled high or the STANDBY parameter must be set to 1. To bring the device out of standby, the STANDBY parameter must read as 0 and the standby pin must be in a low state.

7.5 Register Maps

7.5.1 Serial Interface Register Map

Table 27 lists the serial interface registers.

Table 27. Register Map

ADDR (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOFTWARE_RESET
02h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MOD_PLL_UPDATE	0	0
04h	0	LOW_LATENCY_MODE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05h	0	0	HIGH_AMBIENT_EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	STANDBY	0	0
0Bh	0	0	0	0	0	0	0	0	0	0	INIT_2	0	0	0	0	0	0	0	0	0	0	0	0	0
0Ch	0	0	MOD_M						MOD_M_FRAC															

Register Maps (continued)

Table 27. Register Map (continued)

ADDR (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0Eh	0	0	0	0	0	0	ILLUM_DC_CORR_DIR	ILLUM_DC_CORR				0	0	0	0	0	0	0	0	0	0	0	0	0
0Fh	0	0	0	ILLUM_STATIC_POL	DEMOD_STATIC_POL	MODULATION_HOLD	0	0	0	0	0	0	0	1	0	0	1	MOD_PS			1	0	MOD_N	
11h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	QUAD_HOP_OFFSET			QUAD_HOP_EN
12h	PHASE_LIN_COEFF_0													PHASE_LIN_CORR_DIS	0	0	0	INIT_0						
13h	PHASE_LIN_COEFF_1													PHASE_LIN_CORR_PERIOD	0	0	0	0	0	0	0	0	0	0
14h	PHASE_LIN_COEFF_2													0	0	0	0	0	0	0	0	0	0	0
15h	PHASE_LIN_COEFF_3													0	0	0	0	0	0	0	0	0	0	0
16h	PHASE_LIN_COEFF_4													0	0	0	0	0	0	0	0	0	0	0
17h	PHASE_LIN_COEFF_5													0	0	0	0	0	0	0	0	0	0	0
18h	PHASE_LIN_COEFF_6													0	0	0	0	0	0	0	0	0	0	0
19h	PHASE_LIN_COEFF_7													0	0	0	0	0	0	0	0	0	0	0

Register Maps (continued)

Table 27. Register Map (continued)

ADDR (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1Ah	PHASE_LIN_COEFF_8													0	0	0	0	0	0	0	0	0	0	0
1Bh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	INIT_1						
1Fh	ROW_END								0	0	0	0	0	0	0	0	ROW_START							
20h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL_START							
21h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	COL_END							
39h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MOD_CDRIV_DC_BIAS				0	0	0	0
3Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	COL_RDOUT_DIR	ROW_RDOUT_DIR	0	0	0	0	0	0	0	0	0
3Bh	0	0	MOD_CDRIV_ CURR_STEP		MOD_CDRIV_CURR					MOD_CDRIV_EN	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4Fh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SUP_FRM_INTG_SCALE					
50h	INTG_DUTY_CYCLE_SET_FAILED	PIX_CNT_MAX_SET_FAILED	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	0
57h	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	TSENSOR								
5Bh	EASY_CONF_EN	SHUTTER_EN	ILLUM_EN_EARLY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Maps (continued)

Table 27. Register Map (continued)

ADDR (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5Ch	INTG_DUTY_CYCLE						LUMPED_DEAD_TIME	EN_DYN_PDN	MV_FLAGS_TO_AMBIENT	HD_POL	VD_POL	OP_DATA_ARRANGE_MODE	0	0	0	0	0	0	0	0	0	0	0	0
6Ah	0	0	0	0	0	INVERT_HD_VD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6Ch	0	0	0	0	0	0	0	TEST_PATTERN				0	0	1	0	0	0	1	0	0	0	1	0	0
80h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TG_EN
81h	0	0	0	0	0	0	0	0	0	0	0	SYNC_MODE	0	0	0	0	1	0	UPDATE_SEL		0	0	0	SLAVE_MODE
82h	0	0	PIX_CNT_MAX																					
83h	0	0	0	0	0	0	0	0	0	0	0	0	0	SUB_FRAME_CNT_MAX1							0	1	0	0
D6h	0	1	FRAME_SYNC_DELAY																					
D9h	0	0	COLS_TO_MERGE		ROWS_TO_MERGE		0	IQ_SCALE_EN	BINNING_MODE	TEST_PATTERN_ENABLE	0	0	0	0	SATURATION_THRESHOLD				0	0	1	IQ_SCALE		
DCh	VD_ACTIVE			LINE_BLANK_SIZE										LINE_ACTIVE_SIZE										0
DDh	0	0	0	0	0	0	0	1	1	FRM_BLANK_SIZE						0	0	0	1	1	1	1	0	0
DEh	AMPLITUDE_THRESHOLD												0	OP_CLK_FREQ		0	OP_CS_POL	0	0	OP_MODE	0	0	0	0
EEh	0	0	0	0	0	0	0	0	TILLUM_SLV_ADDR								0	0	0	0	0	0	0	0
F2h	0	0	0	0	1	0	0	TILLUM_EN	0	0	0	0	0	0	0	0	TILLUM							
F5h	0	0	0	0	0	0	0	0	0	0	0	PHASE_CORR_2												

Register Maps (continued)

Table 27. Register Map (continued)

ADDR (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F6h	CALIB_PREC				CLIP_MODE	DISABLE_TEMP_CORR	DISABLE_OFFSET_CORR	COEFF_SENSOR																
F7h	0	0	0	0	0	0	0	COEFF_ILLUM																
F8h	SCRATCH1								TILLUM_CALIB								TSENSOR_CALIB							
F9h	0	0	0	0	FLIP_PHASE	0	0	0	0	0	0	PHASE_CORR_1												
FBh	0	0	0	0	0	0	0	1	1	1	1	0	DEALIAS_EN	ALT_FREQ_SEL			SUB_FRAME_CNT_MAX2							ALT_FRM_EN
FEh	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	STATISTICS_EN	0	1	1	1	1

7.5.1.1 Register Descriptions

7.5.1.1.1 Register 00h (address = 00h) [reset = 0h]

Figure 20. Register 00h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	SOFTWARE_ RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0.
8-1	0	R/W	0h	Always read or write 0.
0	SOFTWARE_RESET	R/W	0h	Resets the state of the sensor and resets all registers to their default values.

7.5.1.1.2 Register 02h (address = 02h) [reset = 0h]

Figure 21. Register 02h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	MOD_PLL_ UPDATE	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	W	0h	Must write 0.
10-3	0	R/W	0h	Always read or write 0.
2	MOD_PLL_UPDATE	R/W	0h	After updating the PLL registers, set this register to 1 and then back to 0 to update the PLL frequency.
1-0	0	R/W	0h	Always read or write 0.

7.5.1.1.3 Register 04h (address = 04h) [reset = 0h]

Figure 22. Register 04h

23	22	21	20	19	18	17	16
0	LOW_LATENCY_MODE	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 30. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Always read or write 0.
22	LOW_LATENCY_MODE	R/W	0h	Enables processing of data as soon as the last quad readout is done.
21-0	0	R/W	0h	Always read or write 0.

7.5.1.1.4 Register 05h (address = 05h) [reset = 0h]

Figure 23. Register 05h

23	22	21	20	19	18	17	16
0	0	HIGH_AMBIENT_EN	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 31. Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Always read or write 0.
21-21	HIGH_AMBIENT_EN	R/W	0h	When this mode is enabled, pixel reset is active during readout. Use only in shutter mode (shutter enabled).
20-0	0	R/W	0h	Always read or write 0.

7.5.1.1.5 Register 08h (address = 08h) [reset = 4h]

Figure 24. Register 08h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	STANDBY	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	W	0h	Must write 0.
7-3	0	R/W	0h	Always read or write 0.
2-2	STANDBY	R/W	1h	When set to 1, the device is put in standby mode. By default, the device is in standby.
1-0	0	R/W	0h	Always read or write 0.

7.5.1.1.6 Register 0Bh (address = 0Bh) [reset = 0h]

Figure 25. Register 0Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	INIT_2	0	0	0	0	0
W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-14	0	W	0h	Must write 0.
13-13	INIT_2	R/W	0h	Set to 1 for proper functionality.
12-0	0	R/W	0h	Always read or write 0.

7.5.1.1.7 Register 0Ch (address = 0Ch) [reset = 100000h]

Figure 26. Register 0Ch

23	22	21	20	19	18	17	16
0	0	MOD_M					
R/W-0h	R/W-0h	R/W-10h					
15	14	13	12	11	10	9	8
MOD_M_FRAC							
R/W-0h							
7	6	5	4	3	2	1	0
MOD_M_FRAC							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 34. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Always read or write 0.
21-16	MOD_M	R/W	10h	$MOD\_F = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)} \times QUAD\_CNT\_MAX \times (1 + MOD\_PS)}$ $VCO\_FREQ = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)}}$ The condition 300 MHz < VCO_FREQ < 600 MHz must be met.
15-0	MOD_M_FRAC	R/W	0h	$MOD\_F = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)} \times QUAD\_CNT\_MAX \times (1 + MOD\_PS)}$ $VCO\_FREQ = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)}}$ The condition 300 MHz < VCO_FREQ < 600 MHz must be met.

7.5.1.1.8 Register 0Eh (address = 0Eh) [reset = 0h]

Figure 27. Register 0Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	ILLUM_DC_CORR_DIR	ILLUM_DC_CORR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ILLUM_DC_CORR			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 35. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-18	0	R/W	0h	Always read or write 0.
17-17	ILLUM_DC_CORR_DIR	R/W	0h	Sets the direction of duty cycle correction for illumination output waveforms. Note that when duty cycle is increased, ILLUM_P duty cycle increases and ILLUM_N duty cycle decreases. 0 = Increases the duty cycle of ILLUM_P 1 = Reduces the duty cycle of ILLUM_P
16-13	ILLUM_DC_CORR	R/W	0h	Illumination duty cycle can be corrected in steps of approximately 360 ps. The maximum value of this register is 0Bh and results into a total correction of approximately ±4 ns.
12-0	0	R/W	0h	Always read or write 0.

7.5.1.1.9 Register 0Fh (address = 0Fh) [reset = 499h]

Figure 28. Register 0Fh

23	22	21	20	19	18	17	16
0	0	0	ILLUM_STATIC_POL	DEMOD_STATIC_POL	MODULATION_HOLD	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	1	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	MOD_PS			1	0	MOD_N	
R/W-1h	R/W-1h			R/W-1h	R/W-0h	R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 36. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	R/W	0h	Always read or write 0.
20-20	ILLUM_STATIC_POL	R/W	0h	DC polarity of modulation pins when MODULATION_HOLD is set to 1. 0 = Hold low 1 = Hold high
19-19	DEMOD_STATIC_POL	R/W	0h	DC polarity of demodulation when MODULATION_HOLD is set to 1. 0 = Hold low 1 = Hold high
18-18	MODULATION_HOLD	R/W	0h	When set to 1, holds the demodulation and modulation waveforms to a static state during integration time.
17-7	9	R/W	9h	Always read or write 9.
6-4	MOD_PS	R/W	1h	$MOD\_F = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)} \times QUAD\_CNT\_MAX \times (1 + MOD\_PS)}$ The condition 300 MHz < VCO_FREQ < 600 MHz must be met.
3-2	2	R/W	2h	Always read or write 2.
1-0	MOD_N	R/W	1h	$MOD\_F = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)} \times QUAD\_CNT\_MAX \times (1 + MOD\_PS)}$ $VCO\_FREQ = \frac{MOD\_M \times 24\ MHz}{2^{(MOD\_N\text{-}1)}}$ The condition 300 MHz < VCO_FREQ < 600 MHz must be met.

7.5.1.1.10 Register 11h (address = 11h) [reset = 4h]

Figure 29. Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	QUAD_HOP_OFFSET			QUAD_HOP_EN
W-0h	W-0h	W-0h	W-0h	R/W-2h			R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	W	0h	Must write 0.
3-1	QUAD_HOP_OFFSET	R/W	2h	The offset of the quad sequence for alternate sub-frames.
0	QUAD_HOP_EN	R/W	0h	Enables a different sequence of quads for odd and even sub-frames.

7.5.1.1.11 Register 12h (address = 12h) [reset = 0h]

Figure 30. Register 12h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_0							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASE_LIN_COEFF_0					PHASE_LIN_CORR_DIS	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	INIT_0						
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 38. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_0	R/W	0h	Phase nonlinearity correction coefficient. Signed, twos complement.
10	PHASE_LIN_CORR_DIS	R/W	0h	Disables phase nonlinearity correction when set to 1.
9-7	0	R/W	0h	Always read or write 0.
6-0	INIT_0	R/W	0h	Set to 0Ah for proper functionality.

7.5.1.1.12 Register 13h (address = 13h) [reset = 40000h]

Figure 31. Register 13h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_1							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASE_LIN_COEFF_1					PHASE_LIN_CORR_PERIOD	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 39. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_1	R/W	80h	Phase nonlinearity correction coefficient. Signed, twos complement.
10	PHASE_LIN_CORR_PERIOD	R/W	0h	Represents the repetition period of nonlinearity. The eight LUT values are spread over this period. The remaining periods in 360 degrees are a repeat of this period. 0 = 90° 1 = 180°
9-0	0	R/W	0h	Always read or write 0.

7.5.1.1.13 Register 14h (address = 14h) [reset = 80000h]

Figure 32. Register 14h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_2							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASE_LIN_COEFF_2					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 40. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_2	R/W	100h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.14 Register 15h (address = 15h) [reset = C0000h]

Figure 33. Register 15h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_3					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 41. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_3	R/W	180h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.15 Register 16h (address = 16h) [reset = 100000h]

Figure 34. Register 16h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_4							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_4					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 42. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_4	R/W	200h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.16 Register 17h (address = 17h) [reset = 140000h]

Figure 35. Register 17h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_5							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_5					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 43. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_5	R/W	280h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.17 Register 18h (address = 18h) [reset = 180000h]

Figure 36. Register 18h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_6							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_6					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 44. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_6	R/W	300h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.18 Register 19h (address = 19h) [reset = 1C0000h]

Figure 37. Register 19h

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_7							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_7					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 45. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_7	R/W	380h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.19 Register 1Ah (address = 1Ah) [reset = 200000h]

Figure 38. Register 1Ah

23	22	21	20	19	18	17	16
PHASE_LIN_COEFF_8							
R/W-0h							
15	14	13	12	11	10	9	8
PHASE_LIN_COEFF_8					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 46. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-11	PHASE_LIN_COEFF_8	R/W	400h	Phase nonlinearity correction coefficient. Signed, twos complement.
10-0	0	R/W	0h	Always read or write 0.

7.5.1.1.20 Register 1Bh (address = 1Bh) [reset = 0h]

Figure 39. Register 1Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	INIT_1						
W-0h	R/W-0h						

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-7	0	W	0h	Must write 0.
6-0	INIT_1	R/W	0h	Set to 0Ah for proper functionality.

7.5.1.1.21 Register 1Fh (address = 1Fh) [reset = 3B0000h]

Figure 40. Register 1Fh

23	22	21	20	19	18	17	16
ROW_END							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ROW_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 48. Register 1Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	ROW_END	R/W	3Bh	End address for row address bus of the default ROI. Max = 59
15-8	0	R/W	0h	Always read or write 0.
7-0	ROW_START	R/W	0h	Start address for row address bus of the default ROI. Max = 59

7.5.1.1.22 Register 20h (address = 20h) [reset = 0h]

Figure 41. Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
COL_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 49. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Always read or write 0.
7-0	COL_START	R/W	0h	Start address for column address bus of the default ROI. Max = 79

7.5.1.1.23 Register 21h (address = 21h) [reset = 40004Fh]

Figure 42. Register 21h

23	22	21	20	19	18	17	16
0	1	0	0	0	0	0	0
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
COL_END							
R/W-4Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	16384	R/W	4000h	Always read or write 16384.
7-0	COL_END	R/W	4Fh	End address for col address bus of the default ROI. Max = 79

7.5.1.1.24 Register 39h (address = 39h) [reset = 0h]

Figure 43. Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MOD_CDRIV_DC_BIAS				0	0	0	0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	R/W	0h	Always read or write 0.
7-4	MOD_CDRIV_DC_BIAS	R/W	0h	Sets the dc bias current for the LED driver in steps of MOD_CDRIV_CURR_STEP. Output on current = [MOD_CDRIV_DC_BIAS (mA) + MOD_CDRIV_CURR (mA)] × MOD_CDRIV_CURR_STEP. Output off current = MOD_CDRIV_DC_BIAS (mA) × MOD_CDRIV_CURR_STEP.
3-0	0	R/W	0h	Always read or write 0.

7.5.1.1.25 Register 3Ah (address = 3Ah) [reset = 0h]

Figure 44. Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	COL_RDOUT_DIR	ROW_RDOUT_DIR	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 52. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	R/W	0h	Always read or write 0.
10	COL_RDOUT_DIR	R/W	0h	Used for mirroring the image along the vertical axis (left-right mirroring).
9	ROW_RDOUT_DIR	R/W	0h	Used for mirroring the image along the horizontal axis (up-down mirroring).
8-0	0	R/W	0h	Always read or write 0.

7.5.1.1.26 Register 3Bh (address = 3Bh) [reset = 0h]

Figure 45. Register 3Bh

23	22	21	20	19	18	17	16
0	0	MOD_CDRIV_CURR_STEP		MOD_CDRIV_CURR			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MOD_CDRIV_ CURR	MOD_CDRIV_ EN	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 53. Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Always read or write 0.
21-20	MOD_CDRIV_CURR_STEP	R/W	0h	Step size of the MOD_CDRIV current Output on current = [MOD_CDRIV_DC_BIAS (mA) + MOD_CDRIV_CURR (mA)] × MOD_CDRIV_CURR_STEP. Output off current = MOD_CDRIV_DC_BIAS (mA) × MOD_CDRIV_CURR_STEP. 0 = 5 mA 1 = 3.7 5mA 2 = 2.5 mA 3 = 1.25 mA
19-15	MOD_CDRIV_CURR	R/W	0h	Program LED driver current in steps of MOD_CDRIV_CURR_STEP. Output on current = [MOD_CDRIV_DC_BIAS (mA) + MOD_CDRIV_CURR (mA)] × MOD_CDRIV_CURR_STEP. Output off current = MOD_CDRIV_DC_BIAS (mA) × MOD_CDRIV_CURR_STEP.
14	MOD_CDRIV_EN	R/W	0h	Set to 1 to enable the internal illumination driver on the MOD_CDRIV pin. 0 = Power-down 1 = Active
13-0	0	R/W	0h	Always read or write 0.

7.5.1.1.27 Register 4Fh (address = 4Fh) [reset = 3Fh]

Figure 46. Register 4Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	SUP_FRM_INTG_SCALE					
W-0h	W-0h	R/W-3Fh					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 54. Register 4Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-6	0	W	0h	Must write 0.
5-0	SUP_FRM_INTG_SCALE	R/W	3Fh	Denotes the percentage of INTG_PHASE in the supplementary frame in terms of the base frame. INTG_DUTY_CYCLE2 = INTG_DUTY_CYCLE1 × (SUP_FRM_INTG_SCALE + 1) / 64.

7.5.1.1.28 Register 50h (address = 50h) [reset = C32h]

Figure 47. Register 50h

23	22	21	20	19	18	17	16
INTG_DUTY_ CYCLE_SET_ FAILED	PIX_CNT_MAX _SET_FAILED	0	0	0	0	0	0
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	1	1	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	1	1	0	0	1	0
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
23	INTG_DUTY_CYCLE_SET_FAILED	R	0h	Indicates that the integration duty cycle is higher than what the current quad time (PIX_CNT_MAX) can handle.
22	PIX_CNT_MAX_SET_FAILED	R	0h	Indicates that the PIX_CNT_MAX setting is too low.
21-12	0	R/W	0h	These rows were all lumped together as field = 3122 and reset = C32h. Please adjust whatever you meant by that to be in the proper standard.
11-10	1	R/W	1h	Always read or write 1.
9-6	0	R/W	0h	Always read or write 0.
5-4	1	R/W	1h	Always read or write 1.
3-2	0	R/W	0h	Always read or write 0.
1	1	R/W	1h	Always read or write 1.
0	0	R/W	0h	Always read or write 0.

7.5.1.1.29 Register 57h (address = 57h) [reset = 1000h]

Figure 48. Register 57h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	1	0	0	0	TSENSOR
W-0h	W-0h	W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSOR							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 56. Register 57h Field Descriptions

Bit	Field	Type	Reset	Description
23-13	0	W	0h	Must write 0.
12-9	8	R/W	8h	Always read or write 8.
8-0	TSENSOR	R	0h	Temperature output from the OPT8320 built-in temperature sensor. Signed, twos complement.

7.5.1.1.30 Register 5Bh (address = 5Bh) [reset = 800000h]

Figure 49. Register 5Bh

23	22	21	20	19	18	17	16
EASY_CONF_EN	SHUTTER_EN	ILLUM_EN_EARLY	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 57. Register 5Bh Field Descriptions

Bit	Field	Type	Reset	Description
23	EASY_CONF_EN	R/W	1h	When set to 1, enables simple configuration of timings that covers most of the usual scenarios.
22	SHUTTER_EN	R/W	0h	If set to 0, shutter functionality is disabled. If shutter functionality is disabled, the pixel charge continues to transfer to the storage node during the sensor readout.
21	ILLUM_EN_EARLY	R/W	0h	Activates the illumination modulation before integration starts by 15 µs when set to 1.
20-0	0	R/W	0h	Always read or write 0.

7.5.1.1.31 Register 5Ch (address = 5Ch) [reset = 340000h]

Figure 50. Register 5Ch

23	22	21	20	19	18	17	16
INTG_DUTY_CYCLE						LUMPED_DEAD_TIME	EN_DYN_PDN
R/W-0h						R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MV_FLAGS_TO_AMBIENT	HD_POL	VD_POL	OP_DATA_ARRANGE_MODE	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 58. Register 5Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-18	INTG_DUTY_CYCLE	R/W	Dh	If no scaling is used, the integration duty cycle (%) = INTG_DUTY_CYCLE × 100 / 64.0.
17	LUMPED_DEAD_TIME	R/W	0h	In easy configuration mode, dead time can either be distributed equally among all quads or can be lumped at the end of each frame. 0 = Uniform quad dead time 1 = Lumped frame dead time
16	EN_DYN_PDN	R/W	0h	When set to 1, enables dynamic power-down.
15	MV_FLAGS_TO_AMBIENT	R/W	0h	When set to 1, ambient data are replaced by flag data in the data stream.
14	HD_POL	R/W	0h	Sets the polarity of the HD output. 0 = Active high 1 = Active low
13	VD_POL	R/W	0h	Sets the polarity of the VD output. 0 = Active high 1 = Active low
12	OP_DATA_ARRANGE_MODE	R/W	0h	Rearranges the pattern of output data. 0 = Rearranged in chunks of eight 1 = Continuous
11-0	0	R/W	0h	Always read or write 0.

7.5.1.1.32 Register 6Ah (address = 6Ah) [reset = 0h]

Figure 51. Register 6Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	INVERT_ HD_VD	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. Register 6Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	R/W	0h	Always read or write 0.
18	INVERT_HD_VD	R/W	0h	Invert HD and VD.
17-0	0	R/W	0h	Always read or write 0.

7.5.1.1.33 Register 6Ch (address = 6Ch) [reset = 444h]

Figure 52. Register 6Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	TEST_ PATTERN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TEST_PATTERN			0	0	1	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. Register 6Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	R/W	0h	Always read or write 0.
16-13	TEST_PATTERN	R/W	0h	Test pattern. Write 5 to generate a test pattern.
12-0	1092	R/W	444h	Always read or write 1092.

7.5.1.1.34 Register 80h (address = 80h) [reset = 0h]

Figure 53. Register 80h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	TG_EN
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 61. Register 80h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	W	0h	Must write 0.
3-1	0	R/W	0h	Always read or write 0.
0	TG_EN	R/W	0h	When set to 1, enables the timing generator. By default the TG is disabled.

7.5.1.1.35 Register 81h (address = 81h) [reset = 80h]

Figure 54. Register 81h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	SYNC_MODE	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	UPDATE_SEL		0	0	0	SLAVE_MODE
R/W-1h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 62. Register 81h Field Descriptions

Bit	Field	Type	Reset	Description
23-13	0	W	0h	Must write 0.
12	SYNC_MODE	R/W	0h	Puts the TG in sync mode. The TG synchronizes with the external input through the VD_IN pin for the start of frames, but does not depend on it.
11-6	2	R/W	2h	Always read or write 2.
5-4	UPDATE_SEL	R/W	0h	Selects the update mechanism for timing related parameters. Set to 02h for proper functionality in master mode and 00h in slave mode. 0 = Immediate 1 = Immediate 2 = Update on new frame 3 = Update on new sub-frame
3-1	0	R/W	0h	Always read or write 0.
0	SLAVE_MODE	R/W	0h	Puts the TG into slave mode. The TG waits for an external sync through the VD_IN pin for the start of frames.

7.5.1.1.36 Register 82h (address = 82h) [reset = 30D4h]

Figure 55. Register 82h

23	22	21	20	19	18	17	16
0	0	PIX_CNT_MAX					
R/W-0h	R/W-0h	R/W-0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PIX_CNT_MAX							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PIX_CNT_MAX							
R/W-D4h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 63. Register 82h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Always read or write 0.
21-0	PIX_CNT_MAX	R/W	30D4h	Total frame time divided by the number of sub-frames and quads in terms of system clock cycles.

7.5.1.1.37 Register 83h (address = 83h) [reset = 104h]

Figure 56. Register 83h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	SUB_FRAME_CNT_MAX1		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB_FRAME_CNT_MAX1				0	1	0	0
R/W-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 64. Register 83h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	W	0h	Must write 0.
10-4	SUB_FRAME_CNT_MAX1	R/W	10h	Total number of sub-frames in each base frame. Only values that are powers of 2 are valid. Behavior is unpredictable when set to other values. Max = 32
3-0	4	R/W	4h	Always read or write 4.

7.5.1.1.38 Register D6h (address = D6h) [reset = 400001h]

Figure 57. Register D6h

23	22	21	20	19	18	17	16
0	1	FRAME_SYNC_DELAY					
R/W-0h	R/W-1h	R/W-0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FRAME_SYNC_DELAY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRAME_SYNC_DELAY							
R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 65. Register D6h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	1	R/W	1h	Always read or write 1.
21-0	FRAME_SYNC_DELAY	R/W	1h	The programmable delay between the external VD and synced VD. The minimum value of programmable delay is one cycle.

7.5.1.1.39 Register D9h (address = D9h) [reset = Ch]

Figure 58. Register D9h

23	22	21	20	19	18	17	16
0	0	COLS_TO_MERGE		ROWS_TO_MERGE		0	IQ_SCALE_EN
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BINNING_ MODE	TEST_ PATTERN_ ENABLE	0	0	0	0	SATURATION_THRESHOLD	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SATURATION_THRESHOLD		0	0	1	IQ_SCALE		
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-4h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 66. Register D9h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	Always read or write 0.
21-20	COLS_TO_MERGE	R/W	0h	Number of columns to merge for binning = $2^{COLS\_TO\_MERGE}$.
19-18	ROWS_TO_MERGE	R/W	0h	Number of rows to merge for binning = $2^{ROWS\_TO\_MERGE}$.
17	0	R/W	0h	Always read or write 0.
16	IQ_SCALE_EN	R/W	0h	When set to 1, enable scaling of I and Q according to the IQ_SCALE register.
15	BINNING_MODE	R/W	0h	When set to 1, binning does not modify the size of the frame. In the default case, binning scales the frame size as per the binning size.
14	TEST_PATTERN_ENABLE	R/W	0h	Enable test pattern.
13-10	0	R/W	0h	Always read or write 0.
9-6	SATURATION_THRESHOLD	R/W	0h	If the ambient values are below this level, corresponding phase values are zeroed. Amplitude values are retained.
5-3	1	R/W	1h	Always read or write 1.
2-0	IQ_SCALE	R/W	4h	The computed internal I/Q are left-shifted by this factor before computation of phase and amplitude. I = I << IQ_SCALE Q = Q << IQ_SCALE Set IQ_SCALE_EN to enable scaling.

7.5.1.1.40 Register DCh (address = DCh) [reset = 480280h]

Figure 59. Register DCh

23	22	21	20	19	18	17	16
VD_ACTIVE			LINE_BLANK_SIZE				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
LINE_BLANK_SIZE					LINE_ACTIVE_SIZE		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
LINE_ACTIVE_SIZE							0
R/W-40h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 67. Register DCh Field Descriptions

Bit	Field	Type	Reset	Description
23-21	VD_ACTIVE	R/W	2h	The duration of the VD pulse in terms of number of DVP lines [n × (t_{HA} + t_{HB})]. 0 = 1X t_{LINE} 1 = 2X t_{LINE} 2 = 4X t_{LINE} 3 = 8X t_{LINE} 4 = 16X t_{LINE} 5 = 32X t_{LINE} 6 = 4X t_{LINE} 7 = 4X t_{LINE}
20-11	LINE_BLANK_SIZE	R/W	100h	The horizontal blank period in DVP mode in terms of number of pixels (t_{HB} in number of pixels). min = 2
10-1	LINE_ACTIVE_SIZE	R/W	140h	Horizontal active period in DVP mode in terms of number of pixels (t_{HA} in number of pixels).
0	0	R/W	0h	Always read or write 0.

7.5.1.1.41 Register DDh (address = DDh) [reset = 1883Ch]

Figure 60. Register DDh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
1	FRM_BLANK_SIZE						0
R/W-1h	R/W-4h						R/W-0h
7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 68. Register DDh Field Descriptions

Bit	Field	Type	Reset	Description
23-15	3	R/W	3h	Always read or write 3.
14-9	FRM_BLANK_SIZE	R/W	4h	Number of blank DVP lines between VD and the first HD. (t_{VTB} – t_{VD} in number of lines). Min = 2
8-0	60	R/W	3Ch	Always read or write 60.

7.5.1.1.42 Register DEh (address = DEh) [reset = 0h]

Figure 61. Register DEh

23	22	21	20	19	18	17	16
AMPLITUDE_THRESHOLD							
R/W-0h							
15	14	13	12	11	10	9	8
AMPLITUDE_THRESHOLD				0	OP_CLK_FREQ		0
R/W-0h				R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
OP_CS_POL	0	0	OP_MODE	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 69. Register DEh Field Descriptions

Bit	Field	Type	Reset	Description
23-12	AMPLITUDE_THRESHOLD	R/W	0h	Phase becomes 000h when the amplitude is lower than this threshold.
11	0	R/W	0h	Always read or write 0.
10-9	OP_CLK_FREQ	R/W	0h	Sets the output data clock rate. Note that the host responsibility is to ensure that the rate is sufficient to attain the required frame rate without dropping any data. 0 = 24 MHz 1 = 12 MHz 2 = 6 MHz 3 = 3 MHz
8	0	R/W	0h	Always read or write 0.
7	OP_CS_POL	R/W	0h	Controls the polarity of the OP_CS line when active. 0 = Active low 1 = Active high
6-5	0	R/W	0h	Always read or write 0.
4	OP_MODE	R/W	0h	Selects between DVP or serial mode. 0 = DVP mode 1 = Serial mode
3-0	0	R/W	0h	Always read or write 0.

7.5.1.1.43 Register EEh (address = EEh) [reset = 0h]

Figure 62. Register EEh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TILLUM_SLV_ADDR							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 70. Register EEh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	R/W	0h	Always read or write 0.
15-8	TILLUM_SLV_ADDR	R/W	0h	External temperature sensor 8-bit slave read address. This temperature sensor is assumed to be near the ToF illumination driver for calibration. TILLUM_SLV_ADDR = (8-bit SLAVE_ADDR / 1).
7-0	0	R/W	0h	Always read or write 0.

7.5.1.1.44 Register F2h (address = F2h) [reset = 80000h]

Figure 63. Register F2h

23	22	21	20	19	18	17	16
0	0	0	0	1	0	0	TILLUM_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TILLUM							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. Register F2h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	4	R/W	4h	Always read or write 4.
16	TILLUM_EN	R/W	0h	Enables I^2C transactions for reading from the external temperature sensor.
15-8	0	R/W	0h	Always read or write 0.
7-0	TILLUM	R	0h	Temperature output from temperature sensor with 8-bit slave read address = (TILLUM_SLV_ADDR / 1). Signed, twos complement.

7.5.1.1.45 Register F5h (address = F5h) [reset = 0h]

Figure 64. Register F5h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	PHASE_CORR_2				
W-0h	W-0h	W-0h	R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE_CORR_2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 72. Register F5h Field Descriptions

Bit	Field	Type	Reset	Description
23-13	0	W	0h	Must write 0.
12-0	PHASE_CORR_2	R/W	0h	Phase correction for supplementary frame. This value is added to the obtained phase. Signed, twos complement. Min = –2048 Max = 2047

7.5.1.1.46 Register F6h (address = F6h) [reset = 880000h]

Figure 65. Register F6h

23	22	21	20	19	18	17	16
CALIB_PREC				CLIP_MODE	DISABLE_TEMP_CORR	DISABLE_OFFSET_CORR	COEFF_SENSOR
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COEFF_SENSOR							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COEFF_SENSOR							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 73. Register F6h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	CALIB_PREC	R/W	8h	Adjusts the precision of the temperature correction. Coefficients are scaled by CALIB_PREC. Internal coefficient = [programmed coefficient << (CALIB_PREC – 8)].
19	CLIP_MODE	R/W	1h	Set to 1 for proper functionality.
18	DISABLE_TEMP_CORR	R/W	0h	Disables temperature calibration of phase when set to 1.
17	DISABLE_OFFSET_CORR	R/W	0h	Disables phase offset correction when set to 1.
16-0	COEFF_SENSOR	R/W	0h	Phase correction = PHASE_OFFSET + COEFF_ILLUM × (TILLUM – TILLUM_CALIB) + COEFF_SENSOR × (TSENSOR – TSENSOR_CALIB). Phase correction is added to the phase output. Signed, twos complement.

7.5.1.1.47 Register F7h (address = F7h) [reset = 0h]

Figure 66. Register F7h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	COEFF_ILLUM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
COEFF_ILLUM							
R/W-0h							
7	6	5	4	3	2	1	0
COEFF_ILLUM							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 74. Register F7h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	R/W	0h	Always read or write 0.
16-0	COEFF_ILLUM	R/W	0h	Phase correction = PHASE_OFFSET + COEFF_ILLUM × (TILLUM – TILLUM_CALIB) + COEFF_SENSOR × (TSENSOR – TSENSOR_CALIB). Phase correction is added to the phase output. Signed, twos complement.

7.5.1.1.48 Register F8h (address = F8h) [reset = 0h]

Figure 67. Register F8h

23	22	21	20	19	18	17	16
SCRATCH1							
R/W-0h							
15	14	13	12	11	10	9	8
TILLUM_CALIB							
R/W-0h							
7	6	5	4	3	2	1	0
TSENSOR_CALIB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 75. Register F8h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	SCRATCH1	R/W	0h	Used as a scratch register
15-8	TILLUM_CALIB	R/W	0h	Phase correction = PHASE_OFFSET + COEFF_ILLUM × (TILLUM – TILLUM_CALIB) + COEFF_SENSOR × (TSENSOR – TSENSOR_CALIB). Phase correction is added to the phase output.
7-0	TSENSOR_CALIB	R/W	0h	Phase correction = PHASE_OFFSET + COEFF_ILLUM × (TILLUM – TILLUM_CALIB) + COEFF_SENSOR × (TSENSOR – TSENSOR_CALIB). Phase correction is added to the phase output.

7.5.1.1.49 Register F9h (address = F9h) [reset = 80000h]

Figure 68. Register F9h

23	22	21	20	19	18	17	16
0	0	0	0	FLIP_PHASE	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
0	0	0	PHASE_CORR_1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE_CORR_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 76. Register F9h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	R/W	0h	Always read or write 0.
19-19	FLIP_PHASE	R/W	1h	Set to 1 to obtain increasing phase with distance.
18-13	0	R/W	0h	Always read or write 0.
12-0	PHASE_CORR_1	R/W	0h	Phase correction for base frame. This value is added to the obtained phase. Signed, twos complement. Min = –2048 Max = 2047

7.5.1.1.50 Register FBh (address = FBh) [reset = 1E008h]

Figure 69. Register FBh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
1	1	1	0	DEALIAS_EN	ALT_FREQ_SEL		
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUB_FRAME_CNT_MAX2							ALT_FRM_EN
R/W-4h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 77. Register FBh Field Descriptions

Bit	Field	Type	Reset	Description
23-12	30	R/W	1Eh	Always read or write 30.
11	DEALIAS_EN	R/W	0h	When set to 1, enables computation of de-aliased data using the combination of two successive frames. ALT_FRM_EN and ALT_FREQ_SEL must be set.
10-8	ALT_FREQ_SEL	R/W	0h	Ratio of alternate frequency to the base frequency. 0 = 2 1 = 4 2 = 8 3 = 16 4 = 32 5 = 64 6 = 0 7 = 1
7-1	SUB_FRAME_CNT_MAX2	R/W	4h	Total number of sub-frames in each supplementary frame. Only values that are powers of 2 are valid. Behavior is unpredictable when set to other values. Max = 32
0	ALT_FRM_EN	R/W	0h	Enables alternate frames with a different set of sub-frames, integration duty cycle, and frequency.

7.5.1.1.51 Register FEh (address = FEh) [reset = 21090Fh]

Figure 70. Register FEh

23	22	21	20	19	18	17	16
0	0	1	0	0	0	0	1
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
0	0	0	0	1	0	0	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
0	0	STATISTICS_EN	0	1	1	1	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 78. Register FEh Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	R/W	0h	These rows had been lumped together as Field = 33828 and reset = 8424h, please adjust this to follow the standard
21	1	R/W	1h	Always read or write 1.
20-17	0	R/W	0h	Always read or write 0.
16	1	R/W	1h	Always read or write 1.
15-12	0	R/W	0h	Always read or write 0.
11	1	R/W	1h	Always read or write 1.
10-9	0	R/W	0h	Always read or write 0.
8	1	R/W	1h	Always read or write 1.
7-6	0	R/W	0h	Always read or write 0.
5-5	STATISTICS_EN	R/W	0h	When set to 1, enables statistics instead of flags in the data stream.
4-0	15	R/W	Fh	Always read or write 15.

8 Application and Implementation

NOTE

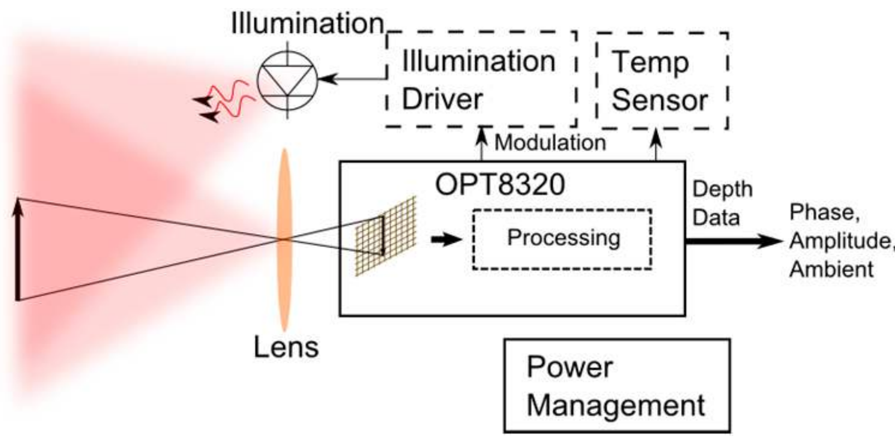
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

ToF cameras provide the complete depth map of a scene. In contrast with the scanning type light detection and ranging (LIDAR) systems, the depth map of the entire scene is captured at the same moment with an array of time-of-flight (ToF) pixels. A broad classification of applications for a 3D camera include:

- Presence detection
- Object location
- Movement detection
- 3D scanning

The OPT8320 sensor provides a fully-integrated solution for depth sensing. Apart from being a single-chip solution, the OPT8320 is highly configurable and thus lends itself to a wide gamut of applications. The relatively large pixel size of 30 µm (combined with a large well capacity and shutter operation) offers excellent dynamic range, allowing for both indoor and outdoor solutions. A small sensor format of 1/6" enables systems with very low profile height. Fast readout speeds up to 1000 frames per second (FPS) also enable applications that are very sensitive to motion blur. The block diagram of a complete 3D ToF camera implementation using the OPT8320 is illustrated in Figure 71.



(1) The external illumination driver is optional. The OPT8320 can modulate up to 150 mA of peak current directly.

(2) The external temperature sensor is optional. This sensor is typically implemented when an external illumination driver is used.

Figure 71. Application Block Diagram

Application Information (continued)

In order to feasibly perform a quick application analysis, TI provides the ToF system estimator tool that can be used to estimate the performance of a ToF camera with various configurations. The estimator allows control of the following parameters:

- Depth resolution
- 2D resolution (number of pixels)
- Distance range
- Frame rate
- Field of view (FoV)
- Ambient light (in watts × nm × m^2 around the sensor filter bandwidth)
- Reflectivity of the objects

For more details on how to select the above parameters, see the ToF system design guide.

8.2 Typical Applications

3D imaging using ToF lends itself to use in a wide gamut of applications. This section covers only a few of the many example applications with the intent of explaining the design procedure. For more details on applications, visit the TI 3D ToF landing page.

8.2.1 Gesture Recognition

Gesture recognition is a requirement for augmented or virtual reality systems to enable interaction with virtual objects. Mobile phones, tablets, and computers can also make use of gesture recognition in order to provide a more natural user interaction. Besides already currently functioning as remote controls, mobile phones can also be used as gesture input devices to control other systems such as TVs, projectors, and miscellaneous home appliances. Most of these examples require short-range gesture recognition. This use case is shown in Figure 72.

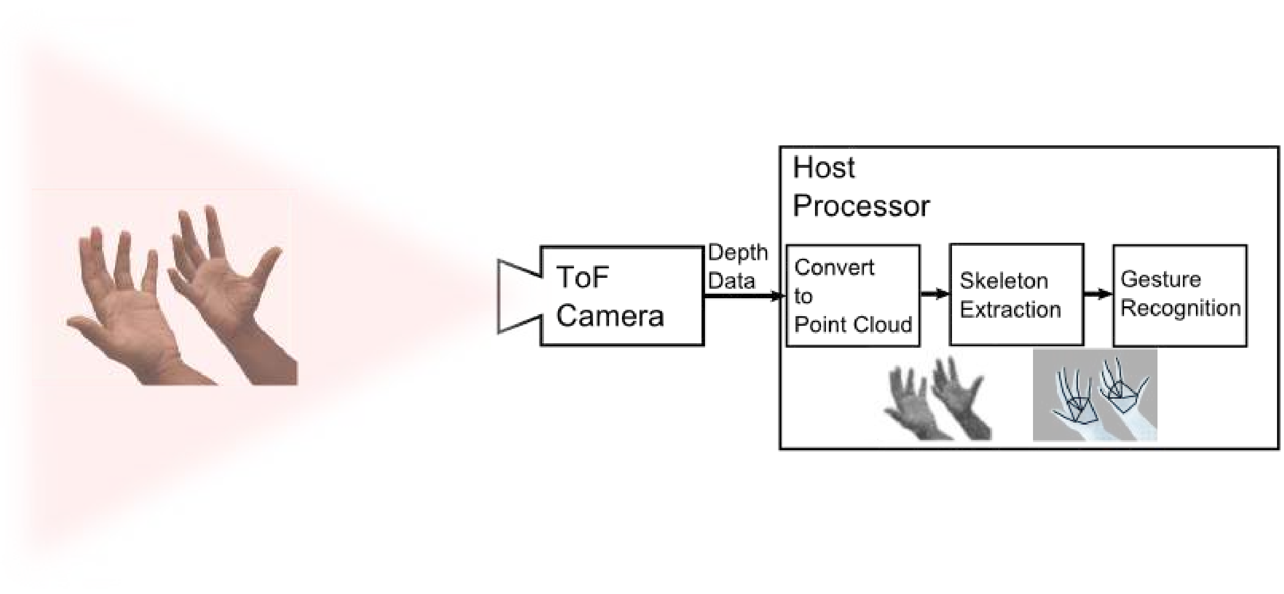


Figure 72. Short-Range Gesture Recognition

8.2.1.1 Design Requirements

The short-range gesture recognition requirements are listed separately in Table 79 and Table 80. Since gesture recognition is needed both indoors and outdoors, trade-offs have been made so that the same hardware (including illumination) can be used for both indoor and outdoor applications. The indoor and outdoor modes can be set by simply reconfiguring the OPT8320 timing parameters.

Typical Applications (continued)

Table 79. Indoor Gesture Recognition

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	10	mm	Temporal standard deviation of measured distance without the use of any software filters
Frame rate	60	Frames per second	For capturing fast hand or finger movements
Field of view	74.4 × 59.3	Degrees (H × V)	Example only, requirements may vary
Minimum distance	0.1	Meters	Example only, requirements may vary
Maximum distance	0.5	Meters	Example only, requirements may vary
Minimum reflectivity of objects at which the depth resolution is specified	40	Percentage	Assuming Lambertian reflection
Number of pixels	80 × 60	Rows x columns	Using a full array
Ambient light	0	W × nm × m^2 around 850 nm	Indoor lighting
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

Table 80. Outdoor Gesture Recognition

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	25	mm	Temporal standard deviation of measured distance without the use of any software filters
Frame rate	30	Frames per second	For capturing medium speed hand or finger movements
Field of view	74.4 × 59.3	Degrees (H × V)	Example only, requirements may vary
Minimum distance	0.1	Meters	Example only, requirements may vary
Maximum distance	0.5	Meters	Example only, requirements may vary
Minimum reflectivity of objects at which the depth resolution is specified	40	Percentage	Assuming Lambertian reflection
Number of pixels	80 × 60	Rows x columns	Using a full array
Ambient light	0.5	W × nm × m^2 around 850 nm	Almost clear skies, bright sunny day during the mornings and evenings
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

8.2.1.2 Detailed Design Procedure

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained. The choice of inputs to the estimator tool is explained in this section.

8.2.1.2.1 Frequencies of Operation

The frequencies of operation are limited by the sensor bandwidth because the illumination source is a laser. Frequencies around 70 MHz to 75 MHz can be used to obtain a good demodulation figure of merit. Because this is a short-range application, de-aliasing is not required and a single frequency of operation is sufficient. 72 MHz is chosen as the operating frequency for this example. The unambiguous range is now given by Equation 22:

$$Unambiguous\ Range = \frac{C}{2 \times f} = \frac{299792458.0\ m/s}{2 \times 72MHz} = 2.08m \quad (22)$$

8.2.1.2.2 Number of Sub-Frames and Quads

For the case of indoor gesture recognition, only one sub-frame and four quads are used. Using minimal sub-frames minimizes system noise and allows the use of minimum optical peak and average powers. On the other hand, for the case of outdoor gesture recognition, eight sub-frames are used to make sure that the sensor does not saturate because of high ambient light.

8.2.1.2.3 Integration Duty Cycle

For the indoor case, duty cycle is adjusted to minimize the peak power consumption. If an application requires only indoor operation, peak optical powers below 150 mW can be obtained using just a single laser diode and the internal illumination driver to minimize cost. For the outdoor case, duty cycle is minimized to avoid saturation resulting from high ambient and keeps the peak optical power levels below 300 mW. Dual lasers with an internal illumination driver or a single laser with an external illumination driver can be used for a 300-mW peak optical power operation. In this example, if the system has both indoor and outdoor applications, the outdoor requirements have a greater bearing on the system design because of the higher peak power requirements.

8.2.1.2.4 Field of View (FoV)

Field of view in the horizontal direction is 74.4 degrees. The diagonal FoV can be calculated using Equation 23.

$$FoV\,(Diagonal) = 2 \times tan^{-1}\left[\frac{5}{4} \times tan\left(\frac{74.4°}{2}\right)\right] \approx 87° \tag{23}$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.1.2.5 Lens

A lens with a 1/6” image circle must be chosen. The FoV of the lens must match the requirements (that is, the FoV must be equal to 87 degrees, as calculated in Equation 23). A lower f.no is always better. For this example, use an f.no of 1.2.

8.2.1.2.6 Design Summary

Screen shots of the system estimator tool are provided in Figure 73 and Figure 74.

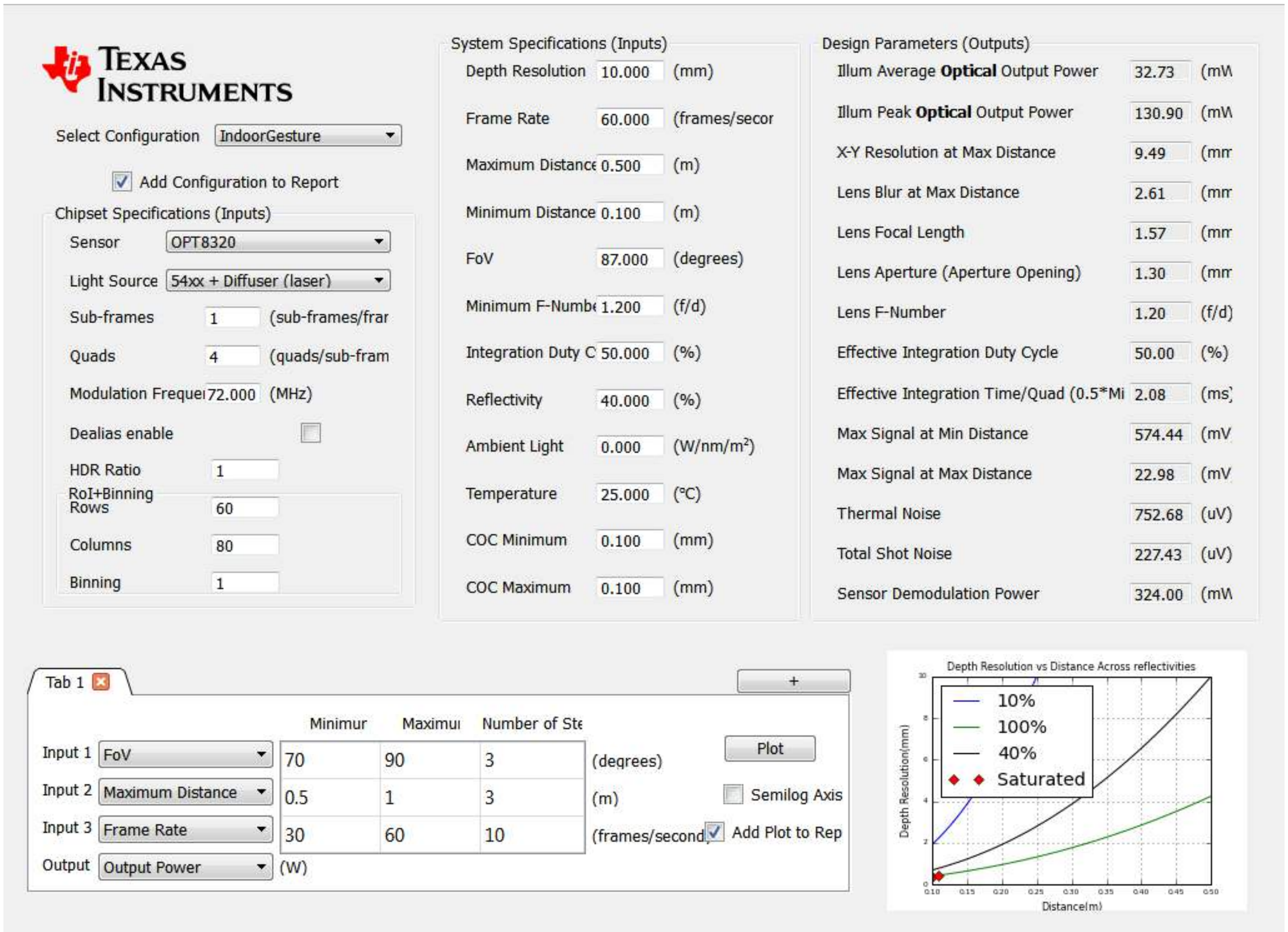


Figure 73. Indoor Gesture Recognition: Screen Shot of the Estimator Tool

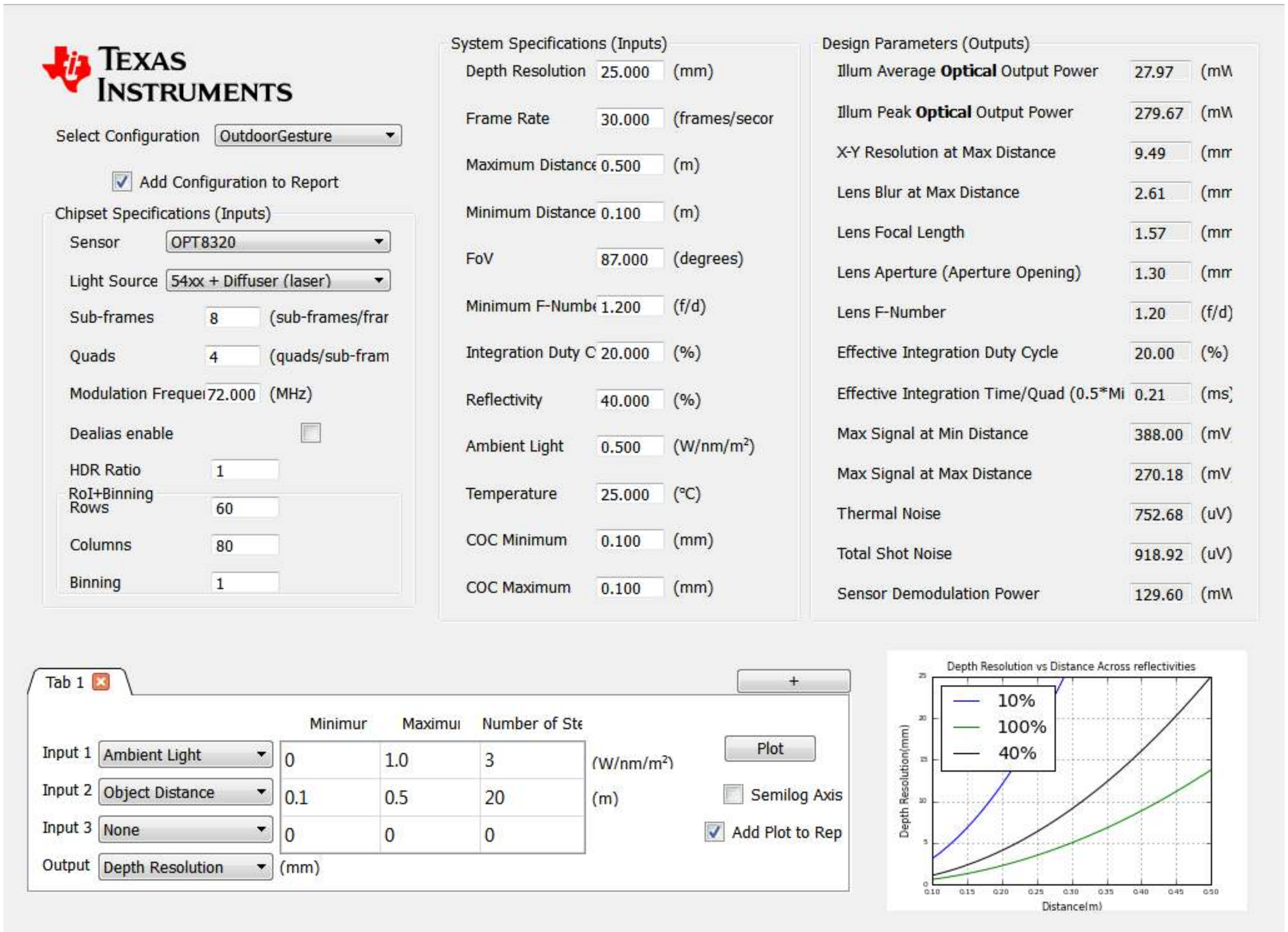
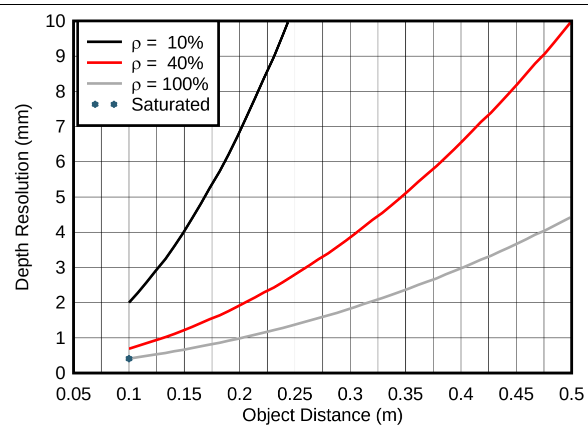


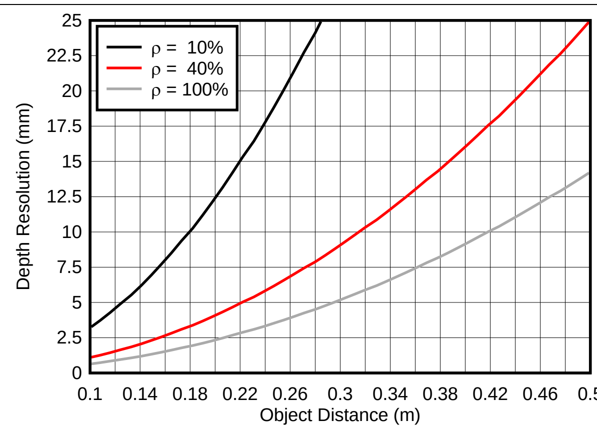
Figure 74. Outdoor Gesture Recognition: Screen Shot of the Estimator Tool

8.2.1.3 Application Curves



ρ represents object reflectivity

Figure 75. Indoor Gesture Recognition: Depth Resolution vs Object Distance



ρ represents object reflectivity

Figure 76. Outdoor Gesture Recognition: Depth Resolution vs Object Distance

8.2.2 Collision Avoidance

Autonomous vehicles are becoming increasingly popular for both industrial and home uses. For both robots on the ground and for air-borne drones, collision avoidance is a necessary feature. The fast readout rate that the OPT8320 offers makes the device a natural fit for collision avoidance applications because minimum latency is a critical parameter. The use case for this application is shown in Figure 77.

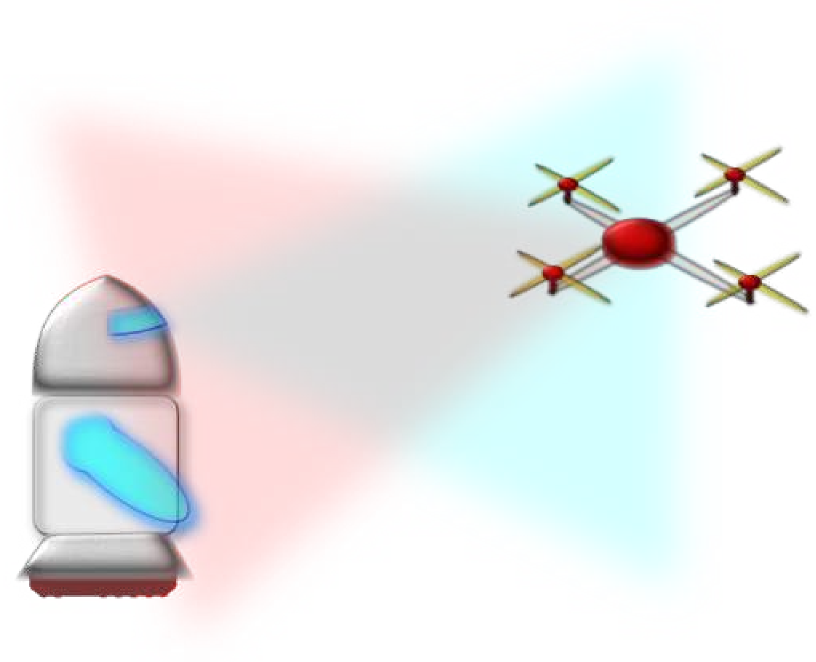


Figure 77. Collision Avoidance

8.2.2.1 Design Requirements

The outdoor example is illustrated in this application because many of the collision avoidance applications are outdoor in nature. The indoor use-case, in comparison, requires lower power. The critical system parameters are listed in Table 81.

Table 81. Collision Avoidance

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	450	mm	Temporal standard deviation of measured distance at maximum distance without the use of any software filters
Frame rate	30	Frames per second	For ensuring minimal latency
Field of view	77.3 × 61.9	Degrees (H × V)	Example only, requirements may vary
Minimum distance	0.3	Meters	Example only, requirements may vary
Maximum distance	4.0	Meters	Example only, requirements may vary
Minimum reflectivity of objects at which the depth resolution is specified	40	Percentage	Assuming Lambertian reflection
Number of pixels	80 × 60	Rows x columns	Using a full array
Ambient light	1	W × nm × m^2 around 850 nm	Full sunlight at noon.
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

8.2.2.2 Detailed Design Procedure

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained. The choice of inputs to the estimator tool is explained in this section.

8.2.2.2.1 Frequencies of Operation

The frequencies of operation are limited by the sensor bandwidth because the illumination source is a laser. Frequencies around 70 MHz to 75 MHz can be used to obtain a good demodulation figure of merit. 72 MHz is chosen as the base operating frequency for this example. The de-aliasing frequency is chose as 9 MHz to extend the range by 8X. The unambiguous range is now given by Equation 24:

$$Unambiguous\ Range = \frac{C}{2 \times f} = \frac{299792458.0\ m/s}{2 \times 9\ MHz} = 16.66m \tag{24}$$

8.2.2.2.2 Number of Sub-Frames and Quads

Because this example shows the case of outdoor collision avoidance in the presence of mid-day sunlight, eight sub-frames are used to make sure that the sensor does not saturate as a result of high ambient light. Also, eight equivalent quads are required for de-aliasing using two frequencies.

8.2.2.2.3 Integration Duty Cycle

Because this is an outdoor application, duty cycle is minimized to avoid saturation resulting from high ambient and keeps the peak optical power levels as low as possible to accommodate single, high-power laser operation.

8.2.2.2.4 Field of View (FoV)

Field of view in the horizontal direction is 77.3 degrees. The diagonal FoV can be calculated using Equation 25.

$$FoV\ (Diagonal) = 2 \times tan^{-1}\left[\frac{5}{4} \times tan\left(\frac{77.3°}{2}\right)\right] \approx 90° \tag{25}$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.2.2.5 Lens

A lens with a 1/6” image circle must be chosen. The FoV of the lens must match the requirements (that is, the FoV must be equal to 90 degrees, as calculated in Equation 25). A lower f.no is always better. For this example, use an f.no of 1.2.

8.2.2.2.6 Design Summary

A screen shot of the system estimator tool is shown in Figure 78.

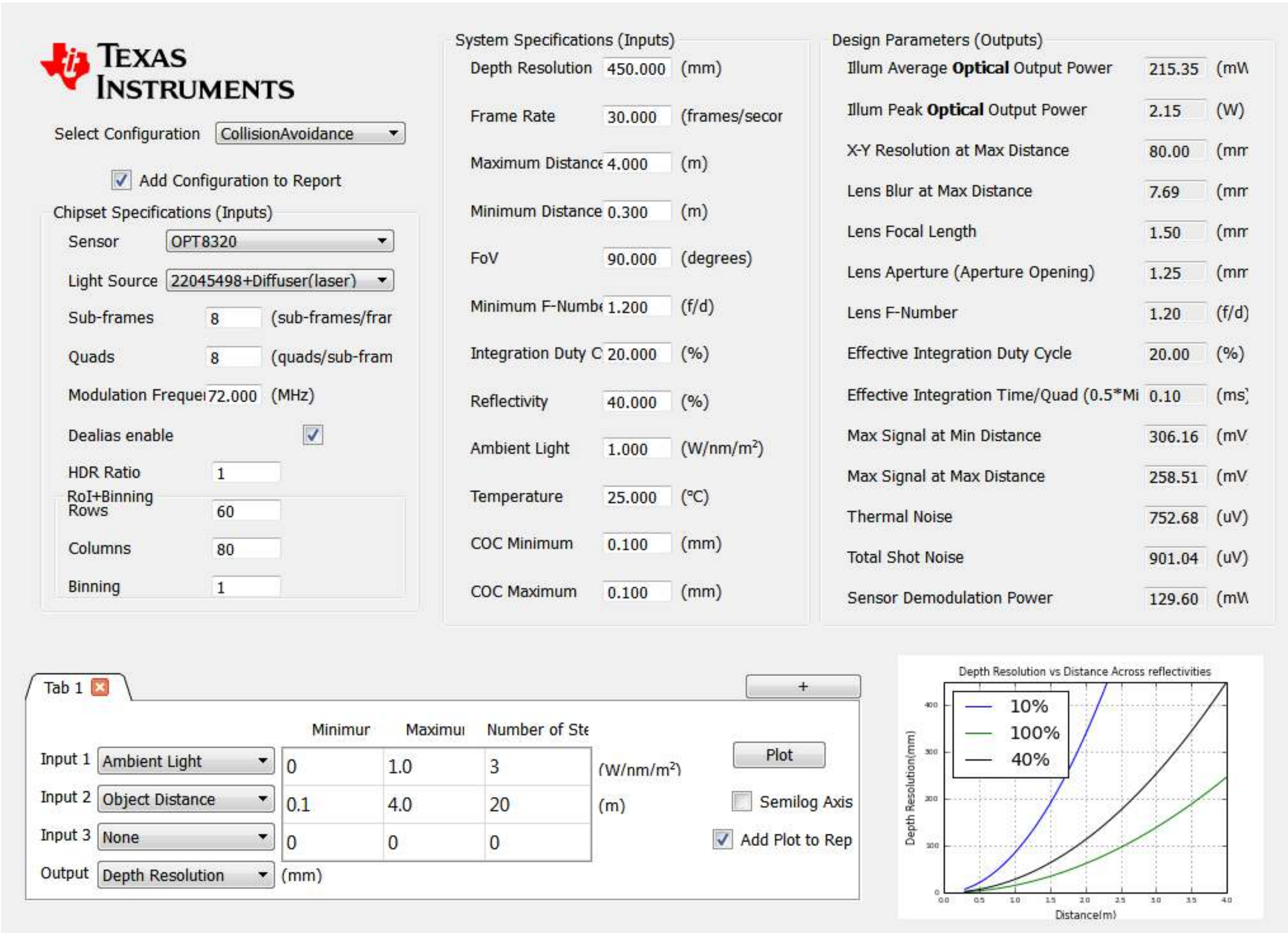
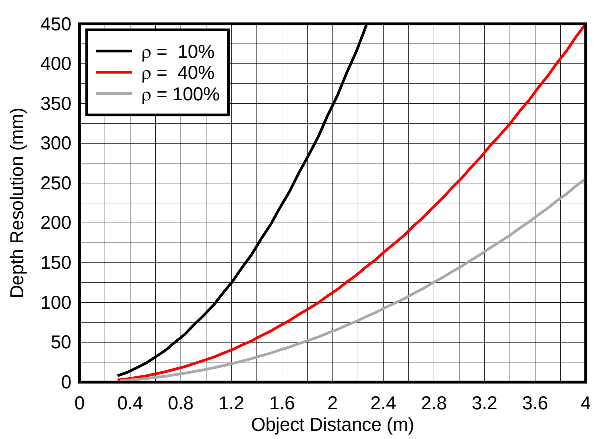


Figure 78. Outdoor Collision Avoidance: Screen Shot of the Estimator Tool

8.2.2.3 Application Curve



ρ represents object reflectivity

Figure 79. Outdoor Collision Avoidance: Depth Resolution vs Object Distance

8.2.3 Autofocus

Mobile phones, point-and shoot-cameras, and even digital single-lens reflex cameras (DSLRs) need assistance for fast focus. The time taken to focus must ideally be less than 100 ms so that the lag is not felt by the user. Fast focus is especially challenging in low light when the contrasts in the image are low. This example demonstrates a near-range, 70-point, auto-focus assistance using just the OPT8320 internal illumination driver and a single laser for mobile and point-and-shoot camera applications. The illustration of the system is shown in Figure 80.

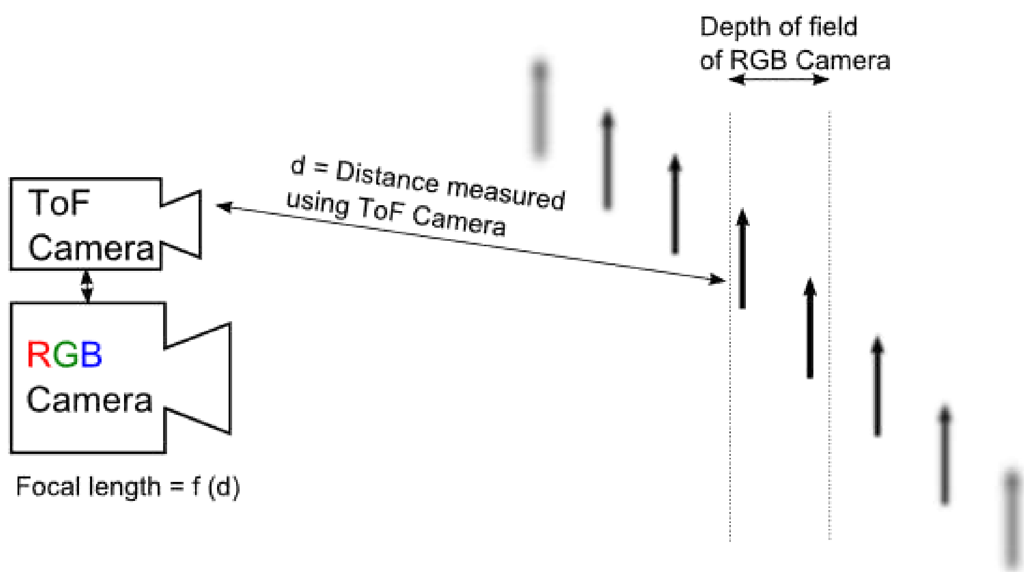


Figure 80. Autofocus

8.2.3.1 Design Requirements

A resolution of 10% for object distance is selected for the maximum distance of operation because depth of field (DoF) is relatively wide for most small-sensor cameras. At lower distances, the resolution is relatively better. The requirements are listed in Table 82.

Table 82. Autofocus

SPECIFICATION	VALUE	UNITS	COMMENTS
Depth resolution	300	mm	Temporal standard deviation of measured distance at maximum distance without the use of any software filters
Frame rate	20	Frames per second	For capturing the image in less than 50 ms
Field of view	54.0 × 41.8	Degrees (H × V)	Example only, requirements may vary (35-mm equivalent focal length for full-frame sensor FoV)
Minimum distance	0.25	Meters	Example only, requirements may vary
Maximum distance	3.0	Meters	Example only, requirements may vary
Minimum reflectivity of objects at which the depth resolution is specified	40	Percentage	Assuming Lambertian reflection
Number of pixels	10 × 7	Rows x columns	Using a full array with 8x8 pixel binning
Ambient light	0.5	W × nm × m^2 around 850 nm	Optimized for outdoor lighting. Works indoors with increased performance.
Illumination source	Laser	—	Laser + diffuser for diffusing light uniformly through the scene

8.2.3.2 Detailed Design Procedure

Using the TI ToF estimator tool, the ToF camera design requirements can be input and the power numbers required for achieving the desired specifications can be obtained. The choice of inputs to the estimator tool is explained in this section.

8.2.3.2.1 Frequencies of Operation

The frequencies of operation are limited by the sensor bandwidth because the illumination source is a laser. Frequencies around 70 MHz to 75 MHz can be used to obtain a good demodulation figure of merit. 72 MHz is chosen as the base operating frequency for this example. The de-aliasing frequency is chosen as 18 MHz to extend the range by 4X. The unambiguous range is now given by Equation 26:

$$Unambiguous\ Range = \frac{C}{2 \times f} = \frac{299792458.0\ m/s}{2 \times 18\ MHz} = 8.33m \tag{26}$$

8.2.3.2.2 Number of Sub-Frames and Quads

Because this example can be used even in outdoor autofocus applications, four sub-frames are used to make sure that the sensor does not saturate resulting from high ambient light. Also, eight equivalent quads are required for de-aliasing using two frequencies.

8.2.3.2.3 Integration Duty Cycle

Because autofocus can be potentially used even in outdoor conditions, duty cycle is minimized to avoid saturation resulting from high ambient and keeps the peak optical power levels as low as possible to accommodate single, high-power laser operation.

8.2.3.2.4 Field of View (FoV)

Field of view in the horizontal direction is 54 degrees. The diagonal FoV can be calculated using Equation 25.

$$FoV\ (Diagonal) = 2 \times tan^{-1}\left[\frac{5}{4} \times tan\left(\frac{54}{2}\right)\right] \approx 65\ Degrees \tag{27}$$

The ratio of 5/4 is used to represent the ratio of the diagonal length to the horizontal length of the sensor.

8.2.3.2.5 Lens

A lens with a 1/6” image circle must be chosen. The FoV of the lens must match the requirements (that is, the FoV must be equal to 65 degrees, as calculated in Equation 25). A lower f.no is always better from a depth resolution point of view, but profile height is very important in this application and, therefore, a lens with a lower f.no of 2.4 is preferred to achieve a lower total track length (TTL).

8.2.3.2.6 Design Summary

A screen shot of the system estimator tool is shown in Figure 81.

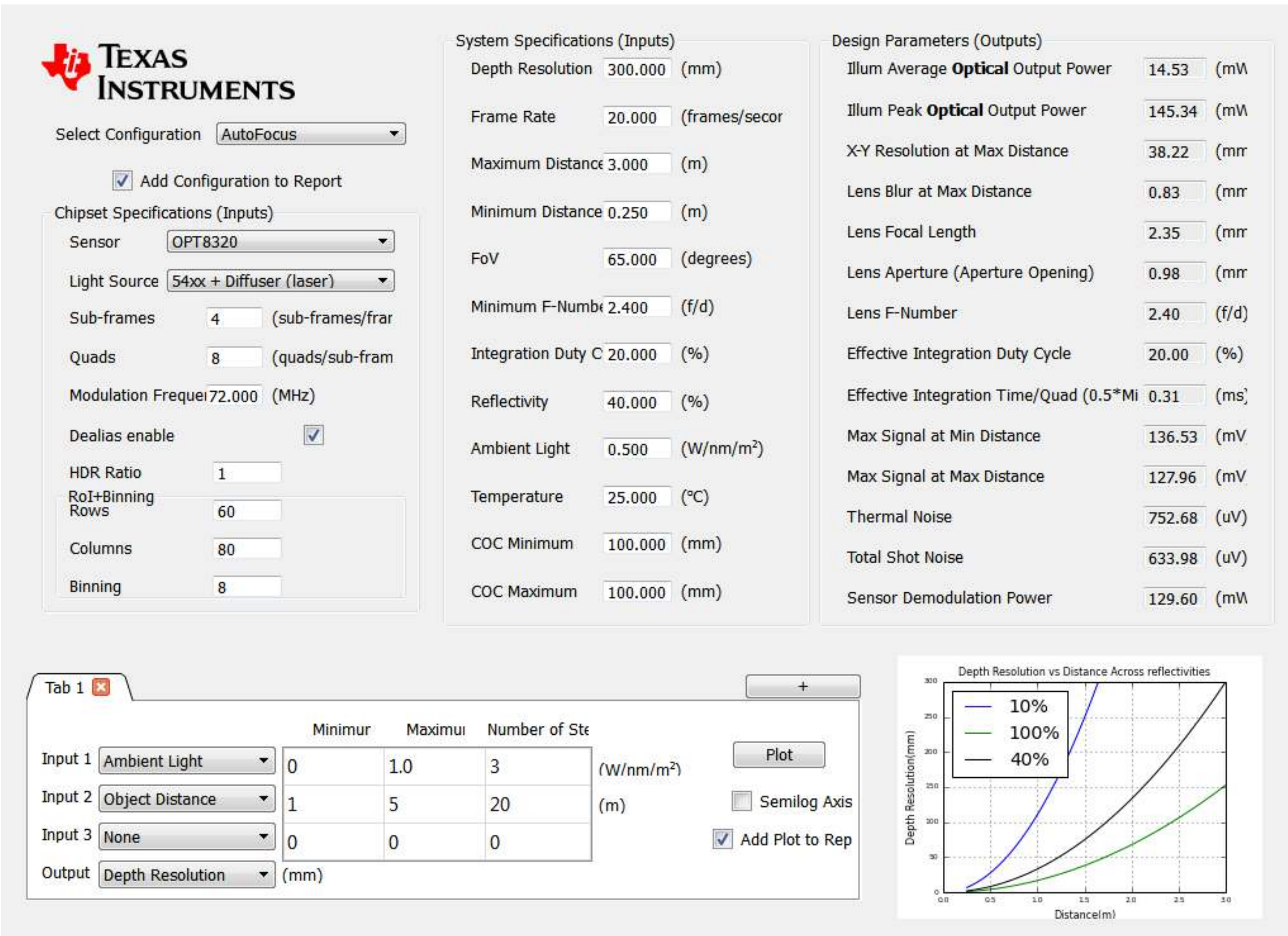
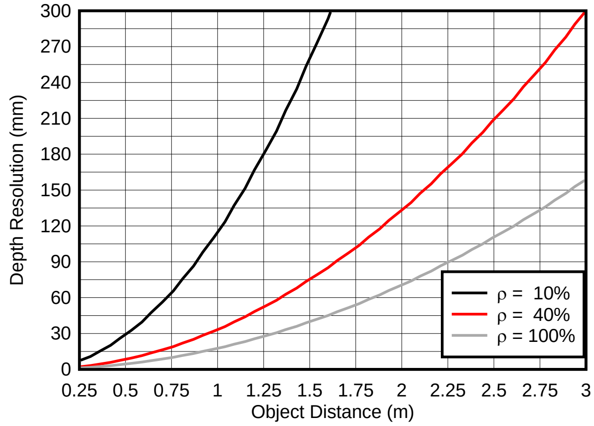


Figure 81. Autofocus Application: Screen Shot of the Estimator Tool

8.2.3.3 Application Curve



ρ represents object reflectivity

Figure 82. Autofocus Application: Depth Resolution vs Object Distance

8.3 Initialization Set Up

The following initialization sequence must be followed after power-up for proper functionality of the device:

- Hold the device in reset by pulling the $\overline{\text{RESET}}$ pin low.
- Release reset. The device will be in standby mode.
- Enable the timing generator by setting the TG_EN parameter to 1.
- Remove the device from standby mode by setting the STANDBY parameter to 0.
- Disable the timing generator by setting the TG_EN parameter to 0.
- Set INIT_0 to 0Ah for proper functionality.
- Set INIT_1 to 0Ah for proper functionality.
- Set INIT_2 to 01h for proper functionality.
- Set UPDATE_SEL to 02h for proper functionality in master mode and 00h in slave mode.
- Set the EN_DYN_PDN parameter to 1 to enable dynamic power-down (optional).
- Set the SHUTTER_EN parameter to 1 in case of high ambient applications (optional).
- Set the timing parameters as per the system requirements.
- If the built-in illumination driver is used, set MOD_CDRIV_EN to 1 and set MOD_CDRIV_CURR to the appropriate value.
- Enable the timing generator by setting the TG_EN parameter to 1.

9 Power Supply Recommendations

The sensor reset noise is sensitive to AVDDH and PVDD supplies. Therefore, linear regulators are recommended for supplying power to the AVDD and PVDD supplies. DC-DC regulators can be used to supply power to the rest of the supplies. Ripple voltage on the V_{MIX} and the SUB_BIAS supplies must be kept at a minimum (< 50 mV) to minimize phase noise resulting from differences between quads. The V_{MIX} regulator must have the bandwidth to supply surge current requirements within a short time of less than 10 µs after the integration period begins because V_{MIX} currents have a pulsed profile.

There is no strict order for the power-on or -off sequence. The V_{MIX} supplies are recommended to be turned on after all supplies have ramped to 90% of their respective values to avoid any power-up surges resulting from high V_{MIX} currents in a non-reset device state.

9.1 Example Power Consumption Numbers

Example power consumption numbers for various frame rates with dynamic power-down enabled are tabulated in Table 83. All specifications are at T_A = 25°C, V_{AVDDH} = 3.3 V, V_{AVDD} = 1.8 V, V_{VMIXH} = 1.8 V, V_{DVDD} = 1.8 V, V_{DVDDH} = 3.3 V, V_{PVDD} = 3.3 V, V_{IOVDD} = 3.3 V, V_{SUB_BIAS} = 0 V, integration duty cycle = 20%, system clock frequency = 24 MHz, modulation frequency = 48 MHz, quads = 4, and sub-frames = 4, unless otherwise noted.

Table 83. Power consumption details

FRAME RATE (FPS)	PVDD (mA)	AVDD (mA)	AVDDH (mA)	AVDD_PLL (mA)	DVDD (mA)	DVDDH (mA)	IOVDD (mA)	TOTAL POWER(1) (mW)
1	0.4	5.0	1.0	4	18.5	0.3	4.2	69.0
5	0.4	5.2	1.1	4	18.6	0.3	4.2	69.2
30	0.5	6.7	1.5	4	19.3	0.3	4.2	74.8
240	1.2	18.4	5.2	4	24.3	0.8	4.2	123.7

(1) Total power does not include MIXH power. MIXH power depends on integration time.

9.2 Power Trade-Off

The OPT8320 with its flexible timing and power-supply options, allows several trade-offs between performance and power. The most important parameters are:

- Integration duty cycle: V_{MIXH} power is active during integration time. Lower integration duty cycle results in lower power because V_{MIXH} demands very high currents. At the same time, to maintain the SNR of the system (if the integration duty cycle is reduced), the illumination peak power must be increased. Depending on the ratio of the illumination to the OPT8320 power, the trade-off may be different for each application because efficiency drops with higher peak powers. Also, in high ambient cases, reducing the integration duty cycle may be necessary to avoid saturation.
- V_{MIXH} voltage: In cases where best performance is critical irrespective of the power consumption, V_{MIXH} must be set to the highest voltage allowed. On the other hand, in power-critical, short-range applications, reducing V_{MIXH} reduces the system power consumption significantly.
- Substrate biasing: Although the current consumed on the SUB_BIAS rail is small compared to the power on the V_{MIXH} rail, the performance improvement is significant. The only downside in applying a negative voltage on the SUB_BIAS pin is the need for additional negative voltage regulators.
- Dynamic power-down: When this feature is enabled, the OPT8320 powers down sub-systems when not in use. This feature allows for lower power consumption, particularly in low frame rate cases.

10 Layout

10.1 Layout Guidelines

10.1.1 MIX Supply Decoupling Capacitors

The V_{MIXH} supply has a peak load current requirement of approximately 400 mA during the integration phase. Moreover, a break-before-make circuit is used during the reversal of the demodulation polarity to avoid high through currents. The break-before-make strategy results in a pulse with a drop and a subsequent rise of demodulation current. The pulse duration is typically approximately 1 ns. In order to effectively support the rise in currents, V_{MIXH} decoupling capacitors must be placed very close to the package. Furthermore, use multiple capacitors to reduce the effect of equivalent series inductance and resistance of the decoupling capacitors. Using a combination of 10-nF and 1-nF capacitors next to the V_{MIXH} pins is recommended, as shown in Figure 85 . Using vias for routing the trace from decoupling capacitors to the package pins must be avoided.

10.1.2 Internal Illumination Driver

The internal illumination driver is a current source driver. The illumination current loop length must be as small as possible because current must to rise and fall rapidly to ensure good optical rise and fall times, as shown in Figure 85. Also, the illumination current ground net (VSS_CDRIV) must be separated from the other ground nets using a ferrite bead.

10.1.3 Thermal Heat Sink and Underfill

Heat sinking must be done from the board side because the OPT8320 is an optical package. Underfill can be used to improve the heat dissipation of the device. The underfill used must be electrically non-conductive and must have good thermal conductance. Use of underfill also improves the board level reliability of the package.

10.1.4 Image Orientation and Optical Centering

The sensor orientation for obtaining an upright image is shown in Figure 83.

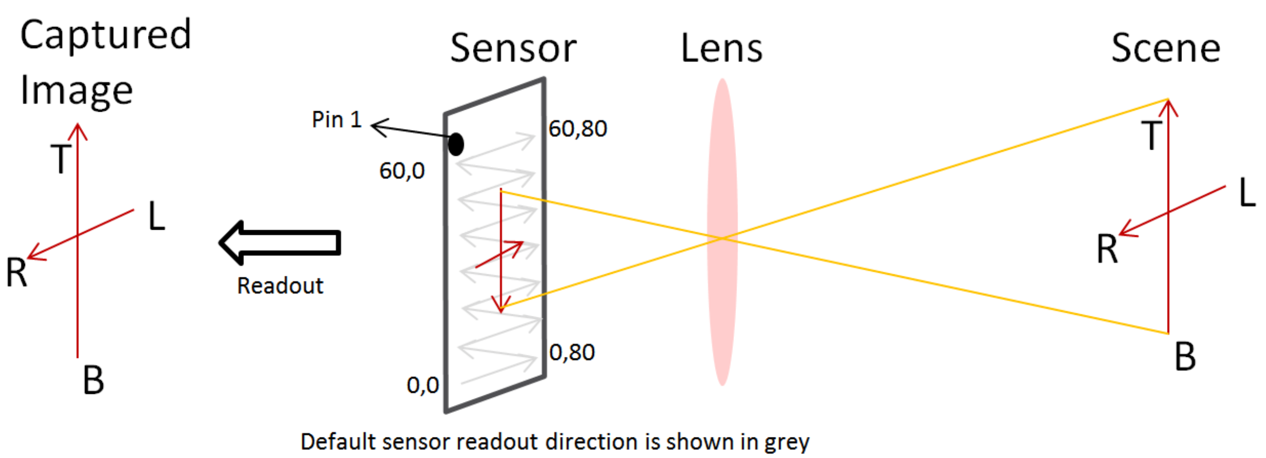


Figure 83. Sensor Orientation for Obtaining an Upright Image

Layout Guidelines (continued)

The pixel area and the location of the optical center with respect to the package center is shown in Figure 84.

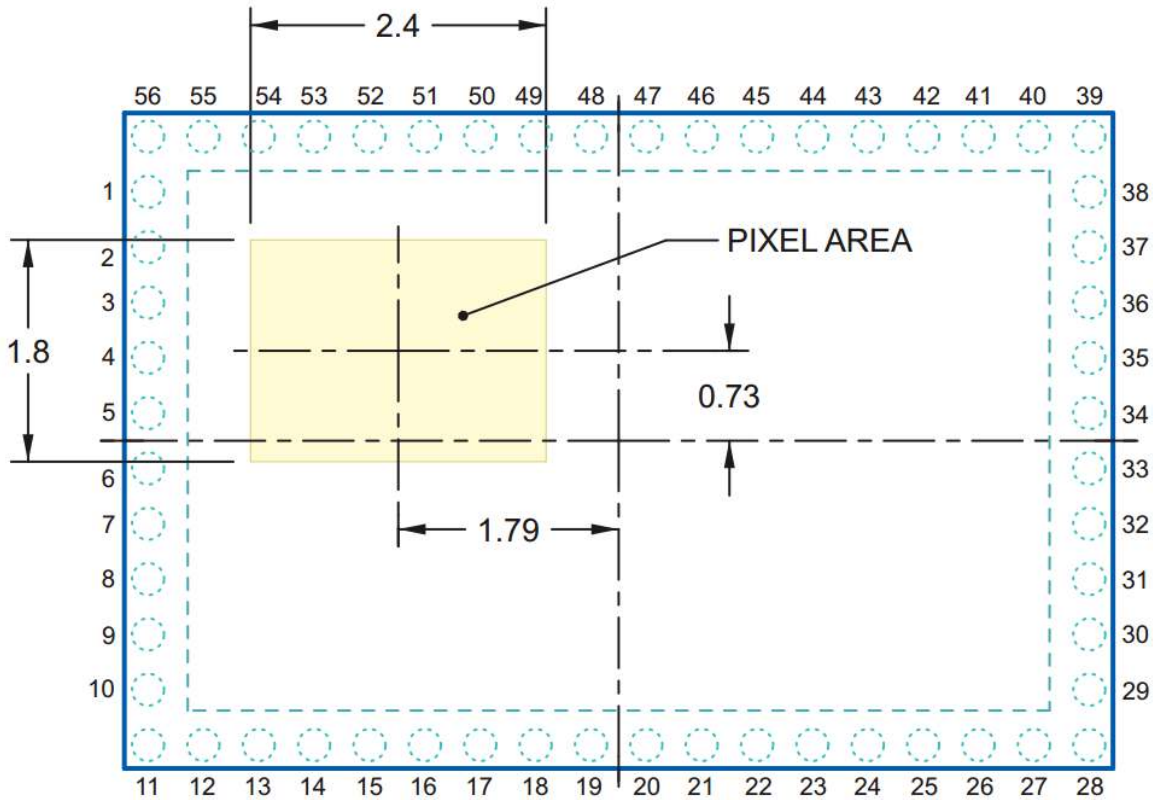


Figure 84. Pixel Area Position

10.2 Layout Example

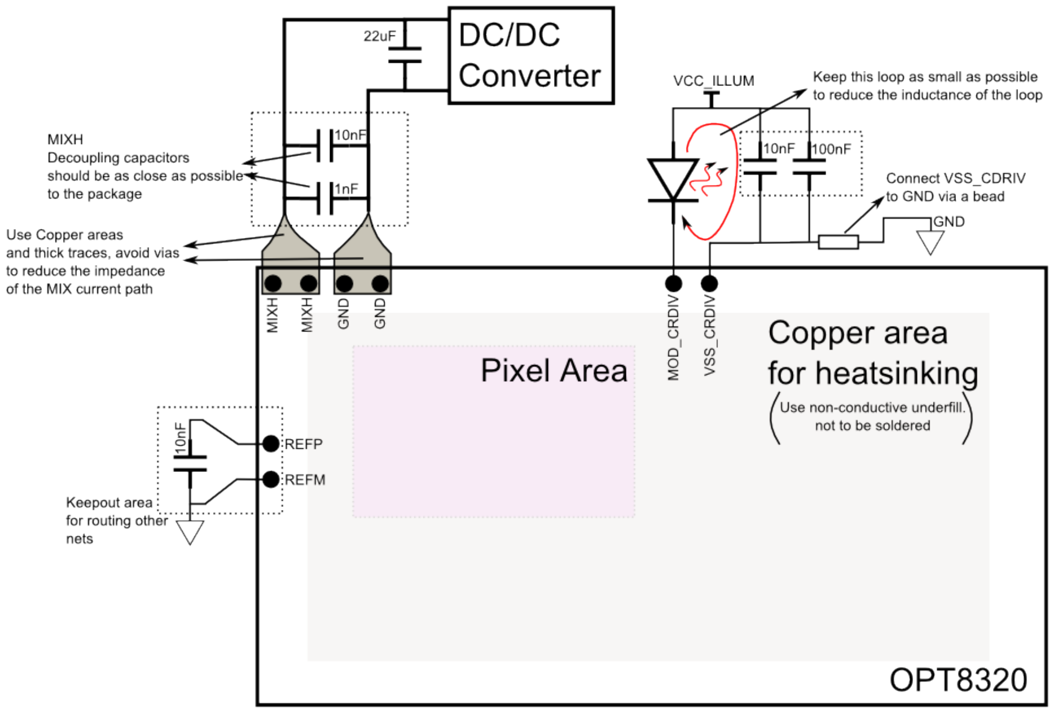


Figure 85. Layout Example

10.3 Mechanical Assembly Guidelines

10.3.1 Board-Level Reliability

TI chip-on-glass products are designed and tested with underfill to ensure board-level reliability. If a customer chooses to underfill a chip-on-glass product, the following guidelines are recommended to maximize board level reliability:

- The underfill material must extend partially up the package edges. Underfill that ends at the bottom (ball side) of the die degrades reliability.
- The underfill material must have a coefficient of thermal expansion (CTE) closely matched to the CTE of the solder interconnect.
- The underfill material must have a glass transition temperature (Tg) above the expected maximum exposure temperature.

Thermoset ME-525 is a good example of a compatible underfill.

10.3.2 Handling

To avoid dust particles on the sensor, the sensor tray must only be opened in a cleanroom facility. In case of accidental exposure to dust, the recommended method to clean the sensors is to use an isopropyl alcohol (IPA) solution with a micro-fiber cloth swab with no lint. Do not handle the sensor edges with hard or abrasive materials (such as metal tweezers) because the sensor package has a glass outline. Such handling may lead to cracks that can negatively affect package reliability and image quality.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

TMP103 Data Sheet, SBOS545

Time-of-Flight Camera – An Introduction, SLOA190

Introduction to the Time-of-Flight (ToF) System Design, SBAU219

3D ToF System Estimator Tool

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT8320NBP	ACTIVE	COG	NBP	56	300	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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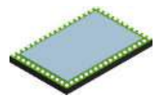
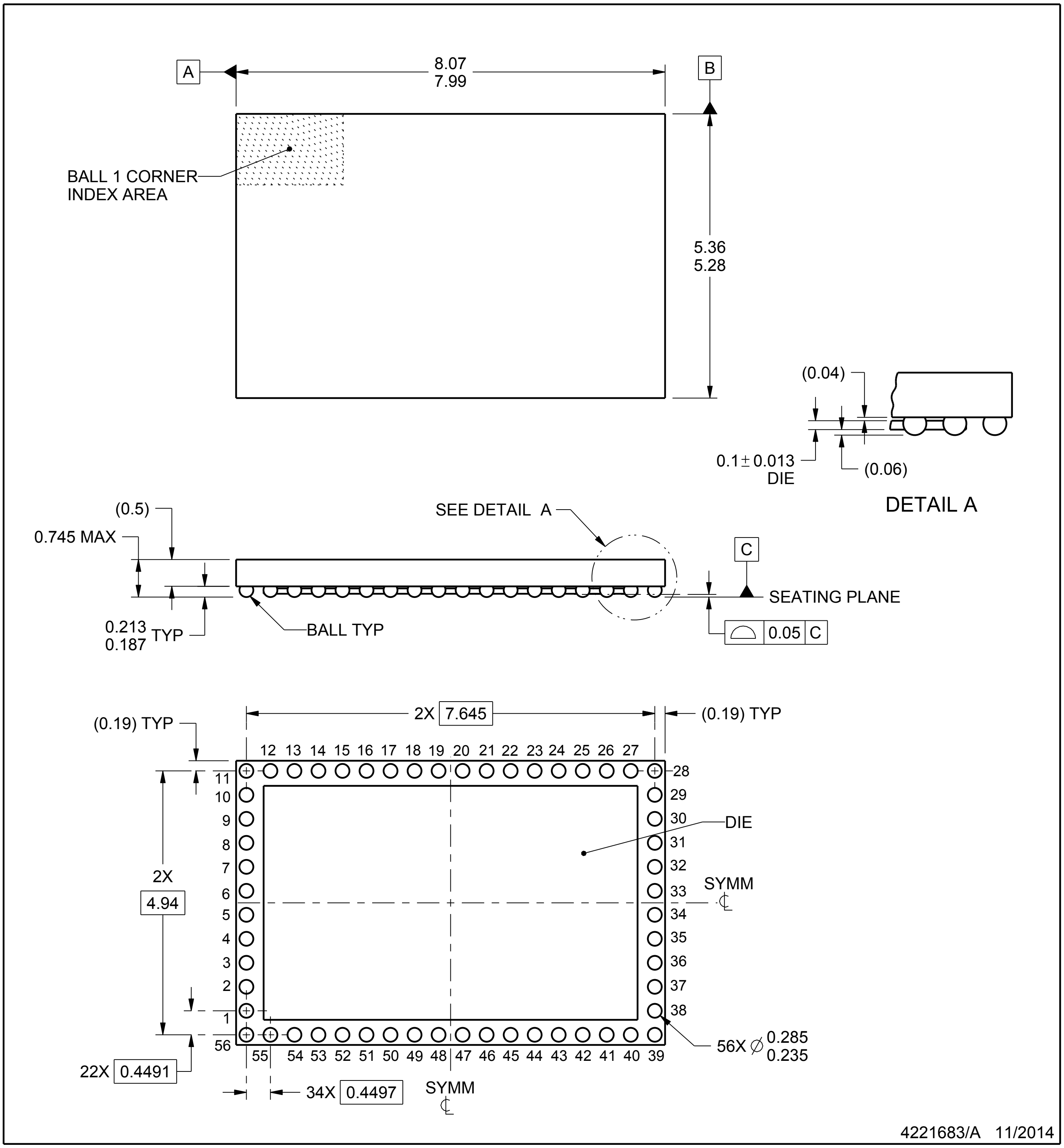
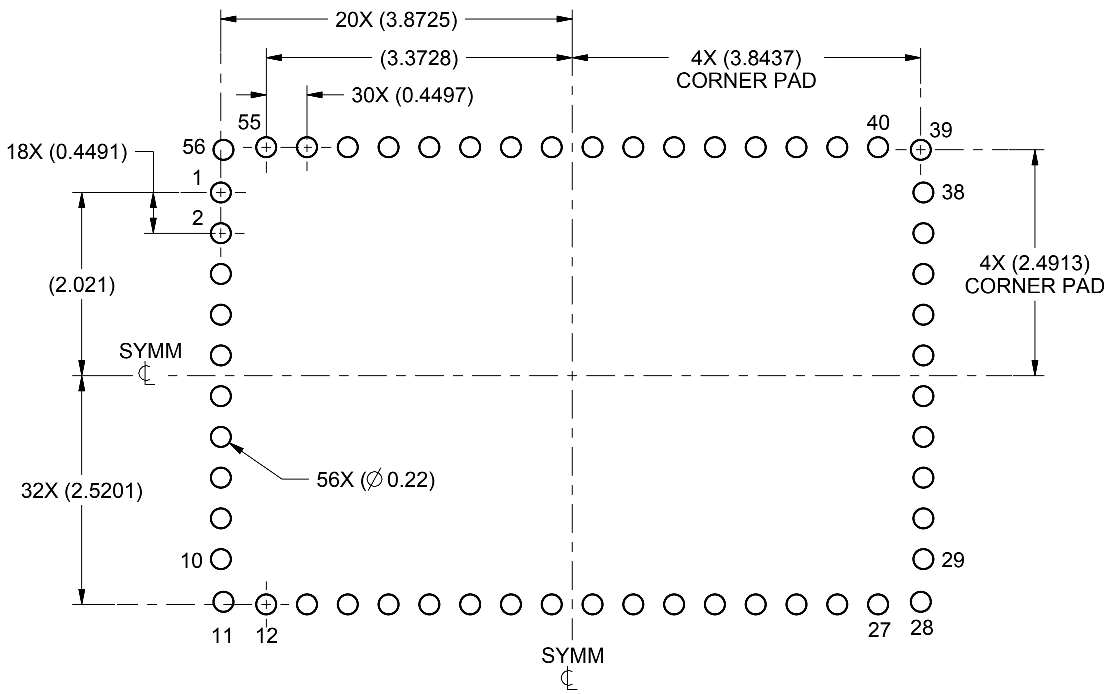


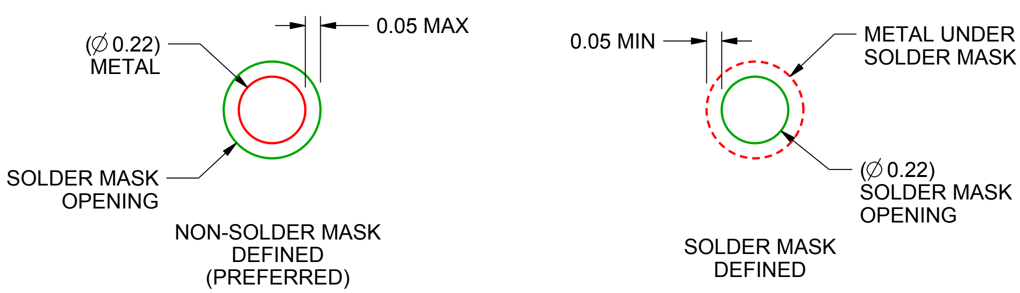


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.



LAND PATTERN EXAMPLE
SCALE:12X

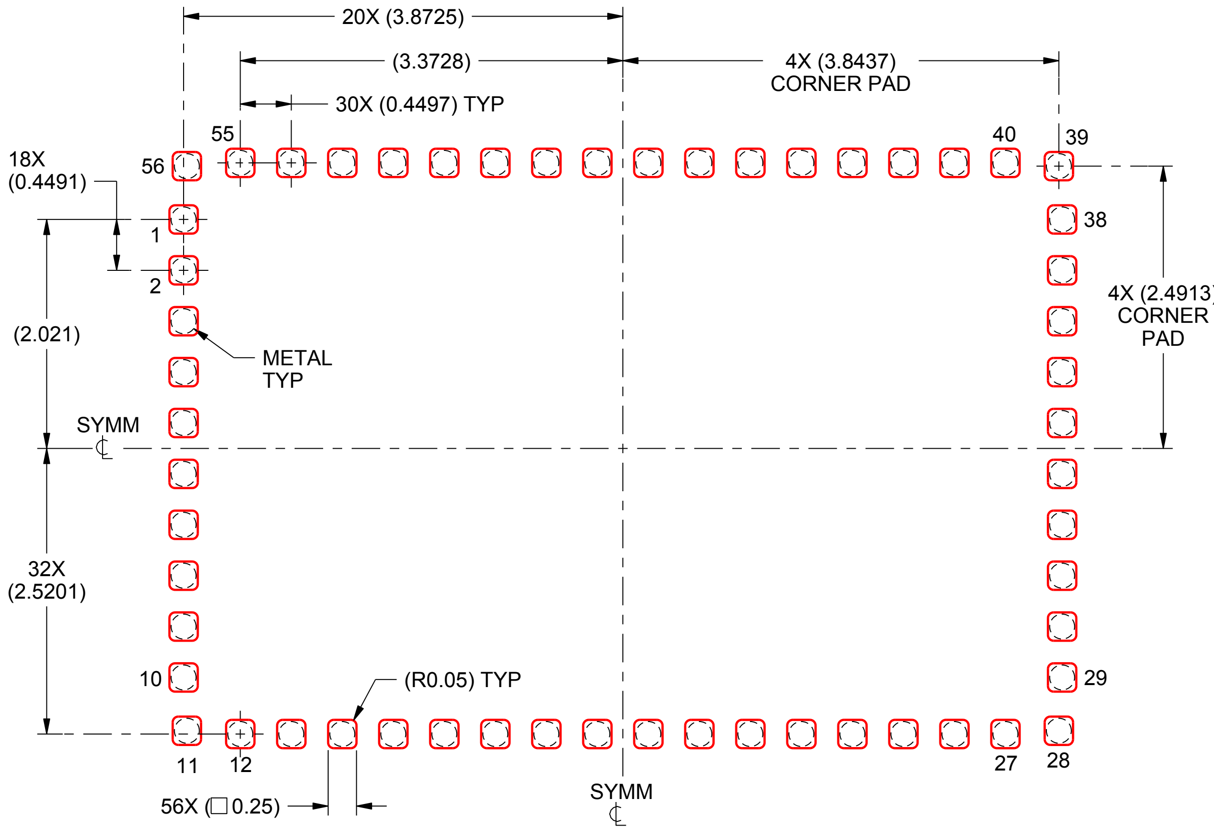


SOLDER MASK DETAILS
NOT TO SCALE

4221683/A 11/2014

NOTES: (continued)

5. PCB pads shift from original positions to prevent solder balls from touching sensor. X and Y direction: 0.05 mm. Corner pads: 0.03 mm.
6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:15X

4221683/A 11/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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