

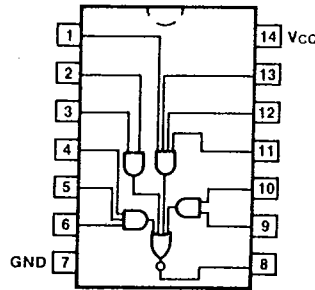
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T-43-15

54S/74S64

4-2-3-2-INPUT AND-OR-INVERT GATE

CONNECTION DIAGRAM PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C to } +70^\circ\text{ C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{ C to } +125^\circ\text{ C}$	
Plastic DIP (P)	A	74S64PC		9A
Ceramic DIP (D)	A	74S64DC	54S64DM	6A
Flatpak (F)	A	74S64FC	54S64FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	25/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS	
		Min	Max			
I_{CCH}	Power Supply Current		12.5	mA	$V_{IN} = \text{Gnd}$	$V_{CC} = \text{Max}$
I_{CCL}			16		**	
t_{PLH}	Propagation Delay	2.0	5.5	ns	Figs. 3-1, 3-4	
t_{PHL}		2.0	5.5			

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{ C}$ and $V_{CC} = +5.0\text{ V}$.
 ** I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.