



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

ASSP, 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC

S6BP202A is a 1-Ch Buck-boost DC/DC converter IC with four built-in switching FETs. This IC is able to supply up to 2.4A of load current within the very wide range from 2.5V to 42V in the input voltage. This IC has an operation mode that is automatically changed to PFM operation during low load, which can achieve super-high efficiency with a very low quiescent current 20 μ A. It is possible to provide stable output voltage from an automotive cold cranking and load dump, up to 42V, conditions within 1 ms transition time. As a result, this IC is suitable for power supply solutions of automotive and Industrial applications. This IC has the SYNC function, which is able to inputs an external clock signal. When an external clock signal in the range from 200 kHz to 400 kHz is inputted, the FETs perform the switching operation with synchronizing signal from an external clock. When an external clock signal is not inputted, the FETs perform the switching operation from an internal clock. The internal clock signal in the range from 200 kHz to 2.1 MHz can be set by an external resistor. Since external voltage setting resistors and phase compensation capacitors are not required with this IC, it can reduce the number of parts and a part mounting area. This IC has five protection functions, input under voltage lockout (input UVLO), output under voltage protection (output UVP), output over voltage protection (output OVP), output over current protection (output OCP), and thermal shutdown (TSD). Moreover, this IC has the power good (PG) function that indicates the state of the output voltage (VOUT pin). When the output voltage reaches the PG voltage, the PG signal is outputted.

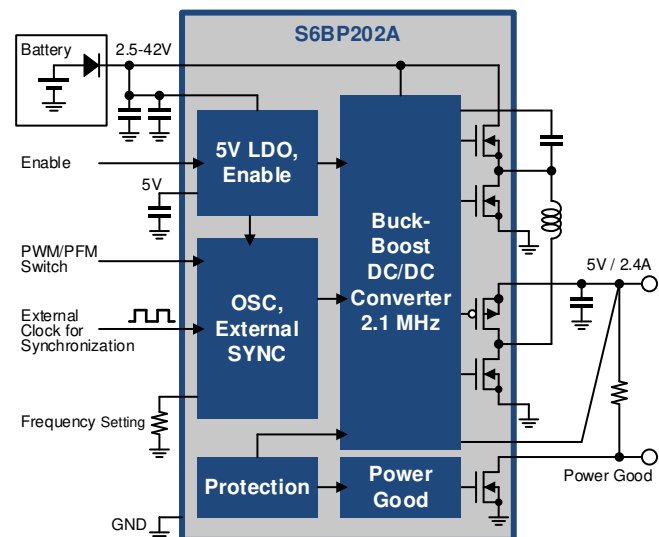
Features

- Wide input voltage range: 2.5V to 42V
- Preset output voltage: 5.000V
- Wide operating frequency range: 200 kHz to 2.1 MHz
- External synchronized clock range: 200 kHz to 400 kHz
- SYNC function
 - SYNC_IN: External clock input
(Unless inputting clock, this IC operates by internal clock)
- Super-high efficiency by PFM operation
(When setting MODE pin to a low level)
- Automatic PWM/PFM switching operation and fixed PWM operation are selectable by MODE pin
- Built-in switching FET
- Synchronous current mode architecture
- Shutdown current: Lower than 1 μ A
- Quiescent current: 20 μ A
- Power Good Monitor
 - Output voltage monitoring by window comparator
 - Power-on reset time: 14 ms
- Soft start time without load dependence: 0.9 ms
(When switching frequency = 2.1 MHz)
- Enhanced protection functions
 - Input UVLO
 - Output UVP: 92.0%
 - Output OVP: 108.0%
 - Output OVC
 - Thermal shutdown
- Small ETSSOP16 package (exposed PAD): 5 mm \times 6.4 mm
- AEC-Q100 compliant (Grade-1)

Applications

- Instrument cluster
- Advanced driver assistance systems (ADAS)
- Gateway module
- Automotive applications
- Industrial applications

Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com/pmic to help you to select the right PMIC device for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for S6BP202A.

- Overview: [Automotive PMIC Portfolio](#), [Automotive PMIC Roadmap](#)
- Product Selector:
 - [S6BP202A](#):
1-Ch Buck-Boost Automotive PMIC
- Application Notes: Cypress offers S6BP202A application notes. Recommended application notes for getting started with S6BP202A are:
 - [AN99497](#): Designing a Power Management System with S6BP201A, S6BP202A, and S6BP203A
 - [AN201006](#): Thermal Considerations and Parameters
- Evaluation Kit Operation Manual:
 - [S6SBP202A1FVA1001](#):
Power block of automotive instrument cluster
- Related Products:
 - [S6BP201A](#), [S6BP203A](#):
1-Ch Buck-Boost Automotive PMIC
 - [S6BP401A](#):
6-Ch Automotive PMIC for ADAS
 - [S6BP501A](#), [S6BP502A](#):
3-Ch Automotive PMIC for Instrument Cluster

Contents

Features.....	1
Applications	1
Block Diagram.....	1
More Information	2
1. Product Lineup.....	4
2. Pin Assignment	4
3. Pin Descriptions.....	4
4. Architecture Block Diagram	6
5. Absolute Maximum Ratings	7
6. Recommended Operating Conditions	7
7. Electrical Characteristics	8
8. Functional Description	9
8.1 Block Description.....	9
8.2 Protection Function Table.....	10
9. Application Circuit Example and Parts list	11
10. Application Note.....	12
10.1 Setting the Operation Conditions.....	12
11. Reference Data	14
12. Usage Precaution.....	16
13. RoHS Compliance Information	16
14. Ordering Information	16
15. Package Dimensions	17
16. Major Changes	18
Document History.....	18
Sales, Solutions, and Legal Information.....	19

1. Product Lineup

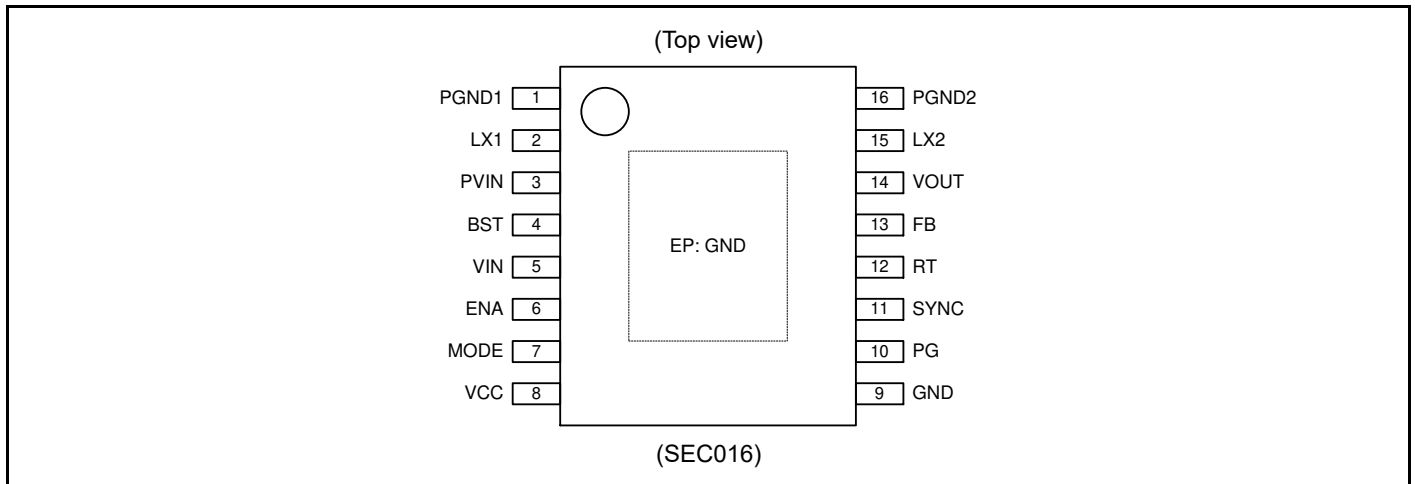
The VOUT output voltage, SYNC function, VOUT UVP threshold, VOUT OVP threshold, power-on reset time of this product are set at the factory shipment.

Part Number (MPN)	Order Code	VOUT Output Voltage [V]	SYNC Function	VOUT UVP Threshold [%]		VOUT OVP Threshold [%]		Power-on Reset Time[s]
				Falling (Typ)	Rising(Typ)	Rising (Typ)	Falling (Typ)	
S6BP202A1FST2B00A	1F	5.000	SYNC_IN	92.0	93.0	108.0	107.0	14.0m

MPN: Marketing Part Number

2. Pin Assignment

Figure 2-1 Pin Assignment

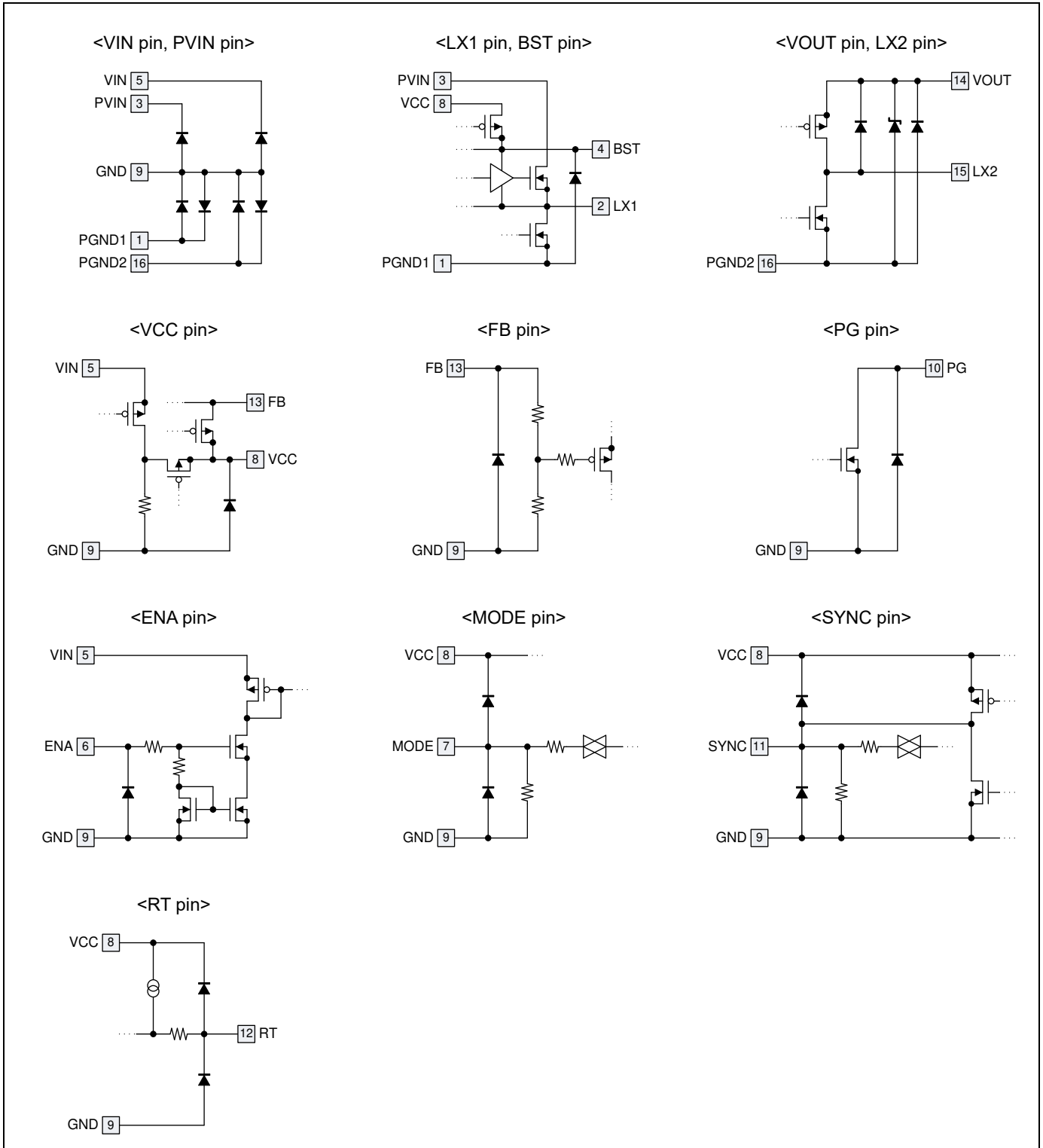


3. Pin Descriptions

Table 3-1 Pin Descriptions

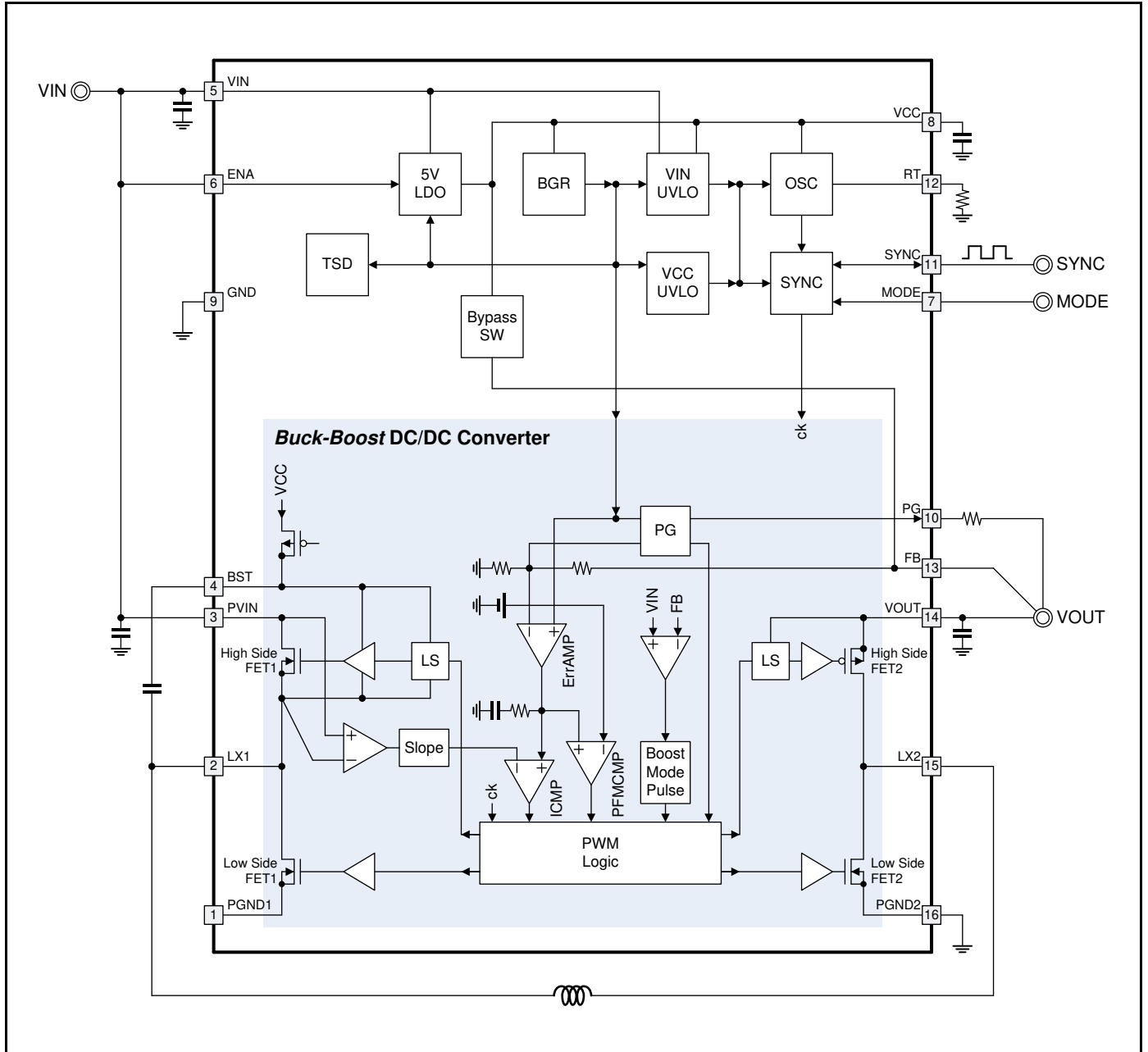
Pin No.	Pin Name	I/O	Description
1	PGND1	-	GND pin for built-in switching FET
2	LX1	O	Inductor connection pin
3	PVIN	I	Power supply pin for PWM controller and switching FETs
4	BST	I	BST(Boost) capacitor connection pin
5	VIN	I	Power supply pin
6	ENA	I	DC/DC converter enable pin
7	MODE	I	PWM/PFM operation control pin
8	VCC	O	VCC capacitor connection pin. LDO output pin of Internal reference voltage
9	GND	-	GND pin
10	PG	O	Open drain output pin for power good. When being used, connect PG pin to VCC pin or VOUT pin. When not being used, leave PG pin open.
11	SYNC	I	External clock input pin For the SYNC pin setting, refer to "10.1 Setting the Operation Conditions"
12	RT	O	Timing resistor connection pin for internal clock (switching frequency) For the resistance, refer to "10.1 Setting the Operation Conditions"
13	FB	I	Output voltage feedback pin
14	VOUT	O	DC/DC converter output pin
15	LX2	O	Inductor connection output pin.
16	PGND2	-	GND pin for built-in switching FET
EP	GND	-	GND pin

Figure 3-1 I/O Pin Equivalent Circuit Diagram



4. Architecture Block Diagram

Figure 4-1 Architecture Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V _{VIN}	VIN pin	-0.3	+48.0	V
	V _{PVIN}	PVIN pin	-0.3	+48.0	V
	V _{VCC}	VCC pin	-0.3	+6.9	V
Terminal voltage(*1)	V _{BST}	BST pin	-0.3	+48.0	V
	V _{LX1}	LX1 pin	-2.0	+48.0	V
	V _{LX2}	LX2 pin	-2.0	+6.9	V
	V _{FB}	FB pin	-0.3	V _{VCC}	V
	V _{RT}	RT pin	-0.3	V _{VCC}	V
	V _{MODE}	MODE pin	-0.3	V _{VCC}	V
	V _{SYNC}	SYNC pin	-0.3	V _{VCC}	V
	V _{ENA}	ENA pin	-0.3	+48.0	V
Difference voltage(*1)	V _{BST-LX}	Between BST-LX1 pins	-0.3	+6.9	V
	V _{GND}	Between GND-PGND1 pins, Between GND-PGND2 pins	-0.3	+0.3	V
PG output current	I _{PG}	PG pin	-3	0	mA
Power dissipation (*1)	P _D	T _a ≤ ±25°C	0	3324 (*2)	mW
Storage temperature	T _{STG}	-	-55	+150	°C

*1: When PGND1 = PGND2 = GND = 0V

*2: When the product is mounted on 76.2 mm × 114.3 mm, four-layer FR-4 board

Warning:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

6. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Power supply voltage (*1)	V _{VIN}	VIN pin	At start-up	5.0	12.0	42.0	V
			After start-up	2.5	12.0	42.0	V
Terminal voltage (*1)	V _{BST}	BST pin	0.0	-	47.5	V	
	V _{LX1}	LX1 pin	-1.0	+12.0	+42.0	V	
	V _{LX2}	LX2 pin	-1.0	-	+5.5	V	
	V _{FB}	FB pin	0.0	-	5.5	V	
	V _{MODE}	MODE pin	0.0	-	5.5	V	
	V _{SYNC}	SYNC pin	0.0	-	5.5	V	
	V _{ENA}	ENA pin	0.0	12.0	42.0	V	
Difference voltage(*1)	V _{BST-LX1}	Between BST-LX1 pins	0.0	-	5.5	V	
	V _{GND}	Between GND-PGND1 pins, Between GND-PGND2 pins	-0.05	0.00	+0.05	V	
PG output current	I _{PG}	PG pin (sink current)	0	-	1	mA	
BST capacitance	C _{BST}	Between BST-LX1 pins	0.068	0.100	0.470	μF	
VCC capacitance	C _{VCC}	Between VCC-GND pins	2.2	4.7	10.0	μF	
Timing resistance	R _{RT}	Between RT-GND pins. When using internal clock	22	-	270	kΩ	
Operating ambient Temperature	T _a	-	-40	+25	+125	°C	

*1: When PGND1 = PGND2 = GND = 0V

Warning:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

7. Electrical Characteristics

VIN=PVIN=12V, ENA=5V

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Buck-boost DC/DC converter Block	VOUT output voltage	V _{VOUT}	I _{VOUT} = 0A, When V _{VOUT} = 5.000	4.925	5.000	5.075	V
	FB input resistance	R _{FB}	EN = 0V, Ta = +25°C	3.84	4.80	5.76	MΩ
	Switching FET on-resistance	R _{H_{SIDE}FET1}	LX1 = -30 mA (Between PVIN-LX1)	-	150	-	mΩ
		R _{L_{SIDE}FET1}	LX1 = 30 mA (Between LX1-PGND1)	-	150	-	mΩ
		R _{H_{SIDE}FET2}	LX2 = -30 mA (Between VOUT-LX2)	-	150	-	mΩ
		R _{L_{SIDE}FET2}	LX2 = 30 mA (Between LX2-PGND2)	-	150	-	mΩ
	switching FET leakage current	I _{LEAK}	-	-	-	5	μA
	Soft-start time	T _{SS}	R _{RT} = 22 kΩ	0.855	0.9	0.945	ms
Maximum output current	I _{VOUT}	PVIN ≥ 7.5V, Ta = 25 °C	2.4 (*1)	-	-	A	
		PVIN = 4.5V, Ta = 25 °C	1.0 (*1)	-	-	A	
Current limit	I _{LIMIT}	PVIN = 12V, L = 2.2 μH	2.4 (*1)	-	-	A	
5V LDO block	VCC output voltage	V _{VCC}	VIN = 12V	4.9	5.0	5.1	V
VIN UVLO block	VIN UVLO falling threshold	V _{UVLOVINHL}	VIN input voltage when falling	2.30	2.40	2.50	V
	VIN UVLO rising threshold	V _{UVLOVINLH}	VIN input voltage when rising	4.55	4.75	4.95	V
VCC UVLO block	VCC UVLO falling threshold	V _{UVLOVCCHL}	VCC input voltage when falling	2.30	2.40	2.50	V
	VCC UVLO rising threshold	V _{UVLOVCCLH}	VCC input voltage when rising	4.55	4.75	4.95	V
ENA pin	Enable condition	V _{ENA}	Enable voltage range	1.10	-	V _{VIN}	V
		V _{DSB}	Disable voltage range	0.0	-	0.2	V
	ENA input current	I _{ENA}	V _{ENA} = 12V	-	1	3	μA
MODE pin	MODE input voltage	V _{MODE_L}	Automatic PWM/PFM switching	0.0	-	0.4	V
		V _{MODE_H}	Fixed PWM operation	2.0	-	V _{VOUT}	V
	MODE Input current	I _{MODE}	MODE = 5.0V	-	5	10	μA
OSC block	Switching frequency (SYNC output frequency)	F _{OSC}	R _{RT} = 22kΩ	2.0	2.1	2.2	MHz
		F _{OSC}	R _{RT} = 270kΩ	180	200	220	kHz
SYNC block (SYNC_IN)	SYNC input threshold	V _{SYNC_L}	When selecting SYNC_IN	0.0	-	0.4	V
		V _{SYNC_H}	When selecting SYNC_IN	2.0	-	V _{VOUT}	V
	SYNC input frequency	V _{SYNC_L}	When selecting SYNC_IN	200	-	400	kHz
	SYNC input duty ratio	V _{SYNC_H}	When selecting SYNC_IN	+20	+50	+80	%
	SYNC leakage current	I _{L_{KS}SYNC}	V _{SYNC} = 5.0V, When selecting SYNC_IN	-	5	10	μA
PG block (UVP, OVP)	VOUT UVP falling threshold	P _{G_{UV}PHL}	Falling threshold for VOUT output voltage setting	90.5	92.0	93.5	%
	VOUT UVP rising threshold	P _{G_{UV}PLH}	Rising threshold for VOUT output voltage setting	91.5	93.0	94.5	%
	VOUT OVP rising threshold	P _{G_{OV}PLH}	Rising threshold for VOUT output voltage setting	106.5	108.0	109.5	%
	VOUT OVP falling threshold	P _{G_{OV}PHL}	Falling threshold for VOUT output voltage setting	105.5	107.0	108.5	%
	Leak current	I _{L_KPG}	V _{PWRGD} = 5.0V, V _{ENA} = 0V	0	-	1	μA
	Low level output voltage	V _{OLPG}	I _{PGSINK} = 1 mA	0.025	0.05	0.15	V
	Delay time at abnormal detection	T _{PPG}	At power shutdown	-	7(*1)	12(*1)	μs
	Power-on reset time	T _{RPG}	At power good	9.1	14.0	18.9	ms
Thermal shutdown block (TSD)	Shutdown temperature	T _{TSDH}	-	-	165 (*1)	-	°C
		T _{TSDL}	Hysteresis	-	10 (*1)	-	°C
Supply current	Shutdown current	I _{V_{IN}SDN}	VIN input current, V _{ENA} = 0V	-	1	5	μA
	Quiescent current	I _{V_{IN}Q}	VIN input current, V _{ENA} = 12V, I _{VOUT} = 0A, MODE/SYNC/PG Pins = OPEN	-	20	40	μA

*1: The electrical characteristic is ensured by statistical characterization and indirect tests.

8. Functional Description

8.1 Block Description

Input Under Voltage Lockout (Input UVLO)

The input UVLO is the function that prevents a malfunction of this IC from the following status, and protects poststage devices.

- Transitional state at start-up
- Momentary drop of power supply voltage

To prevent such a malfunction, this protection monitors the VIN input voltage and VCC voltage. When either VIN or VCC voltage falls to the UVLO falling threshold, 2.4V (Typ), or lower, the IC stops the VOUT voltage output and becomes UVLO status. When both VIN and VCC voltages reach the UVLO rising threshold, 4.75V (Typ), or higher, the IC is released from the UVLO state and returns to the normal operation.

Output Under Voltage Protection (Output UVP)

The output UVP is the function that monitors the voltage drop of the VOUT pin and notifies by the PG pin.

When the output voltage falls to the UVP falling threshold (P_{GUVPHL}) for the output voltage setting or lower, the PG voltage is fixed to the low level. The IC becomes the UVP status, but the switching operation is maintained under the UVP status.

When the output voltage once again reaches the UVP rising threshold (P_{GUVPLH}) for the output voltage setting or higher, the IC is released from the UVP state and the PG voltage is fixed to the high level.

Output Over Voltage Protection (Output OVP)

The output OVP is the function that monitors the voltage rise of the VOUT pin and stops the switching operations, which protects poststage devices from overvoltage. Also, the VOUT state is notified by the PG pin.

When the output voltage rises to the OVP falling threshold (P_{GOVPLH}) for the output voltage setting or higher, the PG voltage is fixed to the low level. The IC becomes the OVP status, and the switching operations of the high-Side FETs are stopped. When the output voltage once again falls to the OVP falling threshold (P_{GOVPHL}) for the output voltage setting or lower, the IC is released from the OVP state and resumes the switching operations. The PG voltage is fixed to the high level again.

Output Over Current Protection (Output OCP)

The output OCP is the function that limits the excessive current load and protects poststage devices.

Thermal Shutdown (TSD)

The TSD is the function that protects the IC from heat-destruction. When the junction temperature reaches +165°C (Typ), the high-side and low-side switching FET are turned off and the IC becomes the TSD status. When the junction temperature once again falls to +155°C (Typ) or lower, the IC is released from the TSD state and restarts the power supply.

8.2 Protection Function Table

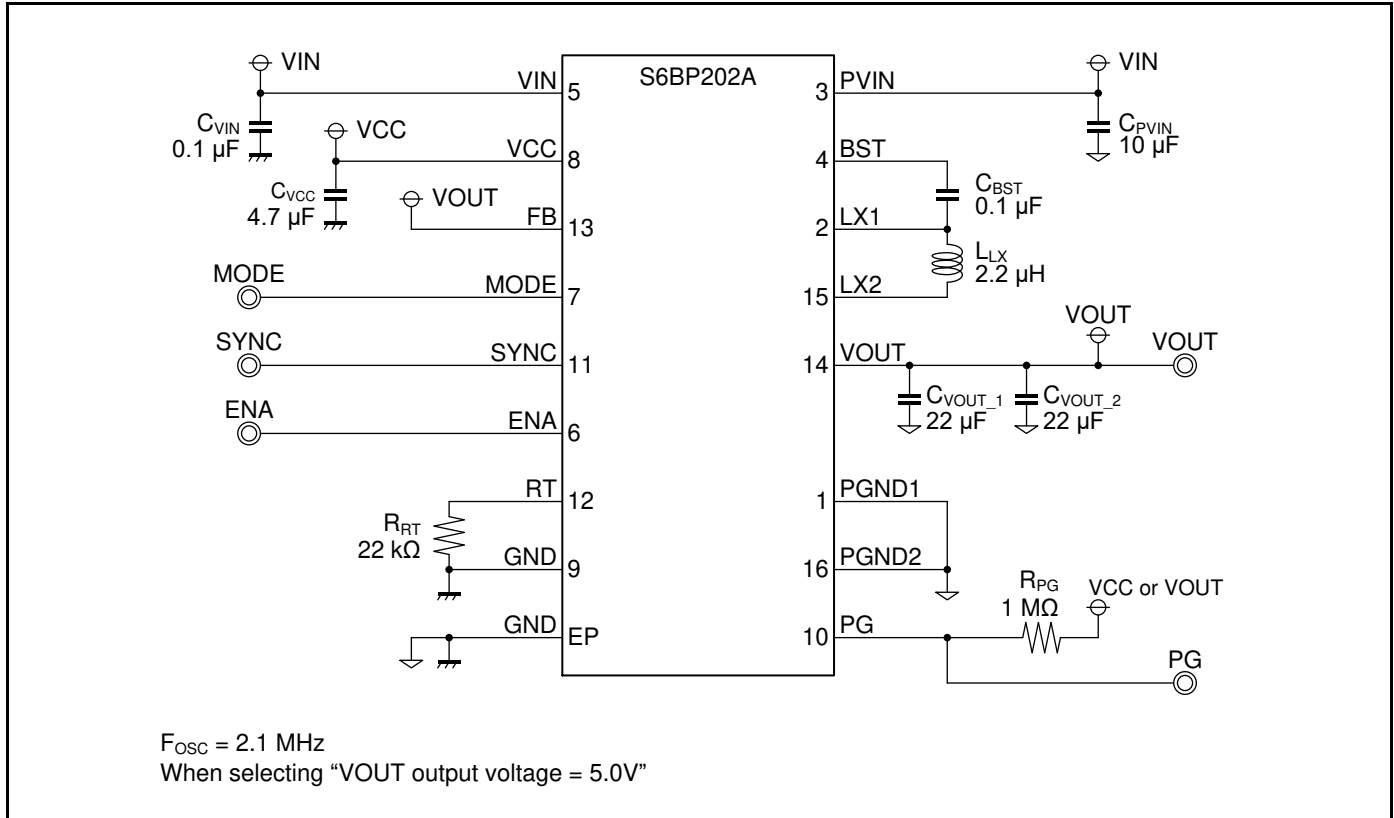
The following table shows the state of each pin when each protection function operates.

Table 8-1 Protection Function Table

Function	ENA Pin Setting	PG Pin Output	DC/DC Converter Operation	Remarks
Shutdown operation	L	Hi-Z (*1)	Shutdown	It is recommended to connect PG pin to VCC pin or VOUT pin via a pull-up resistor. When setting ENA pin to a low level, Both VCC pin and VOUT pin voltages drop to 0V. Therefore, PG pin outputs 0V.
Nominal operation	H	Hi-Z (*1)	Switching	-
Input under voltage protection (Input UVLO)	H	L	Shutdown	After releasing UVLO state, this IC is automatically reset with soft start.
Output under voltage protection (Output UVP)	H	L	Switching	-
Output over voltage protection (Output OVP)	H	L	Shutdown	-
Output over current protection (Output OCP)	H	L	Switching	OCP operates to drop the output voltage.
Thermal shutdown (TSD)	H	L	Shutdown	After releasing TSD state, this IC is automatically reset with soft start.

*1: PG pin is formed as an open drain structure. The internal MOSFET is in the OFF state.

9. Application Circuit Example and Parts list

Figure 9-1 Application Circuit Example

Table 9-1 Parts List

Symbol	Item	Value	Part Number	Vendor	Package Size (W×L×H[mm])	Remarks
C_{VIN} , C_{BST}	Ceramic capacitor	0.1 μF	CGA2B3X7R1H104K050BB	TDK	1.0×0.5×0.5	X7R, Rated voltage: 50 Vdc
C_{PVIN}	Ceramic capacitor	10 μF	CGA9N3X7R1H106K230KB	TDK	5.7×5.0×2.3	X7R, Rated voltage: 50 Vdc
C_{VCC}	Ceramic capacitor	4.7 μF	CGA4J3X7R1C475K125AB	TDK	2.0×1.25×1.25	X7R, Rated voltage: 16 Vdc
C_{VOUT_1} , C_{VOUT_2}	Ceramic capacitor	22 μF	CGA6P1X7R1C226M250AC	TDK	3.2×2.5×2.5	X7R, Rated voltage: 16 Vdc
L_{LX}	Inductor	2.2 μH	CLF7045T-2R2N-D	TDK	7.2×6.9×4.5	DCR: 14.6 m Ω , I_{DC_MAX} : 5.5A
R_{RT}	Resistor	22 k Ω	RK73H1JTDD2202F	KOA	0.8×1.6×0.45	–
R_{PG}	Resistor	1 M Ω	RK73H1JTDD1004F	KOA	0.8×1.6×0.45	–

TDK: TDK Corporation

KOA: KOA Corporation

10. Application Note

10.1 Setting the Operation Conditions

Operation State of DC/DC Convertor When Selecting SYNC_IN

The operation stage of DC/CD converter is set by both MODE pin and SYNC pin.

Table 10-1 Operation State of DC/DC Convertor When Selecting SYNC_IN

MODE Pin	SYNC Pin (Signal Input)	Operation State of DC/DC Convertor
L (*3)	L (*3)	Automatic PWM/PFM switching operation from an internal clock
	External clock input (*5)	Fixed PWM operation with synchronizing signal from an external clock (*2)
	H (*4)	Prohibition of use (*1)
H (*4)	L (*3)	Fixed PWM operation from an internal clock
	External clock input (*5)	Fixed PWM operation with synchronizing signal from an external clock (*2)
	H (*4)	Prohibition of use (*1)

*1: When selecting SYNC_IN and setting SYNC pin to a high level, the quiescent current (I_{VINQ}) is increased.

*2: Set the timing resistance (R_{RT}) to 330 k Ω .

*3: Apply the GND1 or GND2 voltage.

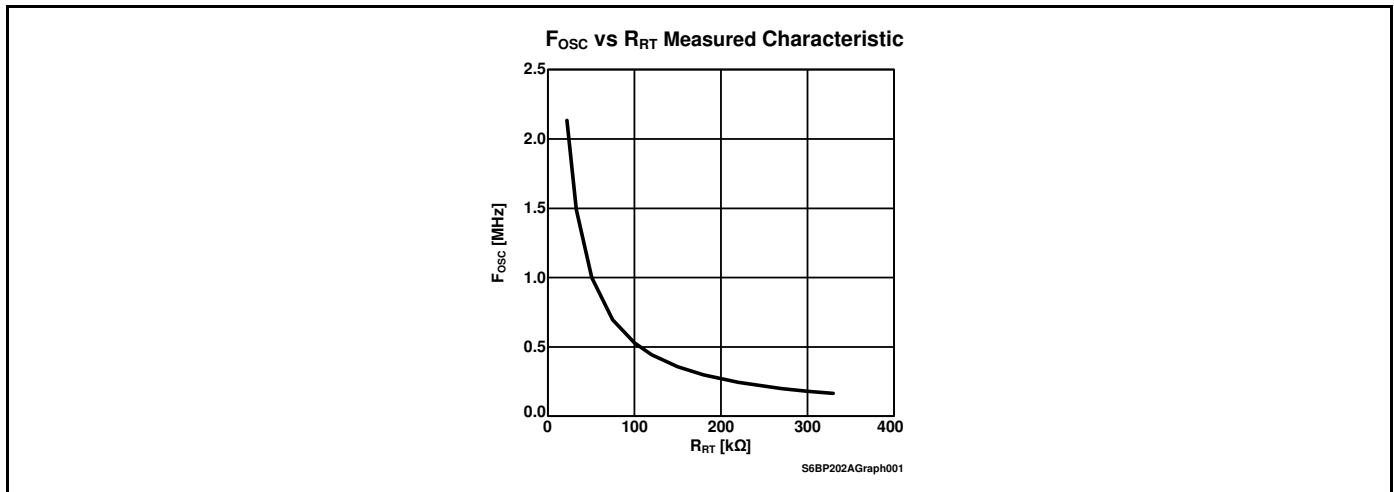
*4: Apply the VOUT voltage.

*5: Apply the VOUT voltage at a high level. Apply the GND1 or GND2 voltage at a low level

Setting of Switching Frequency (Internal Clock)

The switching frequency (internal clock) can be set by RT resistor, which value is the timing resistance (R_{RT}), connected to RT pin. Set the timing resistance in a range within the following graph

Figure 10-1 F_{OSC} vs R_{RT} Measured Characteristic



The reference value can be calculated by the following formula.

$$F_{OSC}[\text{Hz}] \approx \frac{1}{R_{RT} \times 21.7 \times 10^{-12}}$$

F_{OSC} : Switching frequency [Hz]
 R_{RT} : Timing resistance [Ω]

Setting of Soft-start Time

The Soft-start time is determined by the timing resistance (R_{RT}), the value of the resistor connected to RT pin.

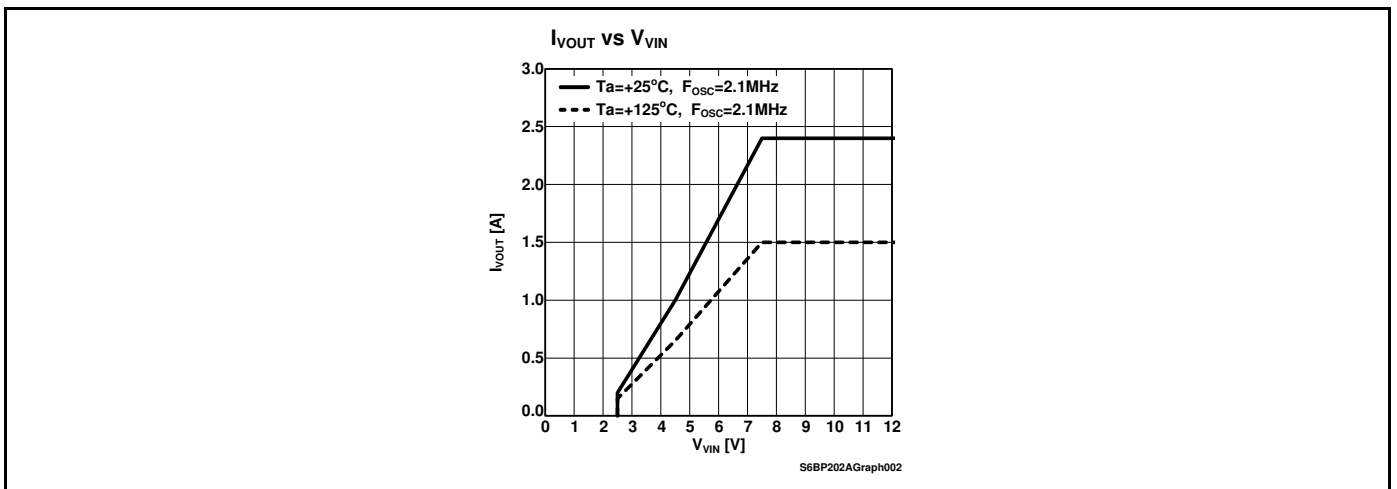
$$T_{SS}[\text{s}] = \frac{1}{F_{OSC}} \times 2 \times 1024$$

T_{SS} : Soft-start time [s]
 F_{OSC} : Switching frequency [Hz]

Consideration of VOUT Maximum Output Current

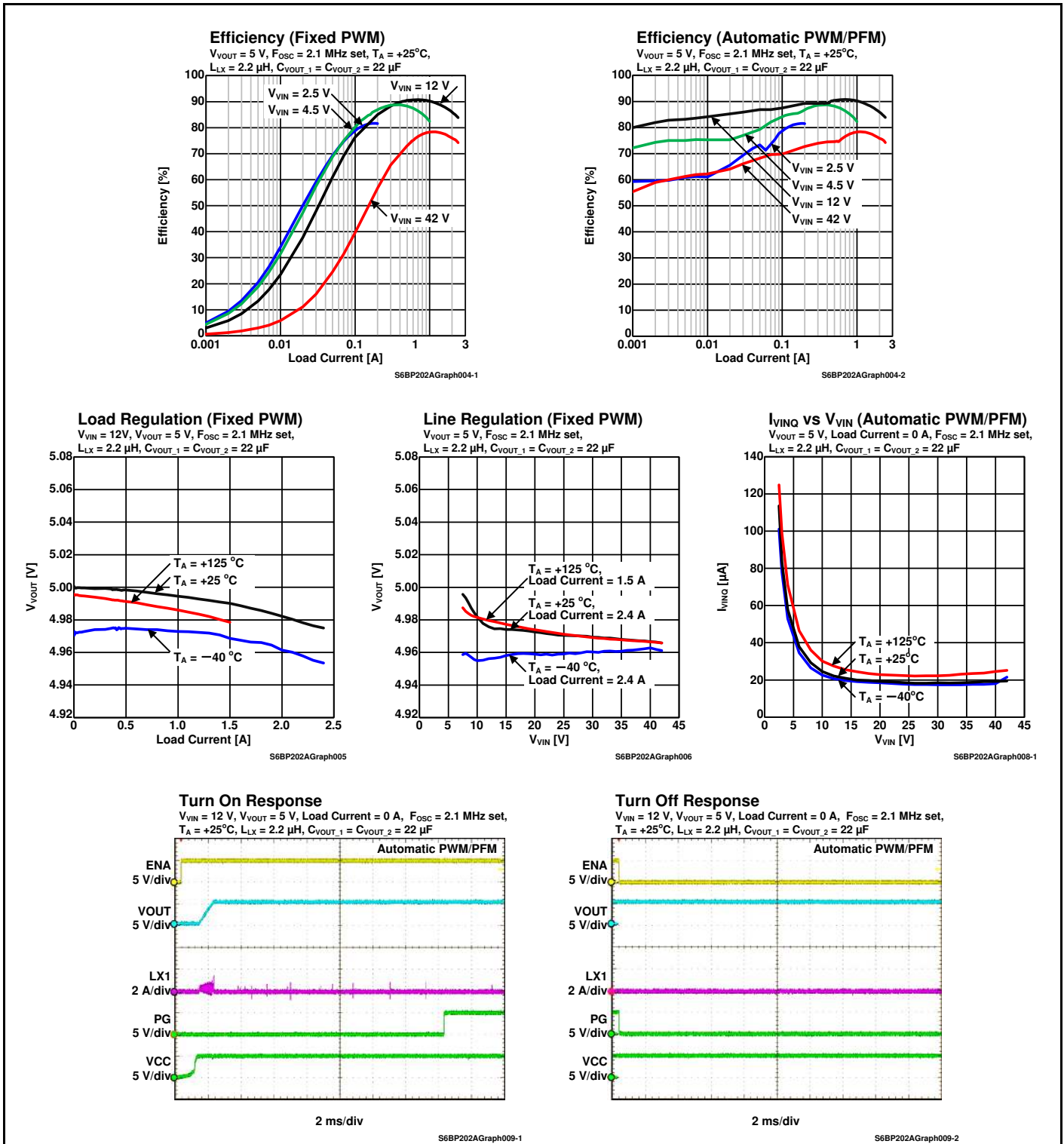
Make sure the VOUT maximum output current in a range within the following graph.

Figure 10-2 I_{VOUT} vs V_{VIN}



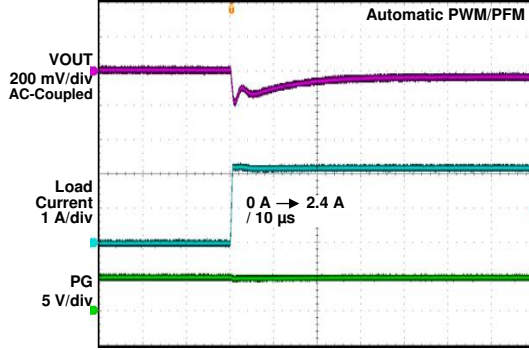
11. Reference Data

The followings are the reference data measured under the conditions shown in "9. Application Circuit Example and Parts list".



Load Transient Response

$V_{VIN} = 12\text{ V}$, $V_{VOUT} = 5\text{ V}$, $F_{OSC} = 2.1\text{ MHz}$ set, $T_A = +25^\circ\text{C}$,
 $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$

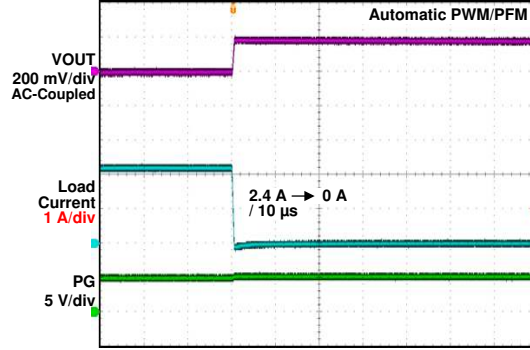


200 $\mu\text{s}/\text{div}$

S6BP202AGraph010-1

Load Transient Response

$V_{VIN} = 12\text{ V}$, $V_{VOUT} = 5\text{ V}$, $F_{OSC} = 2.1\text{ MHz}$ set, $T_A = +25^\circ\text{C}$,
 $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$

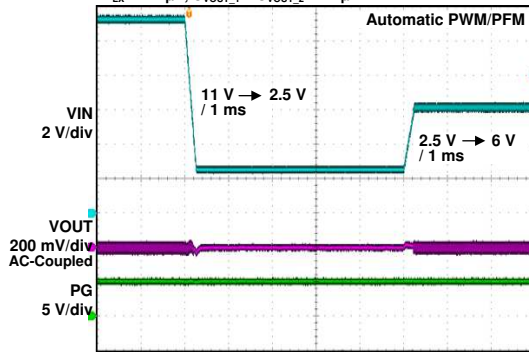


200 $\mu\text{s}/\text{div}$

S6BP202AGraph010-2

Cold Crank Line Transient Response

$V_{VOUT} = 5\text{ V}$, Load Current = 0.2 A, $F_{OSC} = 2.1\text{ MHz}$ set, $T_A = +25^\circ\text{C}$,
 $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$

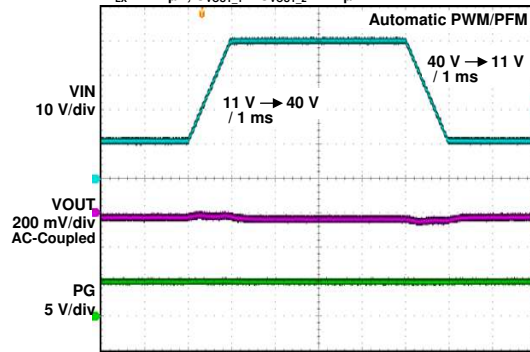


4 ms/div

S6BP202AGraph011-1

Load Dump Line Transient Response

$V_{VOUT} = 5\text{ V}$, Load Current = 2.4 A, $F_{OSC} = 2.1\text{ MHz}$ set, $T_A = +25^\circ\text{C}$,
 $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$

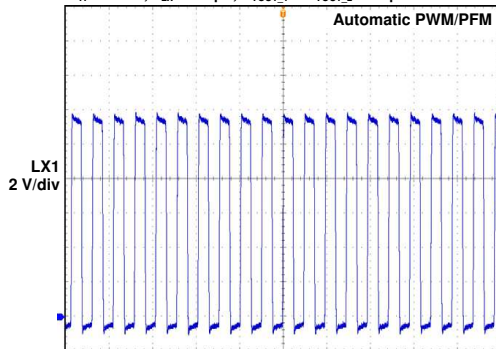


1 ms/div

S6BP202AGraph011-2

Switching Waveform

$V_{VIN} = 12\text{ V}$, $V_{VOUT} = 5\text{ V}$, Load Current = 2.4 A, $F_{OSC} = 2.1\text{ MHz}$ set,
 $T_A = +25^\circ\text{C}$, $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$

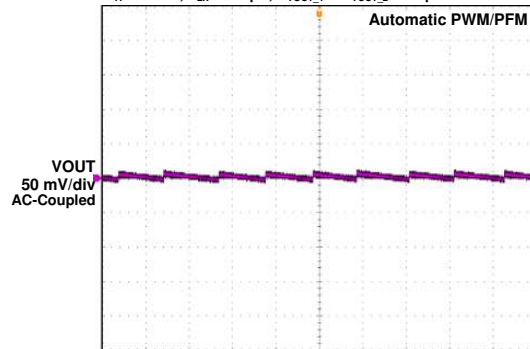


1 $\mu\text{s}/\text{div}$

S6BP202AGraph012-1

Ripple Waveform

$V_{VIN} = 12\text{ V}$, $V_{VOUT} = 5\text{ V}$, Load Current = 0 A, $F_{OSC} = 2.1\text{ MHz}$ set,
 $T_A = +25^\circ\text{C}$, $L_{LX} = 2.2\text{ }\mu\text{H}$, $C_{VOUT_1} = C_{VOUT_2} = 22\text{ }\mu\text{F}$



10 ms/div

S6BP202AGraph012-2

12. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below -0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

13. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

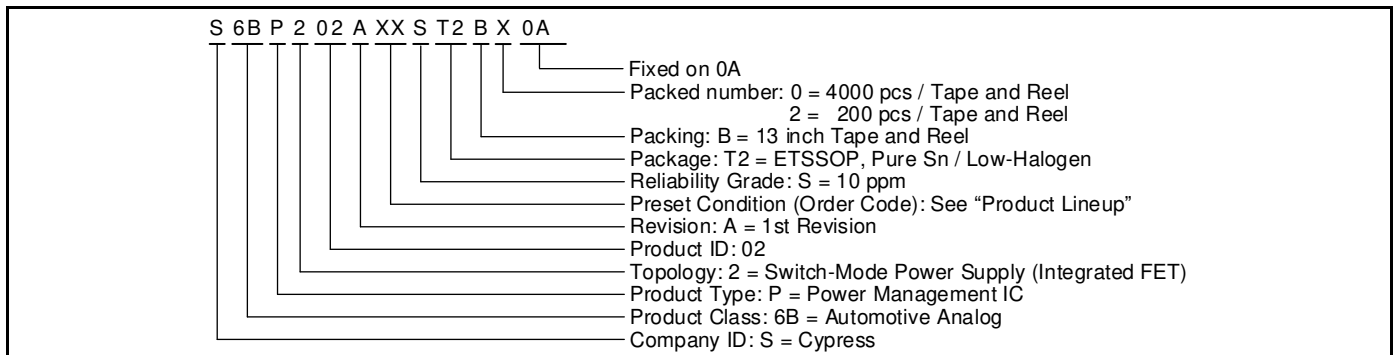
14. Ordering Information

Table 14-1 Ordering Information

Order Code	Part Number (MPN)	Package
1F	S6BP202A1FST2B00A, S6BP202A1FST2B20A	Plastic ETSSOP16 (0.65 mm pitch), 16-pin (Package Code: SEC016)

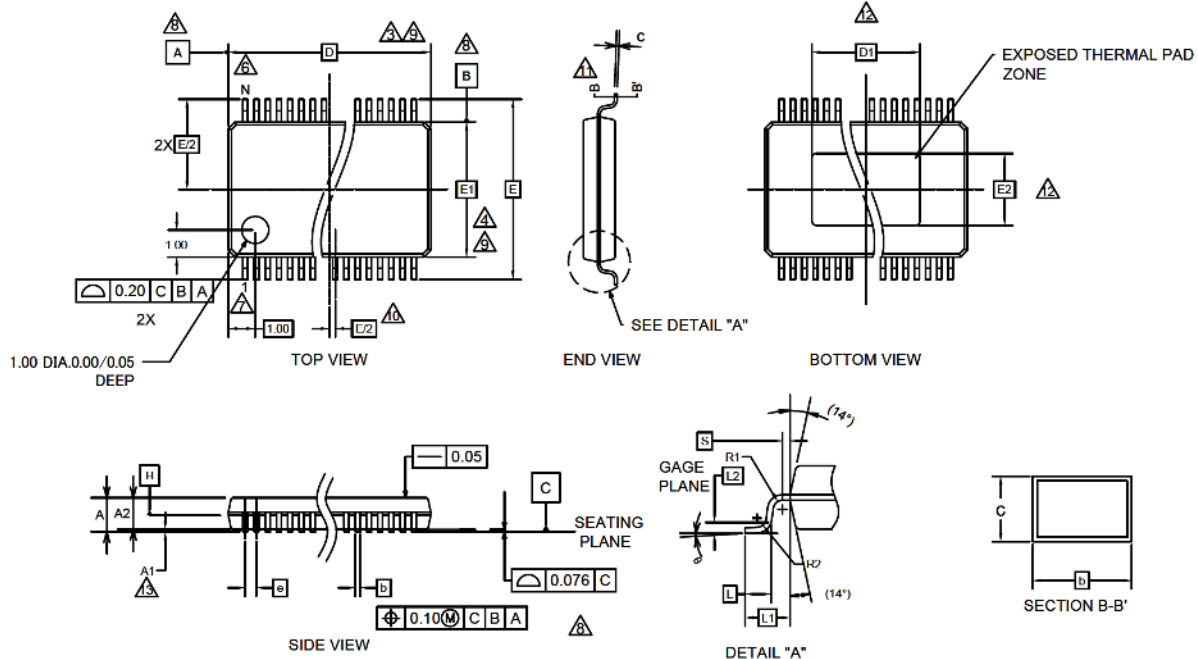
MPN: Marketing Part Number

Figure 14-1 Ordering Part Number Definitions



15. Package Dimensions

Package Code: SEC016



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.10
A1	0.05	-	0.15
A2	0.85	0.90	0.95
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
D1	2.90	3.00	3.10
E2	2.90	3.00	3.10
S	0.20	-	-
R1	0.09	-	-
R2	0.09	-	-
θ	0°	-	8°
c	0.09	-	0.20
b	0.19	-	0.30
L	0.50	0.60	0.70
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		
N	16		

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSIONS SHALL BE 0.07mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHOULD BE 0.08mm FOR 0.65mm PITCH, 0.08mm FOR 0.50mm PITCH AND 0.07mm FOR 0.40mm PITCH PACKAGES.
6. 'N' IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH
7. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
8. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
9. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.
10. THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE, DATUM A.
11. CROSS SECTION B-B' TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.
12. DIMENSIONS "D1" AND "E2" ARE THERMALLY ENHANCED VARIATIONS. END USER SHOULD VERIFY AVAILABLE SIZE OF EXPOSED PER FOR SPECIFIC DEVICE APPLICATION "D1" AND "E2" DIMENSIONS DO NOT INCLUDE MOLD FLASH.
13. A1 IS DEFINED AS THE VERTICAL CLEARANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

 PACKAGE OUTLINE, 16 LEAD ETSSOP
 SEC016

002-10769 Rev. **

16. Major Changes

Spancion Publication Number: S6BP202A_DS405-00027

Page	Section	Change Results
Preliminary 0.1		
-	-	Initial release
Preliminary 0.2		
1	Cover page	The sentences of the "Notice to Readers" were changed from "the contents of Full Production" to "the contents of Preliminary".
13	10. Electrical Characteristics	"(TSD)" was added in the table of "10. Electrical Characteristics".

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: S6BP202A, ASSP, 42V, 2.4A, Synchronous Buck-boost DC/DC Converter IC

Document Number: 002-08496

Revision	ECN	Submission Date	Description of Change
**	-	09/04/2015	New Spec.
*A	5056149	12/18/2015	Added Block Diagram Added Figure 15-1 Updated 16. Package Dimensions
*B	5164343	03/08/2016	Added "AEC-Q100 compliant (Grade-1)" in Features Added Figure 3-1 I/O Pin Equivalent Circuit Diagram The followings in 7. Electrical Characteristics were updated. The parameter name of I _{VOUT} was changed from "V _{OUT} output voltage" to "Maximum output current" The max values of I _{VOUT} were moved to the min column. Added 11. Development Support Added 12. Reference Data Deleted the ES part number from Table 15-1
*C	5839054	07/31/2017	Adapted Cypress new logo.
*D	5909405	10/13/2017	Updated to the Cypress naming and format Updated "TSSOP" → "ETSSOP" in Features , Table 14-1 and Figure 14-1 Updated 15 Package Dimensions Added More Information Deleted "11. Development Support" (Moved to More Information) Changed the suffix of the Part Number from "000" to "00A" in 1. Product Lineup Table 14-1 and Figure 14-1
*E	6409930	12/13/2018	No change; sunset review.
*F	7022884	11/18/2020	Updated Features and Block Diagram for orderable S6BP202A1F Updated MPN in 1.Product Lineup , Table 14-1 Ordering Information and Figure 14-1 Ordering Part Number Definitions . Deleted "Operation State of DC/DC Converter When Selecting SYNC_OUT"

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmics
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

© Cypress Semiconductor Corporation, 2015-2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.