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# ADuC7060 Evaluation Board User Guide
# MicroConverter® ADuC7060 Development System

## FEATURES

**2-layer PCB (4 in. × 5 in. form factor)**
**9 V power supply regulated to 3.3 V and 2.5 V on board**
**4-pin UART header to connect to RS-232 interface cable**
**20-pin standard JTAG connector**
**Demonstration circuit**
**32.768 kHz watch crystal to drive the PLL clock**
**ADR280 1.2 V external reference chip**
**Reset/download/IRQ0 push buttons**
**Power indicator/general-purpose LEDs**
**Access to all ADC inputs and DAC output from external header; all device ports are brought out to external header pins**
**Surface-mount and through-hole general-purpose prototype area**

## EVALUATION KIT CONTENTS

**mIDAS-Link JTAG programming POD**
**CD containing evaluation software including user manuals, data sheets, example code, ARMWSD, and evaluation compilers**
**9 V power supply**
**RS-232 to UART cable**
**USB cable**

## GENERAL DESCRIPTION

This user guide refers to the ADuC7060 evaluation board. This evaluation board allows evaluation of the ADuC7060 and ADuC7061 parts. The ADuC7060 is the superset of the ADuC706x series, and all features of the ADuC7061 can be evaluated using the ADuC7060. The ADuC7060 contains an ARM7TDMI core, 32 kB of flash, 4 kB of SRAM, dual 24-bit sigma-delta (Σ-Δ) ADCs, and a 12-bit DAC as well as many other features.

This evaluation board allows a user to program the ADuC7060 via the JTAG or the UART interfaces. The user may also debug their source code through the JTAG interface.

In this user guide, all references to the physical orientation of components on the board are made with respect to a component-side view of the board with the prototype area appearing in the bottom of the board.

The board is laid out to minimize coupling between the analog and digital sections of the board. To this end, the ground plane is split with the analog section on the left side and a digital plane on the right side of the board. The regulated 2.5 V power supply is routed directly to the digital section and is filtered before being routed into the analog section of the board.

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## REVISION HISTORY

**8/09—Revision 0: Initial Version**

# EVALUATION BOARD HARDWARE

## POWER SUPPLY

Connect the 9 V power supply via the 2 mm input power socket (J1). The input connector is configured as a center negative, that is, with GND on the center pin and 9 V on the outer shield.

The 9 V supply is regulated via the linear voltage regulator, U3. The 2.5 V regulator output is used to drive the digital side of the board directly. The 2.5 V supply is also filtered and then used to supply the analog side of the board. This regulator supplies the ADuC7060 microcontroller.

The 9 V supply is also regulated via the linear voltage regulator, U2. The 3.3 V output of this regulator is used to supply the JTAG programming interface. This device does not supply the ADuC7060 device.

When on, the LED (D4) indicates that a valid 2.5 V supply is driven from the regulator circuit. All active components are decoupled with 0.1 μF capacitors at device supply pins to ground.

## RS-232 INTERFACE

The ADuC7060 (U1) P1.1 and P1.0 lines are connected to the RS-232 interface cable via Connector J4. The interface cable generates the required level shifting to allow direct connection to a PC serial port. Ensure that the cable supplied is connected to the board correctly, that is, DVDD is connected to DVDD and DGND is connected to DGND.

## EMULATION INTERFACE

Nonintrusive emulation and download are possible on the ADuC7060 via JTAG by connecting a JTAG emulator to the J5 connector.

## CRYSTAL CIRCUIT

The board is fitted with a 32.768 kHz crystal, from which the on-chip PLL circuit can generate a 10.24 MHz clock.

## EXTERNAL REFERENCE (ADR280)

The external 1.2 V reference chip, ADR1, has two functions.

- It is provided on the evaluation board to demonstrate the external reference option of the ADuC7060.
- It can also be used as an input source to AIN1, if required.

## RESET/DOWNLOAD/$\overline{\text{INT0}}$ PUSH BUTTONS

The $\overline{\text{INT0}}$ push button is referred to as the $\overline{\text{IRQ0}}$ push button in the ADuC7060/ADuC7061 data sheet. Note that this is the same push button and only differs in name.

A reset push button is provided to allow the user to reset the part manually. When pressed, the reset pin of the ADuC7060 is pulled to DGND. Because the $\overline{\text{RESET}}$ pin on the ADuC7060 is Schmidt-triggered internally, there is no need to use an external Schmidt trigger on this pin.

When pressed, the $\overline{\text{INT0}}$ push button switch drives P0.4/IRQ0 high. This can be used to initiate an External Interrupt 0.

To enter serial download mode, pull the NTRST/$\overline{\text{BM}}$ pin low while reset is toggled. On the evaluation board, serial download mode can be easily initiated by holding down the serial download push button (S3) while pressing and releasing the reset button (S1).

## POWER INDICATOR/GENERAL PURPOSE LEDS

A power LED (D4) is used to indicate that a sufficient supply is available on the board. A general-purpose LED (D6) is directly connected to P1.6 of the ADuC7060. When P1.6 is cleared, the LED is turned on. When P1.6 is set, the LED is turned off.

## ANALOG I/O CONNECTIONS

Note that the ADC0/ADC1 pins and the AIN0/AIN1 pins are the same pins in this user guide. Both sets use the function and differ only in name.

All analog I/O connections are brought out on Header J2.

The primary ADC inputs, AIN0 and AIN1, are connected to an RTD demonstration circuit (see Figure 1). The component, RTD1 is a surface-mount RTD in a 1206 package. It is stimulated by the excitation current source, IEC0 from the ADuC7060, and is measured differentially by the primary ADC. R1 is the 5.6 kΩ reference resistor in the circuit.

The DAC output is buffered externally using the OP293 op amp device, U4.

## GENERAL-PURPOSE PROTOTYPE AREA

General-purpose prototype areas are provided at the bottom of the evaluation board for adding external components as required in the user's application. As can be seen from the layout in Figure 4, $AV_{DD}$, AGND, $V_{DD}$, and DGND tracks are provided in this prototype area.

# DIP SWITCH LINK OPTIONS

**Table 1.**

| Option | Name | Function | Use |
|---|---|---|---|
| S4-1 | RTD AIN0 | Connects the positive side of the RTD to the AIN0 pin (Pin 20). | Slide S1-1 to the on position to connect the positive side of the RTD to the ADuC7060.<br>Slide S1-1 to the off position to disconnect the RTD from AIN0. |
| S4-2 | RTD AIN1 | Connects the negative side of the RTD to the AIN1 pin (Pin 19). | Slide S1-2 to the on position to connect the negative side of the RTD to the ADuC7060.<br>Slide S1-2 to the off position to disconnect the RTD from AIN1. |
| S4-3 | RTD REFIN+ | Connects the positive side of the reference resistor (R1) in the RTD demo circuit to the VREF+ pin (Pin 21). | Slide S1-3 to the on position to connect the positive side of the reference resistor (R1) to the VREF+ pin.<br>Slide S1-3 to the off position to disconnect the reference resistor from the VREF+ pin. |
| S4-4 | RTD REFIN− | Connects the negative side of the reference resistor (R1) in the RTD demo circuit to the VREF− pin (Pin 22). | Slide S1-4 to the on position to connect the negative side of the reference resistor (R1) to the VREF− pin.<br>Slide S1-4 to the off position to disconnect the reference resistor from the VREF− pin. In this position, the VREF− pin is connected to AGND. |
| S4-5 | 1.2V REFIN+ | Connects the ADR280 1.2 V precision reference voltage to the VREF+ pin (Pin 21). | Slide S1-5 to the on position to connect the ADR280 1.2 V precision reference voltage to the VREF+ pin.<br>Slide S1-5 to the off position to disconnect the ADR280 1.2 V reference device from VREF+. |
| S4-6 | AIN1 BIAS | Connects the ADR280 1.2 V precision reference voltage to the AIN1 pin (Pin 19). | Slide S1-6 to the on position to connect the ADR280 1.2 V precision reference voltage to the AIN1 pin.<br>Slide S1-6 to the off position to disconnect the ADR280 1.2 V reference device from AIN1. |
| S4-7 | EXT_REF | Brings the output of the ADR280 reference device to test Pin 13 of J2.<br>Note: Never turn S1-7 and S1-8 on at the same time as this shorts the external reference output to GND. | Slide S1-7 to the on position to connect the ADR280 reference device to Pin 13 of J2.<br>Slide S1-7 to the off position to disconnect the ADR280 reference device from Pin 13 of J2. |
| S4-8 | GND AINCOM | Connects AGND to Pin 13 of J2.<br>Note: Never turn S1-7 and S1-8 on at the same time as this shorts the external reference output to GND. | Slide S1-8 to the on position to connect Pin 13 of J2 to GND.<br>Slide S1-8 to the off position to disconnect Pin 13 of J2 from GND. |

# EXTERNAL CONNECTORS

## ANALOG I/O CONNECTOR J2

Connector J2 provides external connections for all ADC inputs, reference inputs, and DAC outputs. The pinout of the connector is shown in Table 2.

**Table 2. Pin Functions for Analog I/O Connector J2**

| Pin Number | Pin Function |
|---|---|
| J2-1 | AGND |
| J2-2 | AVDD |
| J2-3 | AIN0 |
| J2-4 | AIN1 |
| J2-5 | AIN2 |
| J2-6 | AIN3 |
| J2-7 | VREF− |
| J2-8 | VREF+ |
| J2-9 | AIN4 |
| J2-10 | AIN5 |
| J2-11 | AIN6 |
| J2-12 | AIN7 |
| J2-13 | EXT_REF |
| J2-14 | DAC (unbuffered) |
| J2-15 | DAC (buffered) |
| J2-16 | AIN8 |
| J2-17 | AIN9 |
| J2-18 | V0, op amp output |
| J2-19 | V−, op amp inverting input |
| J2-20 | V+, op amp noninverting input |
| J2-21 | GND_SW |
| J2-22 | IEXC1, Current Excitation Source 1 |

## POWER SUPPLY CONNECTOR J1

Connector J1 allows for connection between the evaluation board and the 9 V power supply provided in the ADuC7060 development system.

## EMULATION CONNECTOR J5

Connector J5 provides a connection of the evaluation board to the PC via a JTAG emulator.

## SERIAL INTERFACE CONNECTOR J4

Connector J4 provides a simple connection of the evaluation board to the PC via a serial port cable provided with the ADuC7060 development system.

## DIGITAL I/O CONNECTOR J3

The digital I/O connector, J3, provides external connections for all GPIOs. The pinout of the connector is shown in Table 3, with details of the pin functions.

**Table 3. Pin Functions for Digital I/O Connector J3**

| Pin No. | Pin Function |
|---|---|
| J3-1 | P1.6 |
| J3-2 | P1.5 |
| J3-3 | P1.4 |
| J3-4 | P1.3 |
| J3-5 | P1.2 |
| J3-6 | P0.6 |
| J3-7 | P0.5 |
| J3-8 | P2.1 |
| J3-9 | P2.0 |
| J3-10 | P1.1/SOUT |
| J3-11 | P1.0/SIN |
| J3-12 | P0.4/INT0 |
| J3-13 | P0.3 |
| J3-14 | P0.2 |
| J3-15 | P0.1 |
| J3-16 | P0.0 |
| J3-17 | $\overline{\text{RESET}}$ |
| J3-18 | DGND |
| J3-19 | DGND |
| J3-20 | DVDD |

# RTD DEMONSTRATION CIRCUIT

The on-board RTD is measured by the primary ADC by using the sample code in the RTD.c file. The RTD.c file is located in the code example folder of the software CD included with the evaluation board kit. The IEXC0 pin provides an excitation current through the RTD. The voltage drop across the RTD is measured differentially by ADC0 through input channels ADC0 and ADC1. The reference resistor, R1, is connected to the VREF+ of the ADuC7060.

For this test, set Switch 1 to Switch 4 of S4 to the on position.

Note that the ADC0/ADC1 pins and the AIN0/AIN1 pins are the same pins in this user guide. Both sets use the function and differ only in name.

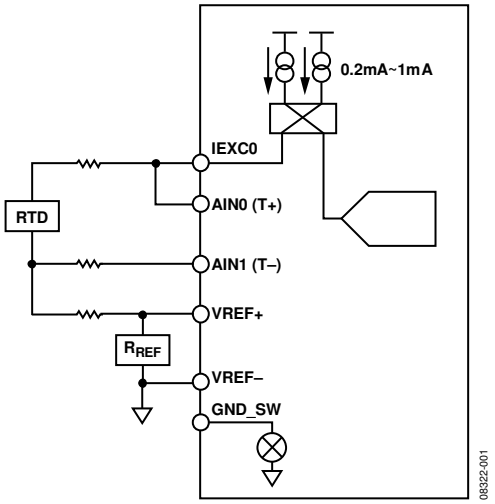


*Figure 1. Diagram of the RTD Circuit*

# EVALUATION BOARD SCHEMATIC AND ARTWORK

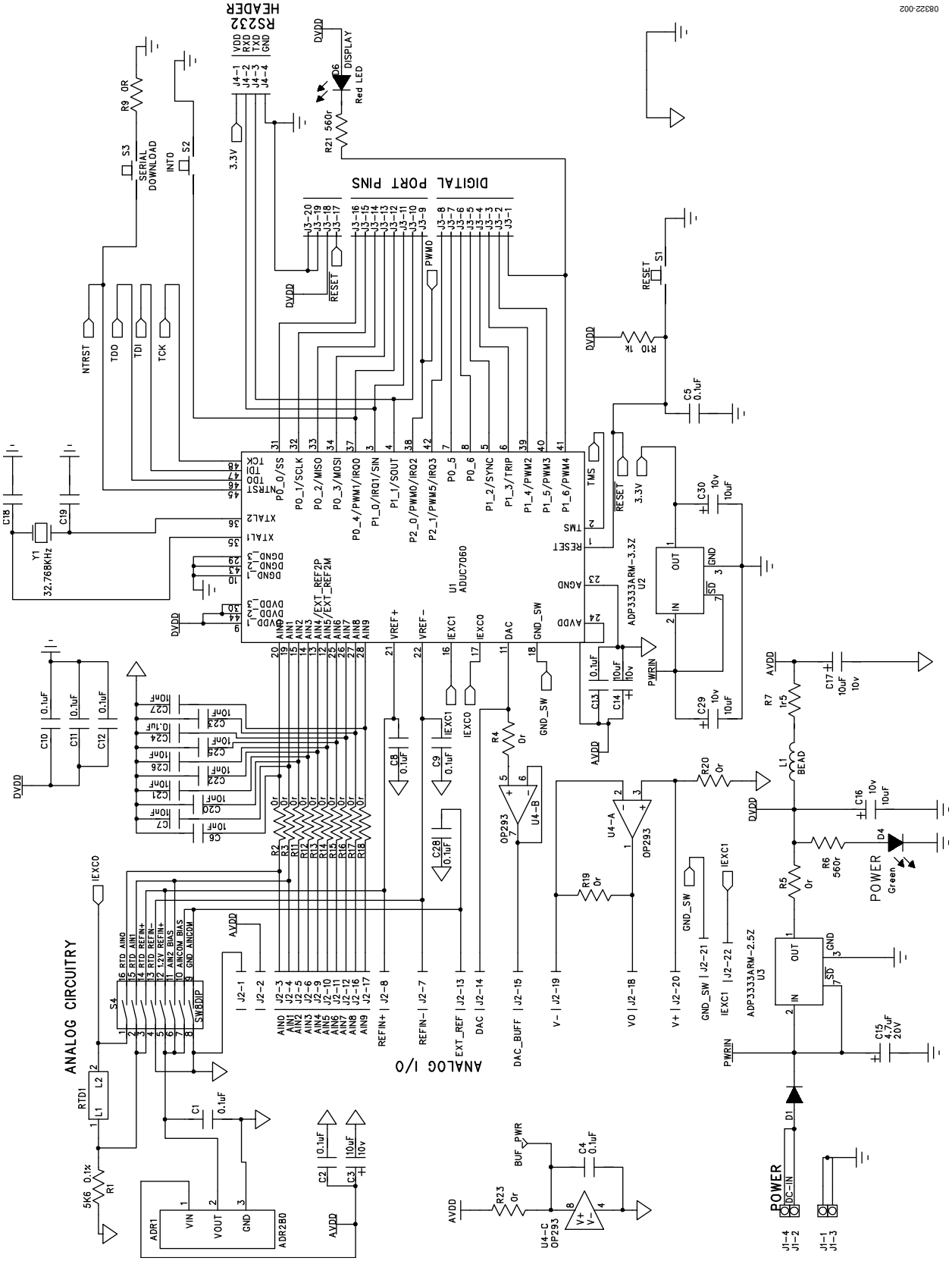


*Figure 2. EVAL-ADuC7060 Board Schematic and Layout*

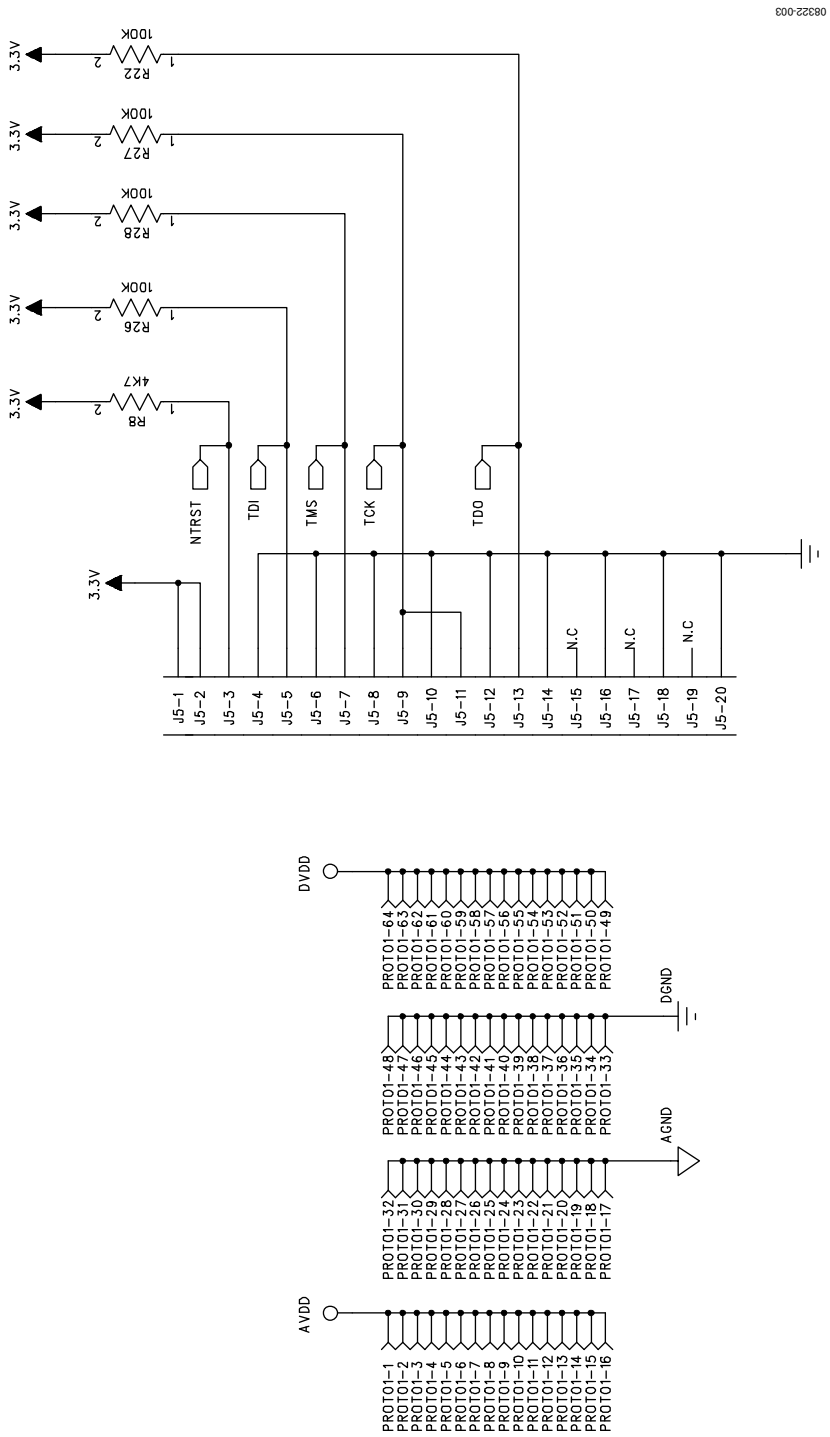


*Figure 3. Evaluation Board Schematic*

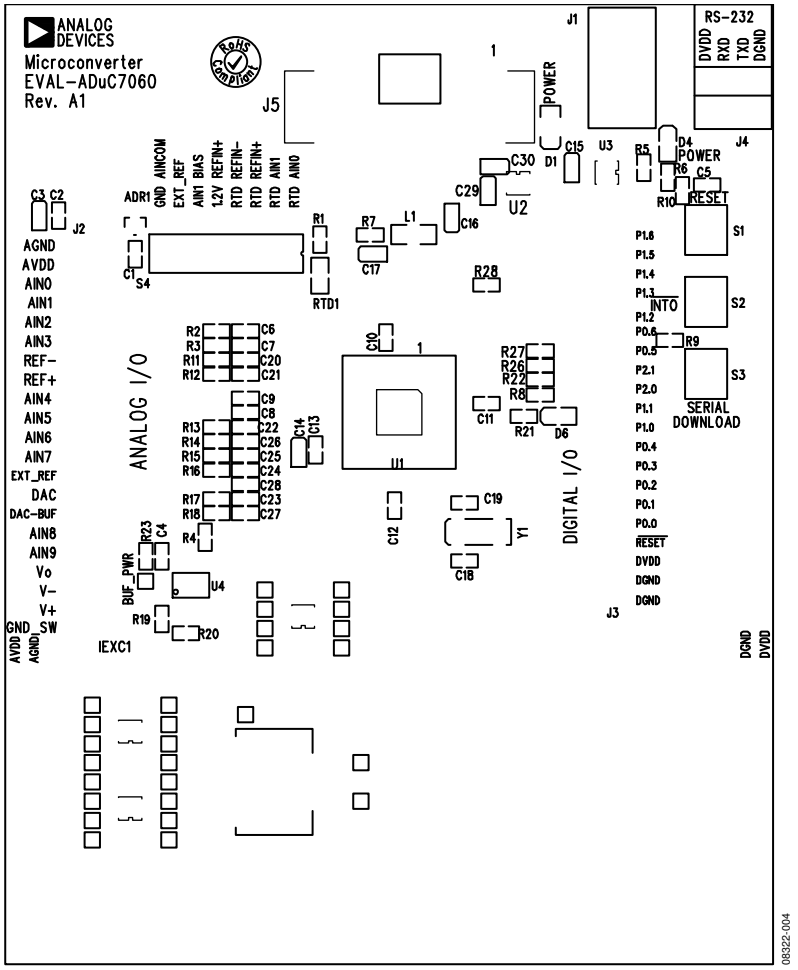


*Figure 4. Evaluation Board Silkscreen*

# BILL OF MATERIALS

**Table 4.**

| Qty | Component | Description | Order No. | Supplier |
|---|---|---|---|---|
| 1 | EVAL-ADuC7060QS QuickStart PCB | Two-sided surface-mount PCB-1 | | |
| 4 | PCB Stand-offs | Stand-off, stick on mounting feet | 1165061 | Farnell |
| 1 | U1 | MicroConverter | ADuC7060 | Analog Devices, Inc. |
| 1 | ADR1 | Band gap reference | ADR280ARTZ-REEL7 | Analog Devices, Inc. |
| 1 | U3 | Fixed 2.5 V linear voltage regulator | ADP3333ARM-2.5Z | Analog Devices, Inc. |
| 1 | U4 | Dual op amp, (8-lead SOIC) | OP293ESZ | Analog Devices, Inc. |
| 1 | U2 | Fixed 3.3 V linear voltage regulator | ADP3333ARM3.3Z | Analog Devices, Inc. |
| 1 | Y1 | 32.768 kHz watch crystal | FEC 3160312 | Farnell |
| 1 | S4 | SW/8-way DIP switch | FEC 9479112 | Farnell |
| 3 | S1, S2, S3 | PCB-mounted push-button switch | FEC 177807 | Farnell |
| 1 | D4 | 1.8 mm miniature LED (green) | FEC 515620 | Fairchild Semiconductor |
| 1 | D6 | 1.8 mm miniature LED (red) | FEC 515607 | Fairchild Semiconductor |
| 1 | D1 | PRLL4002 diode | BAV103TPMSCT-ND | Digi-Key |
| 6 | C3, C14, C16, C17, C29, C30 | 10 µF surface-mount tantalum capacitor, TAJ-B case | FEC 1135105 | Farnell |
| 14 | C1, C2, C4, C5, C8 to C13, C24 | 0.1 µF surface-mount ceramic capacitor, 0603 case | FEC 9406204 | Farnell |
| 1 | C15 | 4.7 µF surface-mount tantalum capacitor, TAJ-B case | FEC 1432459 | Farnell |
| 9 | C6, C7, C20 to C27 | 10 nF surface-mount ceramic capacitor, 0603 case | FEC 722236 | Farnell |
| 2 | C18, C19 | 12 pF surface-mount ceramic capacitor, 0603 case | FEC 721979 | Farnell |
| 1 | RTD | 100 Ω Class B 0805 RTD | PCS 1.1503.1 | Enercorp (Embassy Components) |
| 1 | R1 | 5.6 kΩ surface-mount resistor, 0605 case | FEC 9331352 | Farnell |
| 3 | R12, R12, R21 | 560 Ω surface-mount resistor, 0603 case | FEC 9331344 | Farnell |
| 14 | R2 to R5, R11 to R20 | 0 Ω surface-mount resistor, 0603 case | FEC 9331662 | Farnell |
| 3 | R8 to R10 | 1 kΩ or 4.7 Ω surface mount resistor, 0603 case | FEC 9330380 | Farnell |
| 1 | R7 | 1.5 Ω surface-mount resistor, 0603 case | FEC 9331832 | Farnell |
| 4 | R22, R26 to R28 | 100 kΩ surface-mount resistor, 0603 case | FEC 9233628 | Farnell |
| 1 | L1 | Ferrite bead surface-mount inductor, 1206 case | FEC 9526862 | Farnell |
| 1 | J4 | 4-pin, 90° single row header | TSM-104-02-T-SH | Samtec |
| 1 | J3 | 34-pin straight single row header | TSM-120-01-T-SV | Samtec |
| 1 | J2 | 22-pin straight single row header | TSM-122-01-T-SV | Samtec |
| 1 | J5 | 20-pin connector | TSM-104-02-T-SH | Samtec |
| 1 | J1 | PCB mounted power socket (2 mm pin diameter) | KLDX-SMT2-0202-A | KYCON, Inc. |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# NOTES

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