ANALOG DEVICES

DSP Microcomputer

ADSP-2101

FEATURES

Complete DSP Microcomputer
60 ns Instruction Cycle Time from 16.67 MHz Crystal
ADSP-2100 Family Code & Function Compatible
2K Words of On-Chip Program Memory RAM
1K Word of On-Chip Data Memory RAM
Separate Program and Data Buses On-Chip
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer Provides: Zero Overhead Looping Conditional Arithmetic Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
68-Pin PGA, 68-Lead PLCC and 80-Lead PQFP
MIL-STD-883 Compliant Versions Available

GENERAL DESCRIPTION

The ADSP-2101 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. It combines the complete ADSP-2100 architecture (three computational units, data address generators and a program sequencer) with two serial ports, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The ADSP-2101 has 1K words of (16-bit) data memory RAM and 2K words of (24-bit) program memory RAM on chip.

Fabricated in a high-speed, 1.0 micron, double-layer metal CMOS process, the ADSP-2101 operates with a 60 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power operation.

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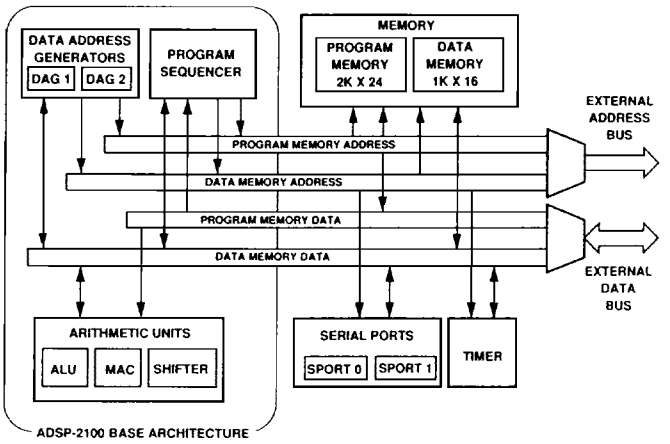
FUNCTIONAL BLOCK DIAGRAM



The ADSP-2101's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2101 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive and transmit data via the two serial ports

Development System

The ADSP-2101 is supported by a complete set of tools for software and hardware system development. The Development Software is a set of modules that supports all ADSP-2100 family processors. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM programmer compatible files. The C Compiler generates ADSP-21xx assembly source code.

Emulators aid in the hardware debugging of ADSP-2101 systems. The full-featured emulator performs a full range of emulation functions including trace and triggering. EZ-Tools are low cost, easy-to-use hardware tools. The EZ-ICE® emulator provides basic functions like changing register values and setting breakpoints. The EZ-LAB® demonstration board is a complete ADSP-2101 system that executes EPROM-based programs. The EZ-Kit package is a DSP design kit that contains an EZ-LAB board, development software, DSP textbooks, and example programs.

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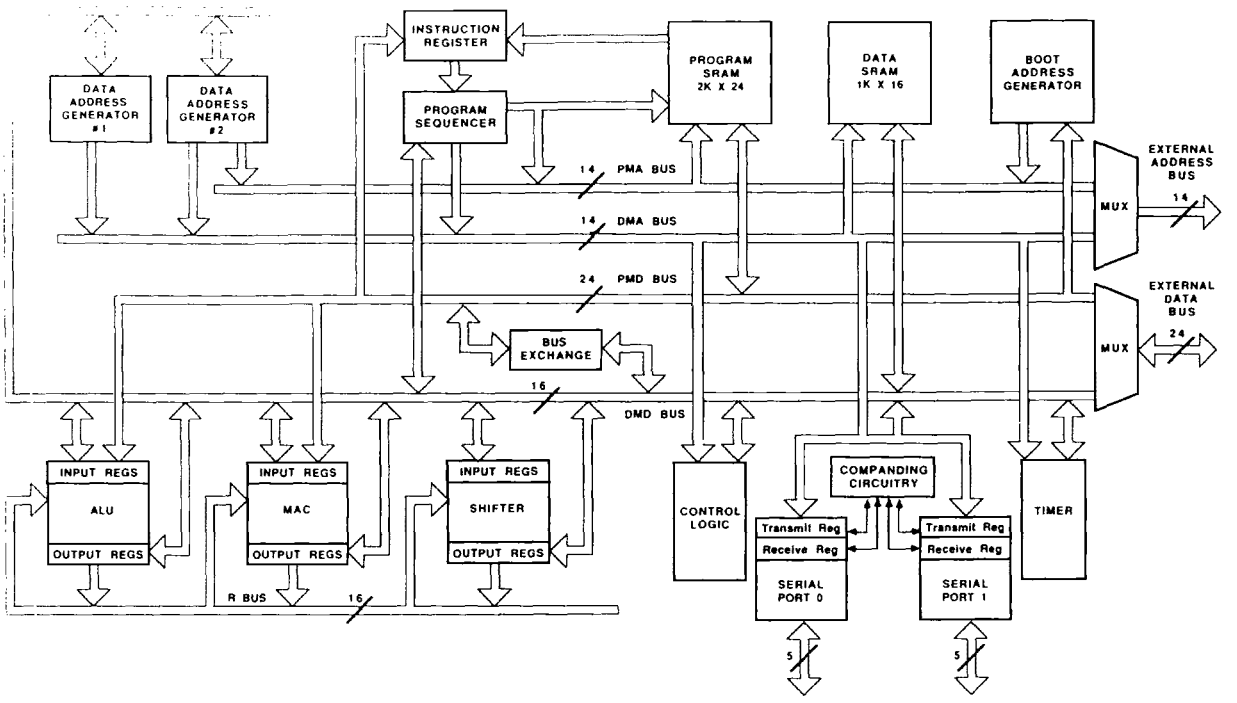


Figure 1. ADSP-2101 Block Diagram

Additional Information

This data sheet provides a general overview of ADSP-2101 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the Development System and ADSP-2101 programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals*.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2101. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2101 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers; these are described on the next page in "Serial Ports."

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. The $\overline{\text{BMS}}$, $\overline{\text{DMS}}$ and $\overline{\text{PMS}}$ signals indicate which memory space the external buses are being used for.

Program memory can store both instructions and data, permitting the ADSP-2101 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2101 can fetch an operand from on-board program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of buses with bus request/grant signals ($\overline{\text{BR}}$ and $\overline{\text{BG}}$). One execution mode allows the ADSP-2101 to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

The ADSP-2101 can respond to six interrupts. There can be up to three external interrupts, configured as edge or level sensi-

tive. Internal interrupts can be generated by the Timer and the Serial Ports, "SPORTs." There is also a master $\overline{\text{RESET}}$ signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use an external 200 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-2101 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2101 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-2101 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Each serial port has a 5-pin interface consisting of the following signals.

Signal Name	Function
SCLK	Serial clock (I/O)
RFS	Receive frame synchronization (I/O)
TFS	Transmit frame synchronization (I/O)
DR	Serial data receive
DT	Serial data transmit

Here is a brief list of the capabilities of the ADSP-2101 SPORTs. (Refer to User's Manual for further details.)

- Bidirectional: each SPORT has a separate transmit and receive section.
- Double-buffered: each SPORT section (both receive and transmit) has a data register accessible to the user and an internal transfer register. The double-buffering provides additional time to service the SPORT.
- Flexible clocking: each SPORT can use an external serial clock (from 0 Hz to 12.5 MHz) or generate its own (up to 1/2 the processor frequency).
- Flexible framing: framings for the receive and transmit sections on each SPORT are independent. Each section can run in a frameless mode, with internally generated or externally generated frame synchronization signals, with active high or inverted frame signals, with either of two pulse widths/timings. The receive and transmit sections share the same serial clock.
- Flexible word length: each SPORT supports serial data word lengths from three to sixteen bits.
- Companding in hardware: each SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711. Different companding can be used for each SPORT, for example, A-law for SPORT0 and μ-law for SPORT1.
- Flexible interrupt scheme: each SPORT section (receive and transmit) can generate a unique interrupt upon completing a data word transfer or after transferring an entire buffer (see next item).
- Auto-buffering with single-cycle overhead: using the ADSP-2101 DAGs, each SPORT can receive and/or transmit an entire circular buffer of data with an overhead of only one cycle per data word. Transfers to and from the SPORT and the circular buffer are automatic in this mode and do not require additional programming. An interrupt is generated only when the receive buffer is full or the transmit buffer is empty.
- Multichannel capability: SPORT0 provides a multichannel interface for selective receipt and transmission of arbitrary data channels from a twenty-four or thirty-two word, time-division multiplexed, serial bitstream. This is especially useful for T1 or CEPT interfaces or as a network communication scheme for multiple processors.
- Alternate configuration: SPORT1 can be configured as two external interrupt inputs ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-2101 is available in a 68-pin PGA, a 68-lead PLCC and an 80-lead PQFP.

Table I. ADSP-2101 Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Address	14	O	Address Output for Program, Data and Boot Memory Spaces.
Data	24	I/O	Data I/O pins for program and data memories. Input only for Boot memory space, with two MSBs used as Boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor Reset Input.
$\overline{\text{IRQ2}}$	1	I	External Interrupt Request #2.
$\overline{\text{BR}}$	1	I	External Bus Request Input.
$\overline{\text{BG}}$	1	O	External Bus Grant Output.
$\overline{\text{PMS}}$	1	O	External Program Memory Select.
$\overline{\text{DMS}}$	1	O	External Data Memory Select.
$\overline{\text{BMS}}$	1	O	Boot Memory Select.
$\overline{\text{RD}}$	1	O	External Memory Read Enable.
$\overline{\text{WR}}$	1	O	External Memory Write Enable.
MMAP	1	I	Memory Map Select.
CLKIN, XTAL	2	I	External Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output.
SPORT0	5	I/O	Serial Port 0 I/O Pins. (TFS0, RFS0, DT0, DR0, SCLK0).
SPORT1	5	I/O	Serial Port 1 I/O Pins.
or			
$\overline{\text{IRQ1}}$, TFS1	1	I	External Interrupt Request #1
$\overline{\text{IRQ0}}$, RFS1	1	I	External Interrupt Request #0
SCLK1	1	I/O	Programmable Clock Output
FO, DT1	1	O	Flag Output Pin
FI, DR1	1	I	Flag Input Pin

Interrupts

The interrupt controller allows the processor to respond to the six possible interrupts with a minimum of overhead. The ADSP-2101 provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of serial port 1. The ADSP-2101 also supports internal interrupts from the timer and the two serial ports. The interrupt levels are internally prioritized and individually maskable. The input pins can be programmed to be either level- or edge-sensitive. The priorities of all six interrupts are shown in Table II.

Table II. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
$\overline{IRQ2}$ (external pin)	0004 (*highest priority*)
SPORT0 Transmit (internal)	0008
SPORT0 Receive (internal)	000C
SPORT1 Transmit (internal) or $\overline{IRQ1}$ (external)	0010
SPORT1 Receive (internal) or $\overline{IRQ0}$ (external)	0014
Timer (internal)	0018 (*lowest priority*)

The ADSP-2101 supports a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt level. Interrupts can optionally be nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length, so that simple service routines can be coded entirely in this space. Longer routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on Bit 4 in ICNTL, interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially with only one interrupt service active at a time.

The 12-bit interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each of the six possible interrupts.

When responding to an interrupt, the status registers ASTAT, MSTAT, IMASK are pushed onto the status stack, and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep to allow interrupt nesting. The stack is automatically popped when a return from the interrupt is executed.

SYSTEM INTERFACE

Figure 4 shows a basic system configuration with the ADSP-2101, two serial devices, a boot EPROM and optional external program and data memories. Up to 15K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories.

The ADSP-2101 also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

The ADSP-2101 may be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input may not be halted, changed during operation, or operated below the specified frequency.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal is connected to the processors's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

Because the ADSP-2101 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency microprocessor grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor, synchronized to the processor's internal cycles.

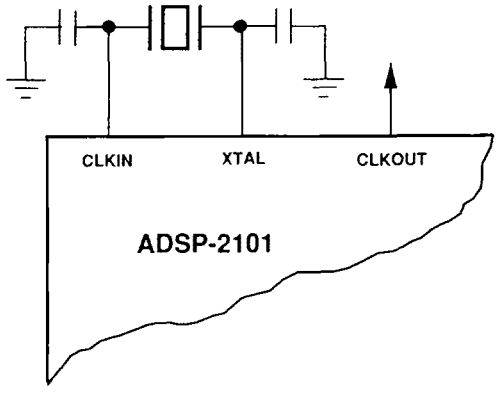


Figure 2. External Crystal Connections

Reset

The $\overline{RESET}$ signal initiates a master reset of the ADSP-2101. The $\overline{RESET}$ signal must be asserted when the chip is powered up to assure proper initialization. $\overline{RESET}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{RESET}$ is activated at any time after power-up, the clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 1000 t_{CK} cycles will ensure that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{RESET}$ signal should be held low. On any subsequent resets, the $\overline{RESET}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{RESET}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{RESET}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{RESET}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000.

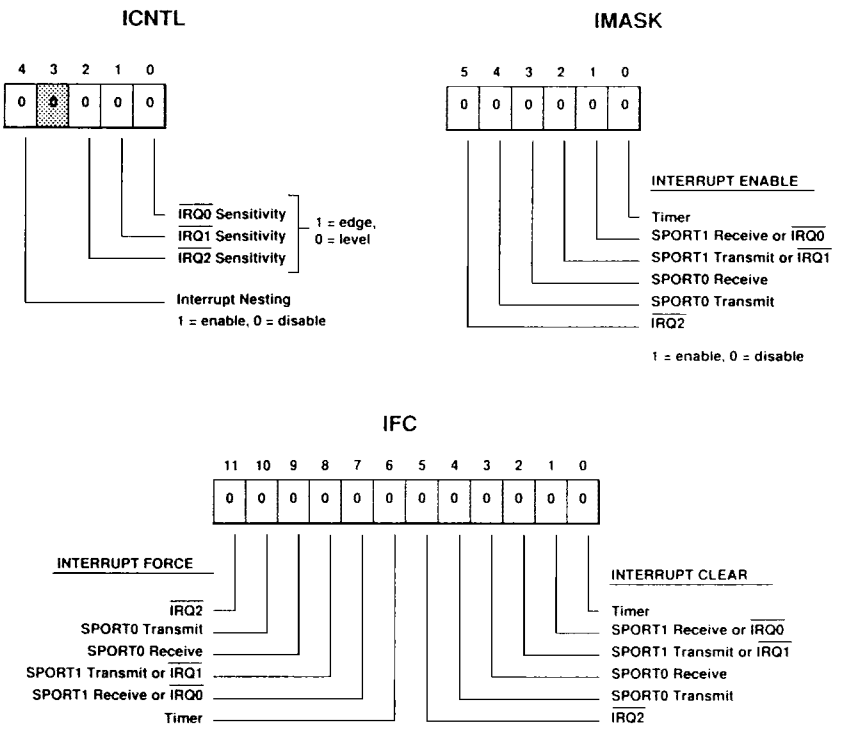
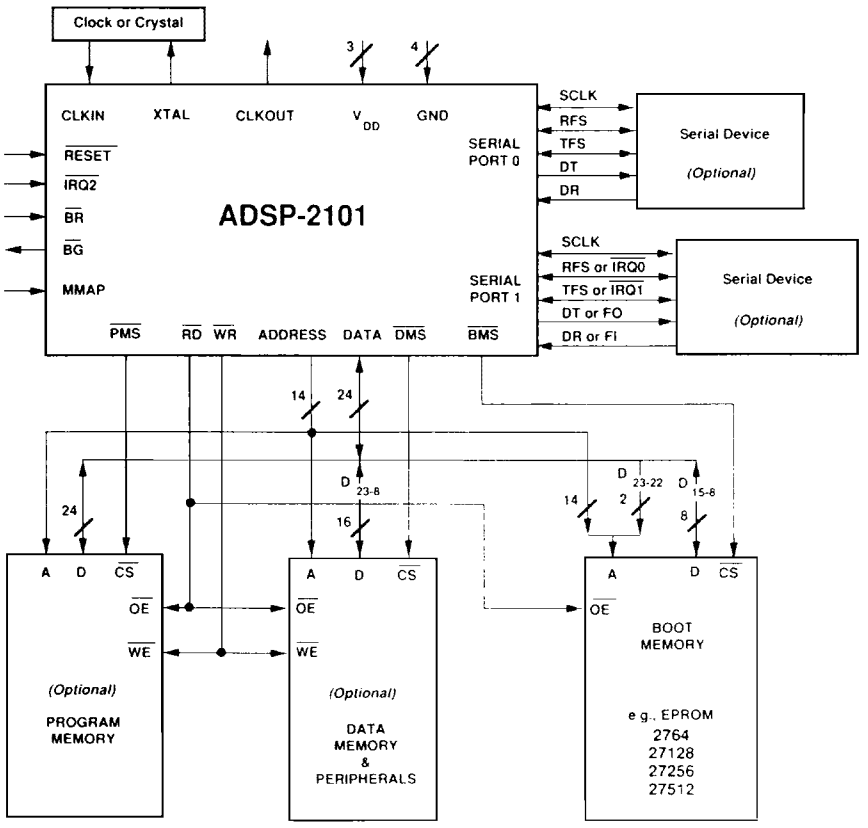


Figure 3. Interrupt Registers



NOTE: The two MSBs of the Boot EPROM Address are also the two MSBs of the Data Bus. This is only required for the 27256 and 27512.

Figure 4. ADSP-2101 System Interface

Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words, of which 2K are on-chip. The data bus is bidirectional and 24 bits wide to external program memory. Program memory may contain code and data.

The program memory data lines are bidirectional. The program memory select ($\overline{PMS}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-2101 writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the two configurations. When MMAP = 0, internal RAM occupies 2K words beginning at address 0x0000; external program memory uses the remaining 14K words beginning at address 0x0800. In this configuration, the boot loading sequence (described in "Boot Memory Interface") is automatically initiated when $\overline{RESET}$ is released.

When MMAP = 1, 14K words of external program memory begin at address 0x0000 and internal RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not loaded although it can be written to and read from under program control.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{RESET}$.

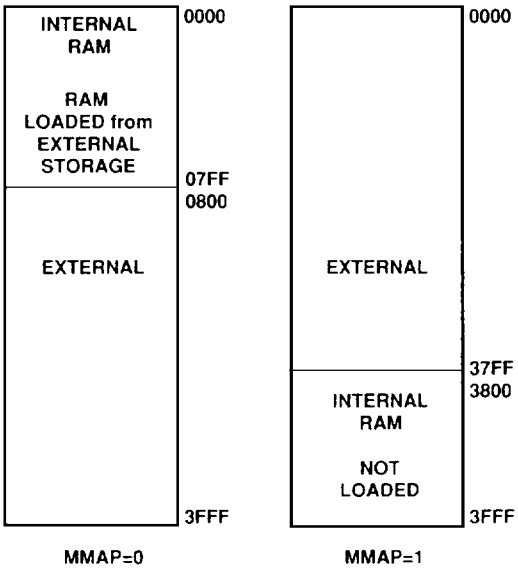


Figure 5. ADSP-2101 Program Memory Maps

Data Memory Interface

The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-2101 supports memory-mapped I/O, with the peripherals memory mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map

The on-chip data memory RAM resides in the 1K words of data memory beginning at address 0x3800, as shown in Figure 6. In addition, data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration and serial port operations are located in this region of memory.

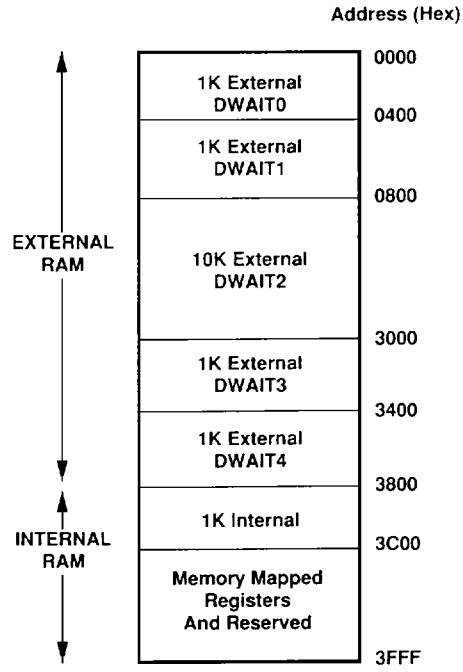


Figure 6. ADSP-2101 Data Memory Map

The remaining 14K of data memory is external. External data memory is divided into five zones, each associated with its own wait state generator. This allows slower peripherals to be memory mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{RESET}$.

Boot Memory Interface

The boot memory space consists of an external 64K by 8 space, divided into eight separate 8K by 8 pages. Three bits in the system control register select which page is loaded by the boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 3 wait states after $\overline{RESET}$. This allows the ADSP-2101 to boot from a single, low cost EPROM such as a 27256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

$\overline{BR}$ is recognized during the booting sequence. The bus is granted after the completion of loading the current byte. $\overline{BR}$ during booting may be used to implement booting under the control of a host processor.

The ADSP-2100 Family Assembler and Linker support the creation of programs and data structures requiring multiple boot pages during execution.

Bus Interface

The ADSP-2101 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2101 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the same cycle by:

- tristating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If the Go mode is set, however, the ADSP-2101 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2101 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not tristate the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes, up to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted; the ADSP-2101 will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

ADSP-2101 REGISTERS

Figure 7 summarizes all the registers in the ADSP-2101. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT register, timer registers and SPORT control registers are all mapped into data memory; that is, you access these registers by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

A secondary set of registers in all computational units allows a single-cycle context switch.

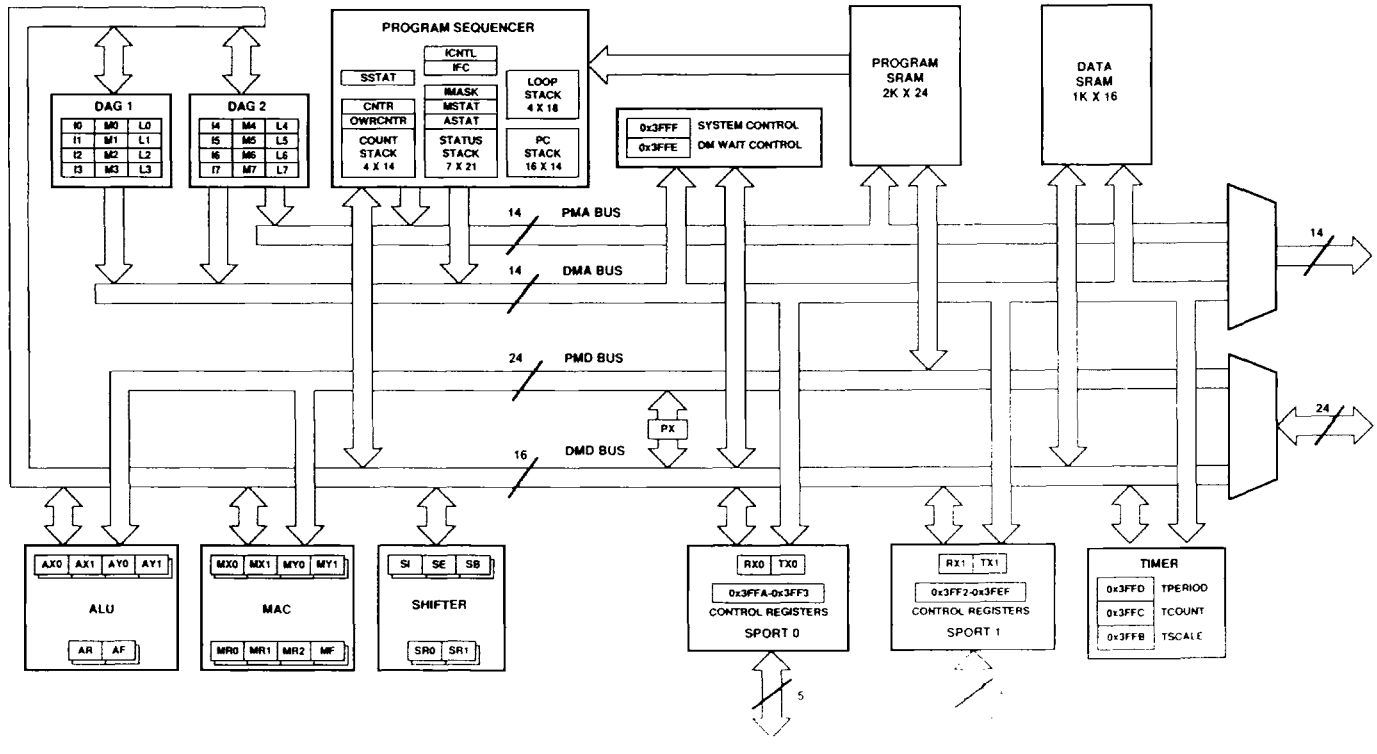
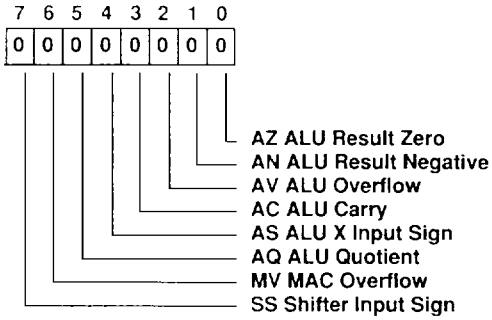
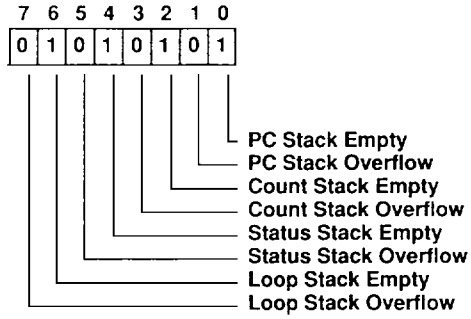


Figure 7. ADSP-2101 Registe

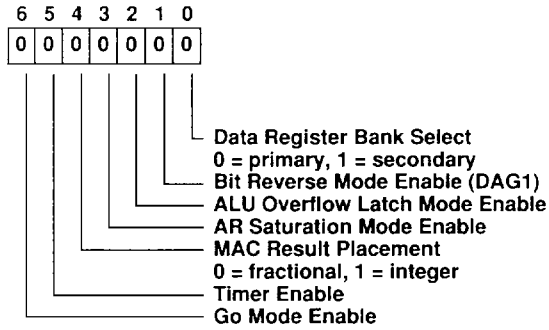
ASTAT



SSTAT (Read-Only)

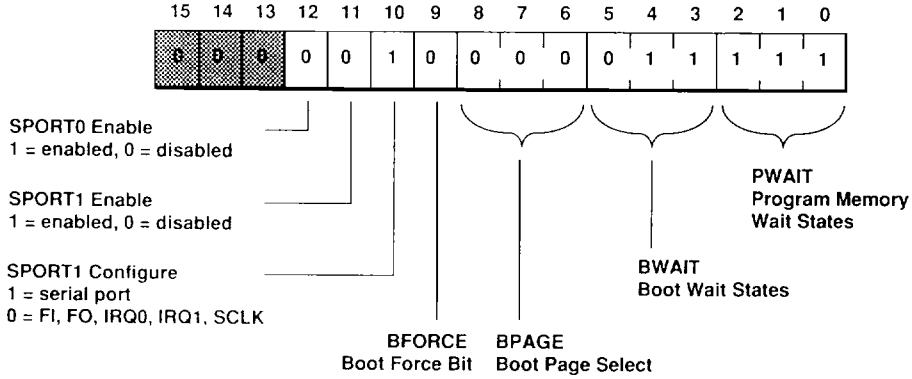


MSTAT



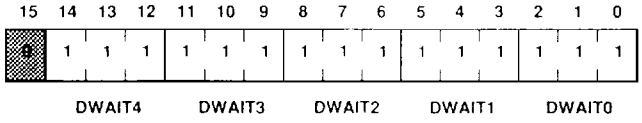
System Control Register

0x3FFF

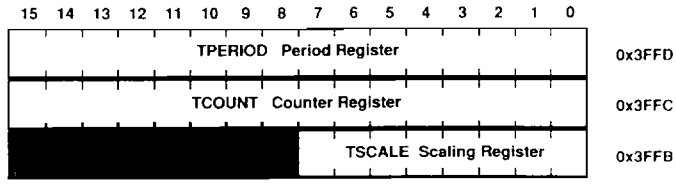


Data Memory Wait State Control Register

0x3FFE



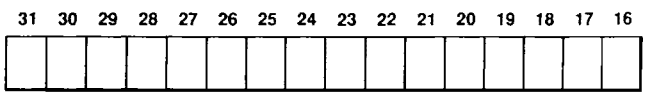
Timer Registers



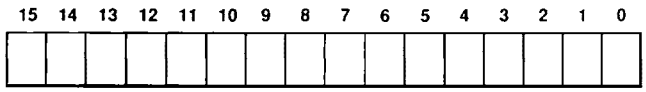
SPORT0 Multichannel Receive Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FFA



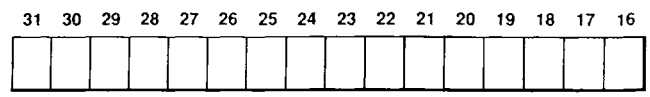
0x3FF9



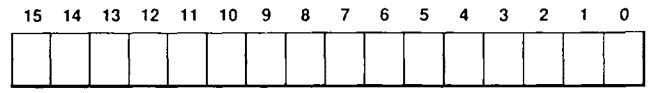
SPORT0 Multichannel Transmit Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FF8

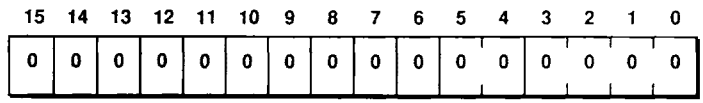


0x3FF7



SPORT0 Control Register

0x3FF6



Multichannel Enable MCE

Internal Serial Clock Generation ISCLK

Receive Frame Sync Required RFSR

Receive Frame Sync Width RFSW

Multichannel Frame Delay MFD
Only If Multichannel Mode Enabled

Transmit Frame Sync Required TFSR

Transmit Frame Sync Width TFSW

ITFS Internal Transmit Frame Sync Enable
(or MCL Multichannel Length; 1 = 32 words, 0 = 24 words
Only If Multichannel Mode Enabled)

SLEN Serial Word Length

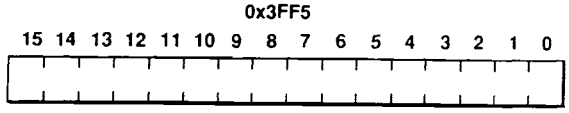
DTYPE Data Format
00 = right justify, zero-fill unused MSBs
01 = right justify, sign extend into unused MSBs
10 = compand using μ-law
11 = compand using A-law

INVRFS Invert Receive Frame Sync

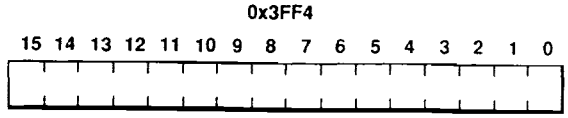
INVTFS Invert Transmit Frame Sync
(or INVTDV Invert Transmit Data Valid
Only If Multichannel Mode Enabled)

IRFS Internal Receive Frame Sync Enable

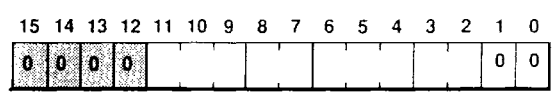
SPORT0 SCLKDIV
Serial Clock Divide Modulus
0x3FF5

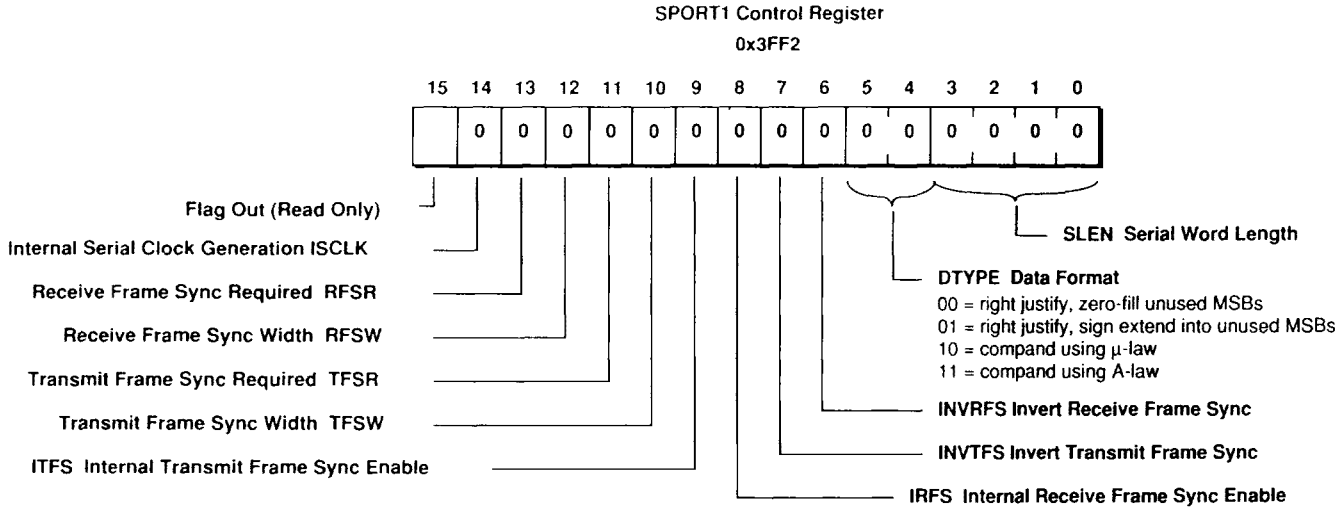


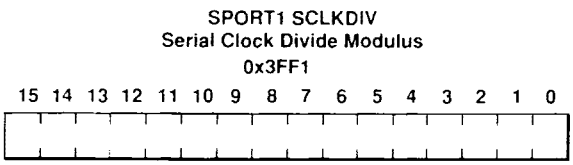
SPORT0 RFSDIV
Receive Frame Sync Divide Modulus
0x3FF4

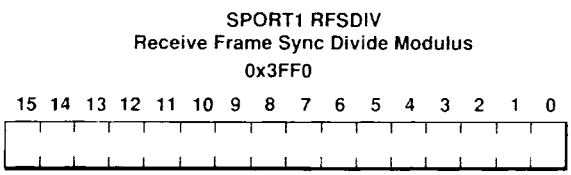


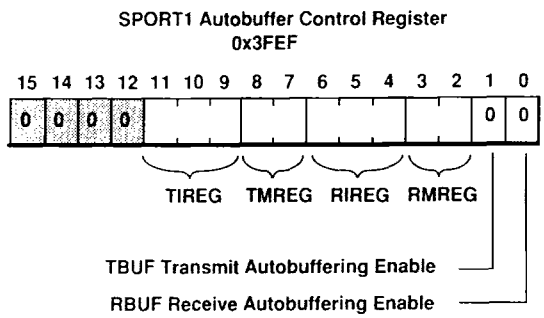
SPORT0 Autobuffer Control Register
0x3FF3











INSTRUCTION SET DESCRIPTION

The ADSP-2100 family assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics. Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Each of these instruction types is described briefly. The complete instruction set is summarized on the following page. The *ADSP-2100 Family User's Manual* and the *ADSP-2100 Family Assembler Manual* contain a complete reference to the instruction set.

ADSP-2100 Family Compatibility

The ADSP-2101 instruction set is a superset of the ADSP-2100 instruction set. The ADSP-2101 is source and object code compatible with all processors of the ADSP-2100 family. An ADSP-2100 program may need to be relocated to utilize internal memory and conform to the ADSP-2101's interrupt vector and reset vector map.

The TRAP instruction of the ADSP-2100, however, is not supported since the ADSP-2101 does not have the TRAP/$\overline{\text{HALT}}$ signals. The TRAP instruction executes as a NOP on the ADSP-2101.

Condition Codes

The condition codes are used to determine whether a conditional instruction, such as a jump, trap, call, return, MAC saturation, or arithmetic operation, is performed. The sixteen basic composite status conditions and their derivations are shown in Table III. Since arithmetic status is latched into ASTAT at the end of a processor cycle, the condition logic represents conditions generated on the previous cycle.

Table III. Condition Codes

Code	Status Condition	True If:
EQ	ALU Equal Zero	AZ = 1
NE	ALU Not Equal Zero	AZ = 0
LT	ALU Less Than Zero	AN .XOR. AV = 1
GE	ALU Greater Than or Equal Zero	AN .XOR. AV = 0
LE	ALU Less Than or Equal Zero	(AN .XOR. AV) .OR. AZ = 1
GT	ALU Greater Than Zero	(AN .XOR. AV) .OR. AZ = 0
AC	ALU Carry	AC = 1
NOT AC	Not ALU Carry	AC = 0
AV	ALU Overflow	AV = 1
NOT AV	Not ALU Overflow	AV = 0
MV	MAC Overflow	MV = 1
NOT MV	Not MAC Overflow	MV = 0
NEG	ALU X Input Sign Negative	AS = 1
POS	ALU X Input Sign Positive	AS = 0
NOT CE	Not Counter Expired	CE = 0
FOREVER	Always	Always True

In addition to the basic sixteen conditions, the JUMP and CALL instructions also support the use of the FI (Flag In) pin as a conditional flag. This pin is one of the five dual-function pins used for serial port 1. The state of this pin and its complement are available as conditions for JUMP and CALL instructions if the pin is configured as FI rather than DR1.

Table IV. Additional Condition Codes For JUMP and CALL

FLAG_IN	FI pin last sampled 1
NOT FLAG_IN	FI pin last sampled 0

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
        MF = MX0*MY1 (RND), MX0 = DM (I2,M1) ; {MF = error*beta}
        MR = MX0*MF (RND), AY0 = PM (I6,M5) ;
        DO adapt UNTIL CE;
          AR = MR1 + AY0, MX0 = DM (I2,M1), AY0 = PM (I6,M7) ;
adapt:  PM(I6,M6) = AR, MR = MX0*MF (RND) ;
        MODIFY (I2, M3) ;                    {Point to oldest data}
        MODIFY (I6, M7) ;                    {Point to start of data}
```

INSTRUCTION SET SUMMARY

Key

UPPERCASE	Assembler keyword; exact syntax of instruction
[text]	Parts of the instruction in brackets are optional
x | y | z	Choose x, y or z
[,...]	Any of the operations allowed by this instruction can be combined in any order, separated by commas
Ia, Mb or Ic, Md	Index and modify registers for indirect addressing
x	X input; permissible registers depend on instruction
y	Y input; permissible registers depend on instruction
<data>	Immediate data value
<address>	Immediate address value
condition	Condition from Table x
dreg	Computation unit data register
reg	Any register (except memory-mapped registers)
ALU	Any ALU instruction (except division)
MAC	Any multiply/accumulate instruction
SHIFT	Any shifter instruction (except shift immediate)

ALU Instructions

```
[IF condition]  AR | AF  =  x + y   [+C]      ;
                           x + C              ;
                           x - y   [+C - 1]   ;
                           y - x   [+C - 1]   ;
                           y + 1              ;
                           y - 1              ;
                           x AND | OR | XOR y ;
                           PASS x | y | 0 | 1 ;
                           -x | y  ;
                           NOT x | y  ;
                           ABS x      ;
DIVS y, x;
DIVQ x;
```

MAC Instructions

```
[IF condition]  MR | MF  =  x * y          (SS | SU | US | UU | RND) ;
                            MR + x * y     (SS | SU | US | UU | RND) ;
                            MR - x * y     (SS | SU | US | UU | RND) ;
                            MR             [(RND)] ;
                            0 ;
IF MV SAT MR;
```

Shifter Instructions

```
[IF condition]  SR = [SR OR] ASHIFT | LSHIFT | NORM x (HI | LO) ;
[IF condition]  SE = EXP x  (HI | LO | HIX) ;
[IF condition]  SB = EXPADJ x ;
SR = [SR OR]  ASHIFT | LSHIFT x  BY <data>  (HI | LO) ;
```

Move Instructions

```
reg              = reg | <data> | DM (<address>);
DM (<address>)   = reg;
dreg             = DM (Ia, Mb);
DM (Ia, Mb)      = dreg | <data>;
dreg             = PM (Ic, Md);
PM (Ic, Md)      = dreg;
```

Multifunction Instructions

```
ALU | MAC*,              x = DM (Ia, Mb) ,        y = PM (Ic, Md);
x = DM (Ia, Mb),         y = PM (Ic, Md);
ALU | MAC | SHIFT*,      dreg = DM | PM (Ia, Mb);
DM | PM (Ia, Mb) = dreg ,  ALU | MAC | SHIFT*;
ALU | MAC | SHIFT*,      dreg = dreg;
```

*All computation is unconditional; Division and Shift Immediate operations prohibited.

Program Flow Control Instructions

```
[IF condition]          JUMP  CALL        (Ic) | <address> ;
IF [NOT] FLAG_IN        JUMP  CALL        <address>       ;
[IF condition]          RTS  RTI ;
DO <address>            {UNTIL termination};
IDLE ;
```

Miscellaneous Instructions

```
[IF condition]      SET  RESET  TOGGLE      FLAG_OUT ;
ENA | DIS           BIT_REV     [....] ,
                    AV_LATCH
                    AR_SAT
                    SEC_REG
                    TIMER
                    G_MODE
                    M_MODE
[PUSH  POP  STS]
MSTAT
```

ADSP-2101—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	−55	+125	°C

Refer to Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B/T Grades Min	K/B/T Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = −0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = −100 μA[10]	V_{DD} − 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	μA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	μA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	μA
I_{DD}	Supply Current (Idle)[8, 9]	@ V_{DD} = max		14	mA
I_{DD}	Supply Current (Dynamic)[9]	@ V_{DD} = max, t_{CK} = 60 ns[11]		81	mA
		@ V_{DD} = max, t_{CK} = 80 ns[11]		64	mA
		@ V_{DD} = max, t_{CK} = 97.6 ns[11]		55	mA
C_I	Input Pin Capacitance[1, 10, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 10, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1.
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, DT0, DT1, CLKOUT.
[3]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1.
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1.
[5]$\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 input pins.
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[7]Although specified for TTL outputs, all ADSP-2101 outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc loads.
[8]Idle refers to ADSP-2101 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[9]Current reflects device operating with no output loads.
[10]Guaranteed but not tested.
[11]V_{IN} = 0.4 V and 2.4 V.
[12]Applies to PGA, PLCC and PQFP package types.
[13]Output pin capacitance is the capacitive load for any tristated output pin.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} +0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range (Ambient) . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PLCC and PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-2101 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per method 3015 of MIL-STD-883C, the ADSP-2101 has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to *Analog Devices's ESD Prevention Manual.*

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2101 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0–A13 $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	Address Setup to Write End
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

Parameter		Min	Max	Unit
Clock Signals				
Timing Requirement:				
t_{CK}[1]	CLKIN Period (ADSP-2101–40)	97.6	200	ns
t_{CK}[1]	CLKIN Period (ADSP-2101–50)	80	200	ns
t_{CK}[1]	CLKIN Period (ADSP-2101–66)	60	200	ns
t_{CKL}	CLKIN Width Low	20		ns
t_{CKH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CPL}	CLKOUT Width Low	$0.5t_{CK}$ – 10		ns
t_{CPH}	CLKOUT Width High	$0.5t_{CK}$ – 10		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[2]		ns

NOTES
[1]t_{CK} values within the range of CLKIN period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CPH} = 0.5\ t_{CK} - 10$ ns = 0.5 (60) – 10 ns = 20 ns.
[2]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 1000 processor cycles assuming stable CLKIN (not including crystal oscillator start-up time).

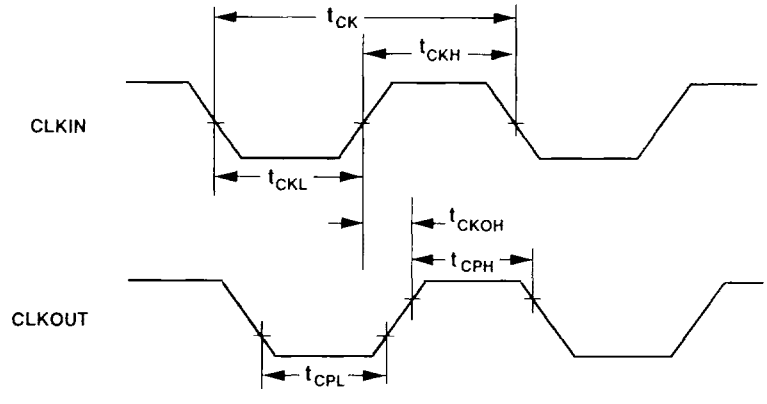


Figure 8. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	IRQx or FI Setup before CLKOUT Low[1, 2]	$0.25t_{CK}$ + 15		ns
t_{IFH}	IRQx or FI Hold after CLKOUT High[1, 2] IRQx = $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$	$0.25t_{CK}$		ns
Switching Characteristic:				
t_{FOH}	FO Hold after CLKOUT High	−5		ns
t_{FOD}	FO Delay from CLKOUT High		15	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

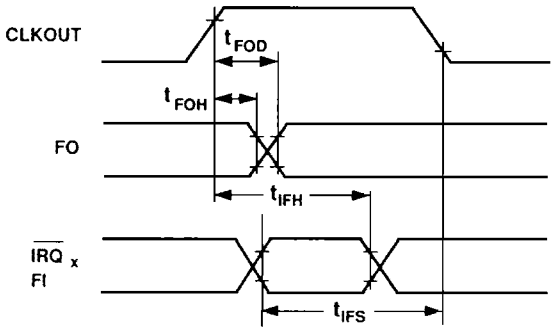


Figure 9. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 20		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ − 10		ns

NOTE
[1]$\overline{BR}$ is a synchronous signal which must meet setup/hold time requirements. Refer to the User's Manual for $\overline{BR}/\overline{BG}$ cycle relationships.

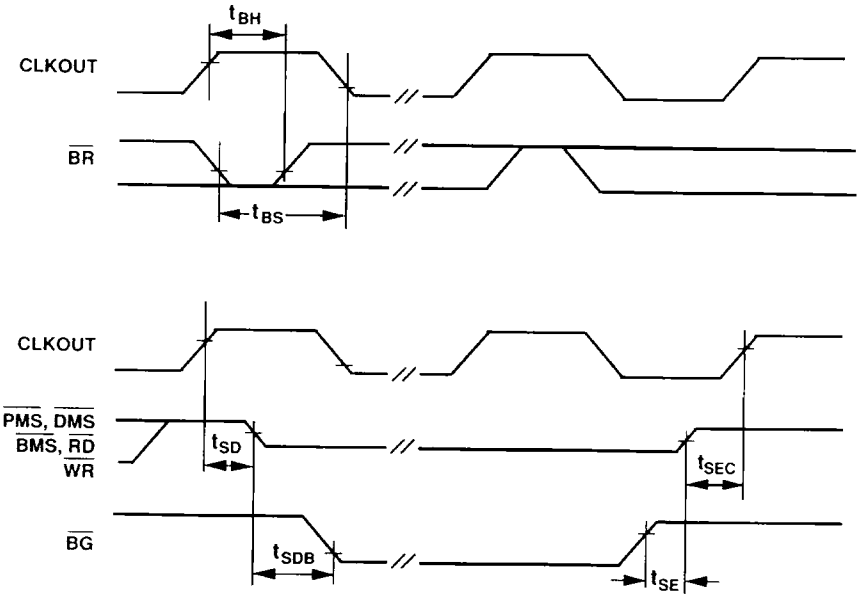


Figure 10. Bus Request – Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$[1]	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

NOTE
[1]t_{AA} (max) = 0.75 t_{CK} – 25 + w for ADSP-2101BG-66, ADSP-2101BP-66, ADSP-2101BS-66.

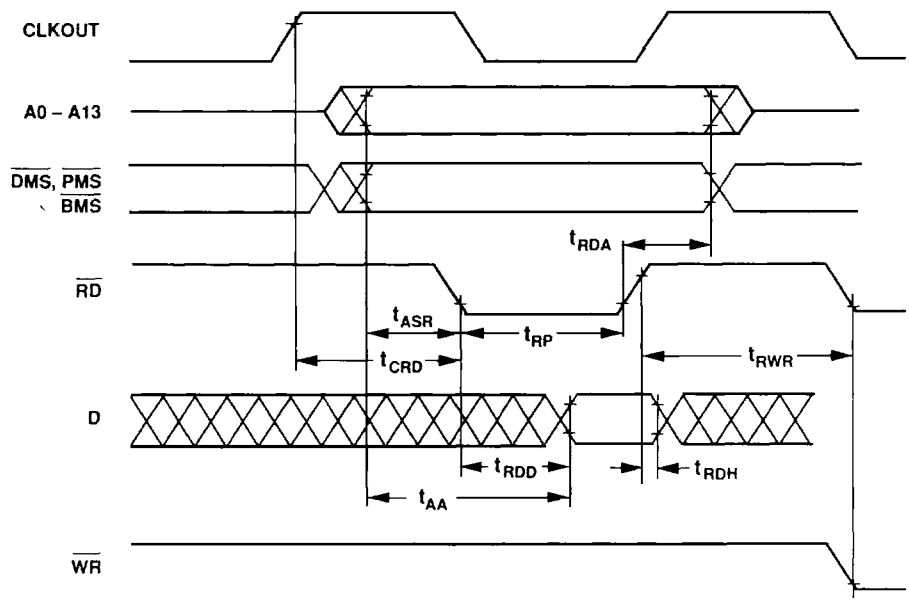


Figure 11. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

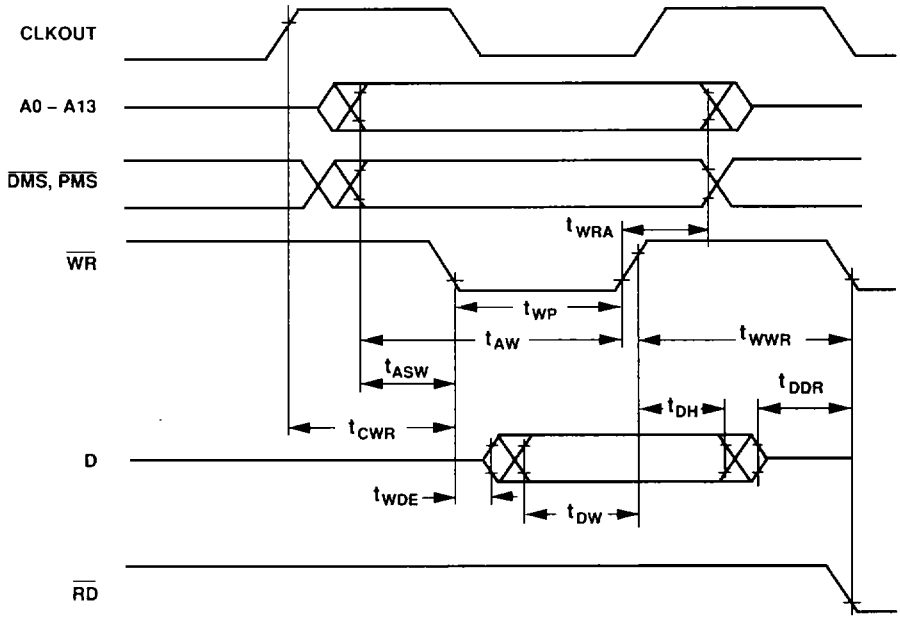


Figure 12. Memory Write

Parameter		ADSP-2101-40 Min	ADSP-2101-40 Max	ADSP-2101-66 ADSP-2101-50 Min	ADSP-2101-66 ADSP-2101-50 Max	Unit
Serial Ports						
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		80		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	10		8		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		ns
t_{SCP}	$SCLK_{in}$ Width	38		30		ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		0		ns
t_{SCDV}	SCLK High to DT Valid		25		20	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		25		20	ns
t_{SCDH}	DT Hold after SCLK High	0		0		ns
t_{TDE}	TFS_{in} (alt) to DT Enable	0		0		ns
t_{TDV}	TFS_{in} (alt) to DT Valid		20		18	ns
t_{SCDD}	SCLK High to DT Disable		30		25	ns
t_{RDV}	RFS_{in} (multichannel, frame delay zero) to DT Valid		25		20	ns

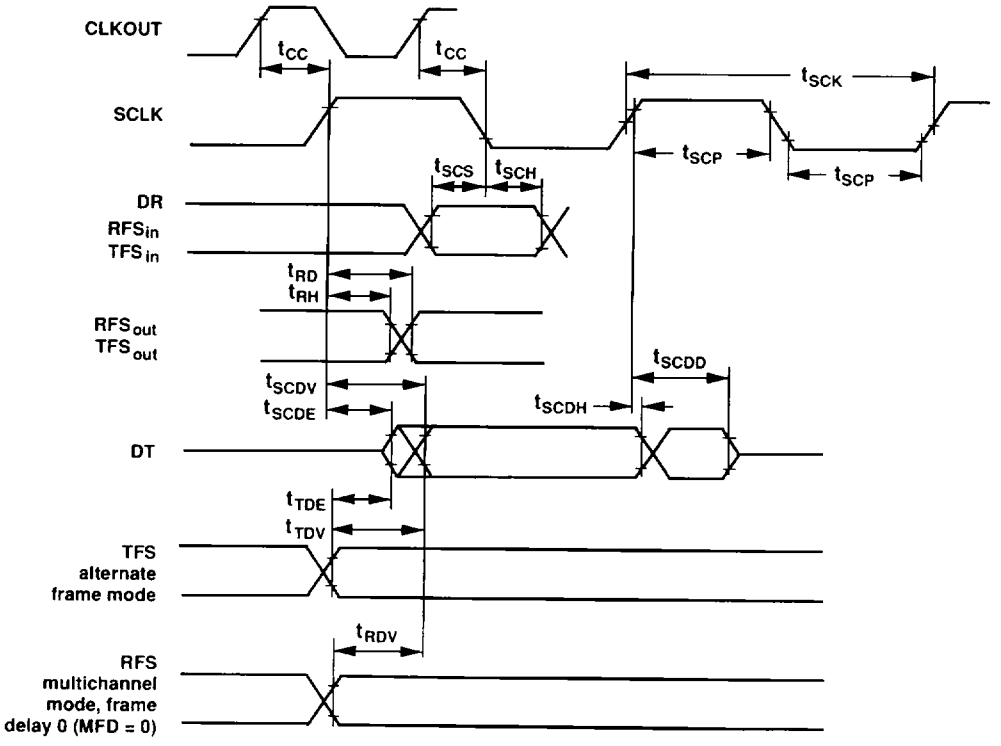


Figure 13. Serial Ports

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{amb} = T_{case} - (PD \times \theta_{CA})$

T_{case} = Case temp in °C
PD = Power dissipation in W
θ_{CA} = Thermal resistance (case-to-ambient)
θ_{JA} = Thermal resistance (junction-to-ambient)
θ_{JC} = Thermal resistance (junction-to-case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PLCC	27°C/W	16°C/W	11°C/W
PGA	18°C/W	9°C/W	9°C/W
PQFP	60.4°C/W	17.9°C/W	42.5°C/W

Power Dissipation

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows.

Assumptions:

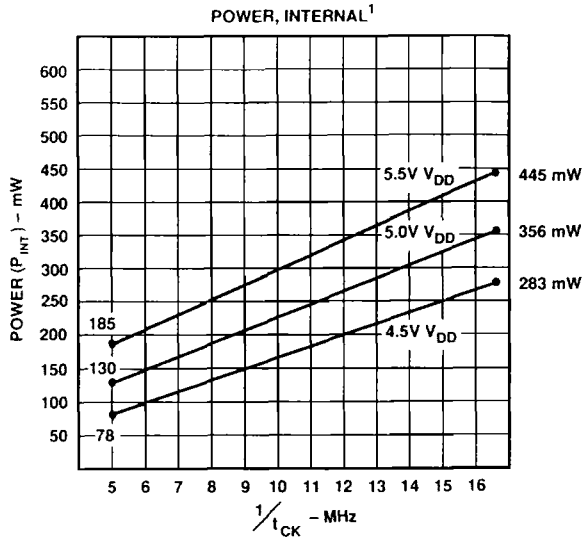
- External data memory is accessed every cycle with 50% of address pins switching.
- External data memory writes occur every other cycle with 50% of address pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 60 ns.

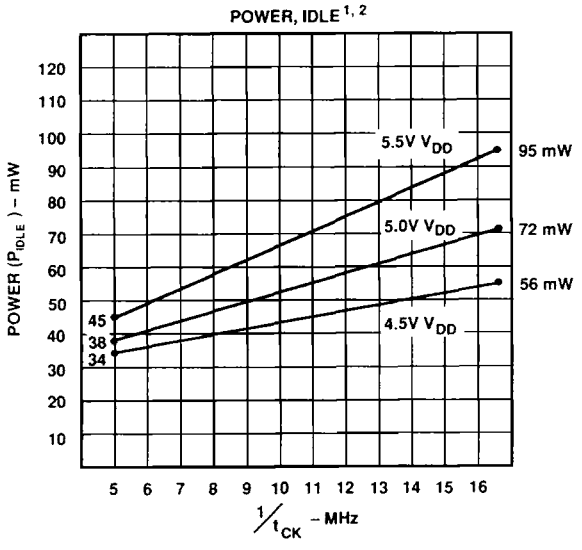
Total Power Dissipation = P_{INT} + ($C \times V_{DD}^2 \times f$)

P_{INT} = internal power dissipation, from Power vs. Frequency graph. $C \times V_{DD}^2 \times f$ is calculated for each output:

	# of Pins	× C	$\times V_{DD}^2$	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 16.67 MHz=	33.34 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 8.34 MHz=	18.77 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 8.34 MHz=	2.09 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 16.67 MHz=	4.18 mW
					58.38 mW

Total power dissipation for this example is P_{INT}+58.38 mW.





VALID FOR ALL TEMPERATURE GRADES.
[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] IDLE REFERS TO ADSP-2101 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 14. Power vs. Frequency

CAPACITIVE LOADING

Figures 15 and 16 show capacitive loading characteristics for the ADSP-2101.

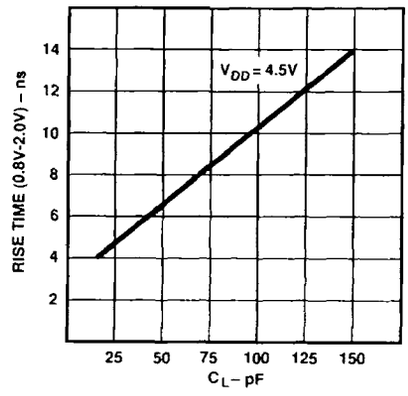


Figure 15. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

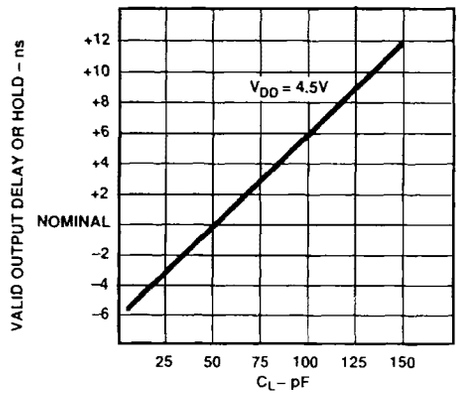


Figure 16. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

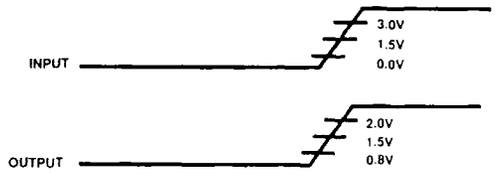


Figure 17. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time, $t_{MEASURED}$, is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

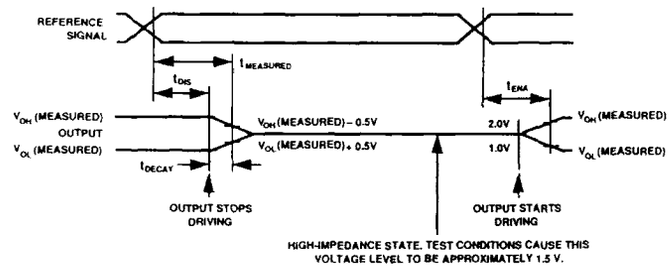


Figure 18. Output Enable/Disable

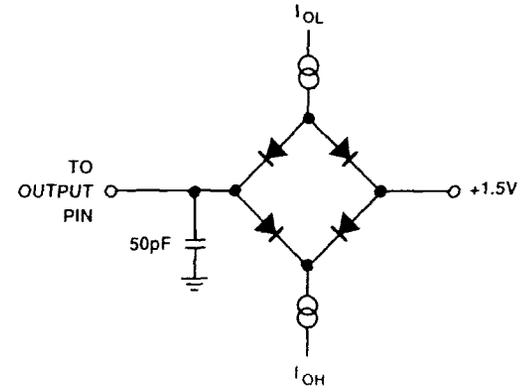


Figure 19. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

EMULATOR MECHANICAL SPECIFICATIONS

If you plan to use the ADSP-2101 Emulator to debug your system, you should take into consideration the physical dimensions of the emulator probe (the part of the emulator that fits in the ADSP-2101 socket in your system). There must be enough clearance around the ADSP-2101 socket to connect the probe.

The emulator probe consists of a target processor board (which holds the emulating ADSP-2101) and two optional boards, an overlay RAM board and interface board. Figures 20 and 21 specify maximum (unless otherwise noted) dimensions for the probe. Figure 20 is the top view of the target processor board; Figure 21 is the side view of the probe including overlay RAM board and interface board. Also shown are the probe fan and PGA-PLCC adaptor. The PGA-PLCC adaptor is available from: Emulation Technology, 2344 Walsh Ave., Bldg. F, Santa Clara, CA 95051, (408) 982-0660, (P/N AP4-68-PGA); and EDI Corp., P.O. Box 366, Patterson, CA 95363, (209) 892-3270, (P/N 68-PGA/PLCC). A PGA-PQFP adaptor is available from Analog Devices.

For more information, see the ADDS-21XX-ICE data sheet.

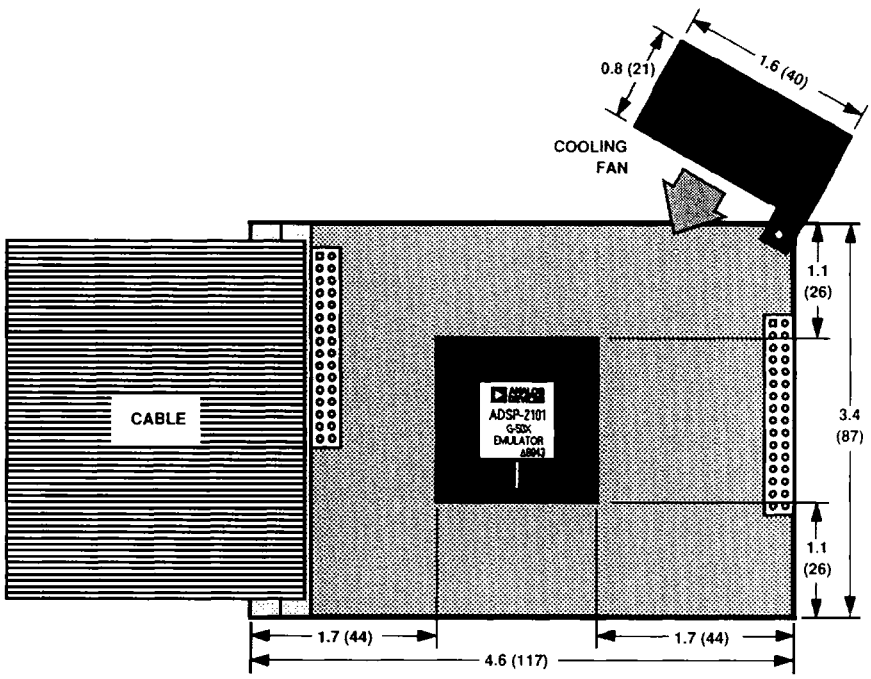


Figure 20. Emulator Probe-Target Processor Board (Top View) Dimensions in Inches (mm)

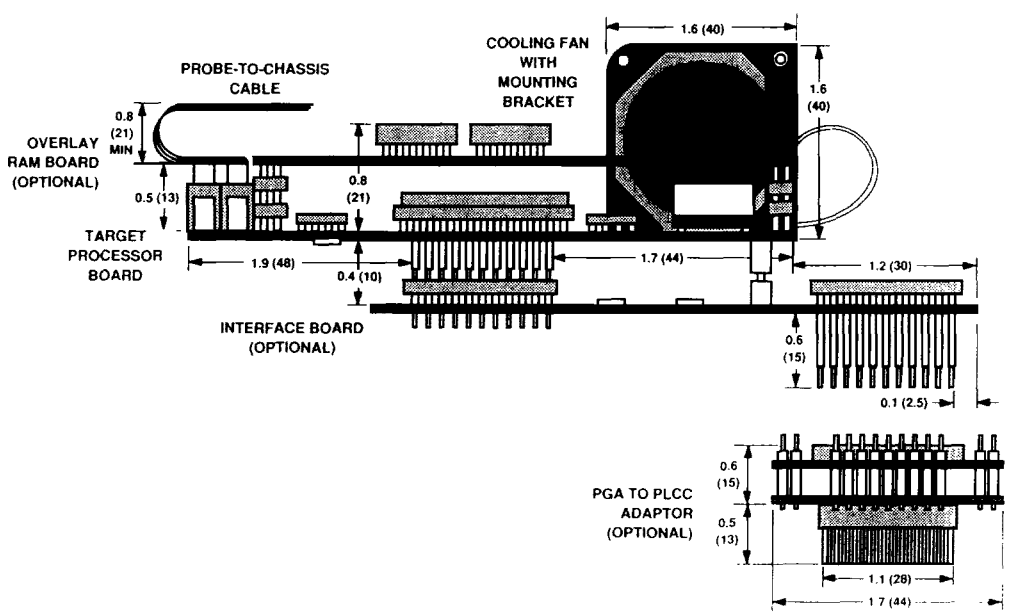
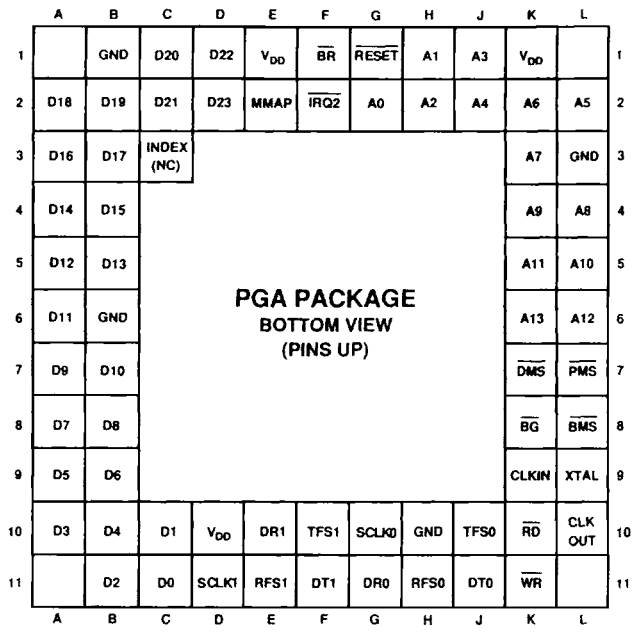
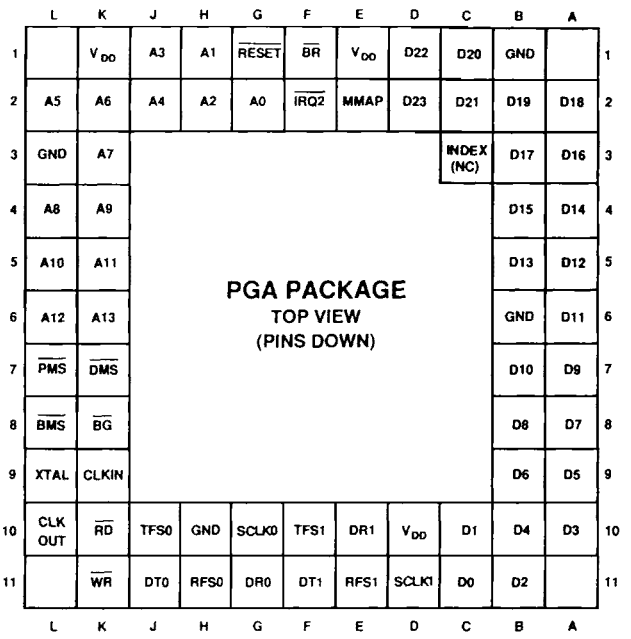


Figure 21. Emulator Probe (Side View) Dimensions in Inches (mm)

PIN CONFIGURATIONS

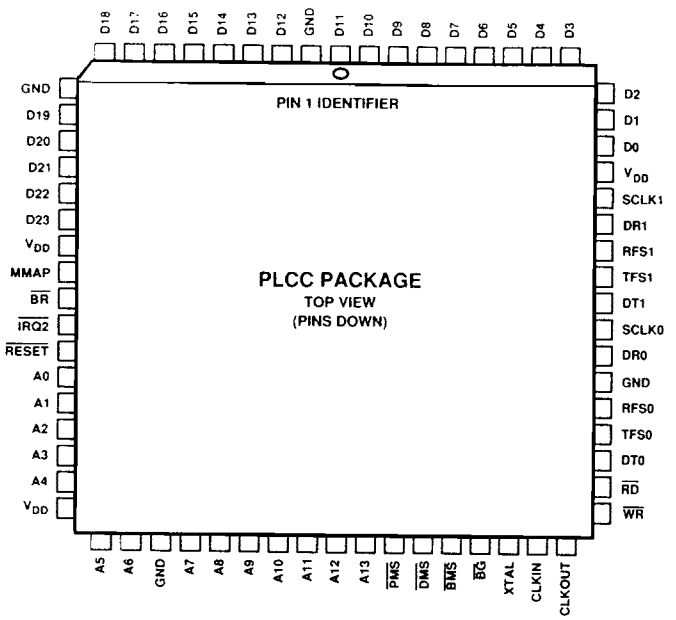


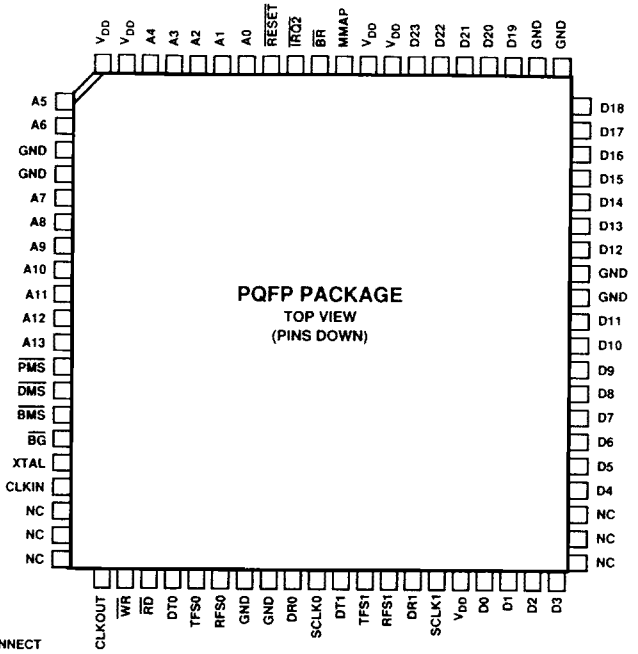


NC = NO CONNECT

PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME
K11	$\overline{WR}$	B1	GND
K10	$\overline{RD}$	B2	D19
J11	DT0	C1	D20
J10	TFS0	C2	D21
H11	RFS0	D1	D22
H10	GND	D2	D23
G11	DR0	E1	V_{DD}
G10	SCLK0	E2	MMAP
F11	DT1	F1	$\overline{BR}$
F10	TFS1	F2	$\overline{IRQ2}$
E11	RFS1	G1	$\overline{RESET}$
E10	DR1	G2	A0
D11	SCLK1	H1	A1
D10	V_{DD}	H2	A2
C11	D0	J1	A3
C10	D1	J2	A4
B11	D2	K1	V_{DD}
A10	D3	L2	A5
B10	D4	K2	A6
A9	D5	L3	GND
B9	D6	K3	A7
A8	D7	L4	A8
B8	D8	K4	A9
A7	D9	L5	A10
B7	D10	K5	A11
A6	D11	L6	A12
B6	GND	K6	A13
A5	D12	L7	$\overline{PMS}$
B5	D13	K7	$\overline{DMS}$
A4	D14	L8	$\overline{BMS}$
B4	D15	K8	$\overline{BG}$
A3	D16	L9	XTAL
B3	D17	K9	CLKIN
A2	D18	L10	CLKOUT
		C3	INDEX (NC)

PIN CONFIGURATIONS



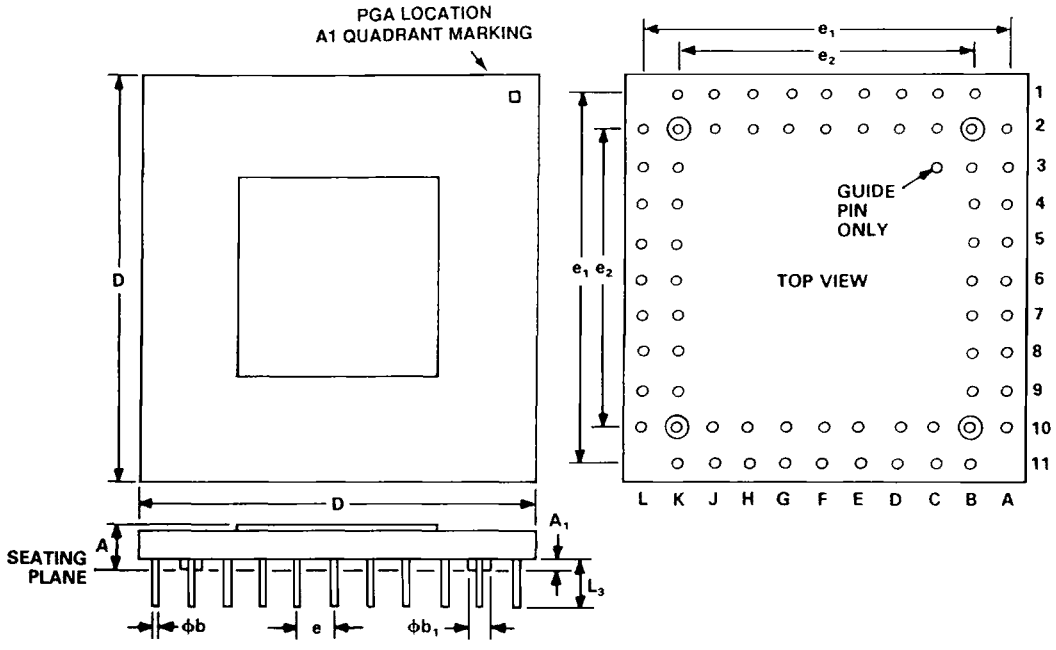


NC = NO CONNECT

PLCC NUMBER	PIN NAME	PLCC NUMBER	PIN NAME
1	D11	35	A12
2	GND	36	A13
3	D12	37	$\overline{PMS}$
4	D13	38	$\overline{DMS}$
5	D14	39	$\overline{BMS}$
6	D15	40	$\overline{BG}$
7	D16	41	XTAL
8	D17	42	CLKIN
9	D18	43	CLKOUT
10	GND	44	$\overline{WR}$
11	D19	45	$\overline{RD}$
12	D20	46	DT0
13	D21	47	TFS0
14	D22	48	RFS0
15	D23	49	GND
16	V_{DD}	50	DR0
17	MMAP	51	SCLK0
18	$\overline{BR}$	52	DT1
19	$\overline{IRQ2}$	53	TFS1
20	$\overline{RESET}$	54	RFS1
21	A0	55	DR1
22	A1	56	SCLK1
23	A2	57	V_{DD}
24	A3	58	D0
25	A4	59	D1
26	V_{DD}	60	D2
27	A5	61	D3
28	A6	62	D4
29	GND	63	D5
30	A7	64	D6
31	A8	65	D7
32	A9	66	D8
33	A10	67	D9
34	A11	68	D10

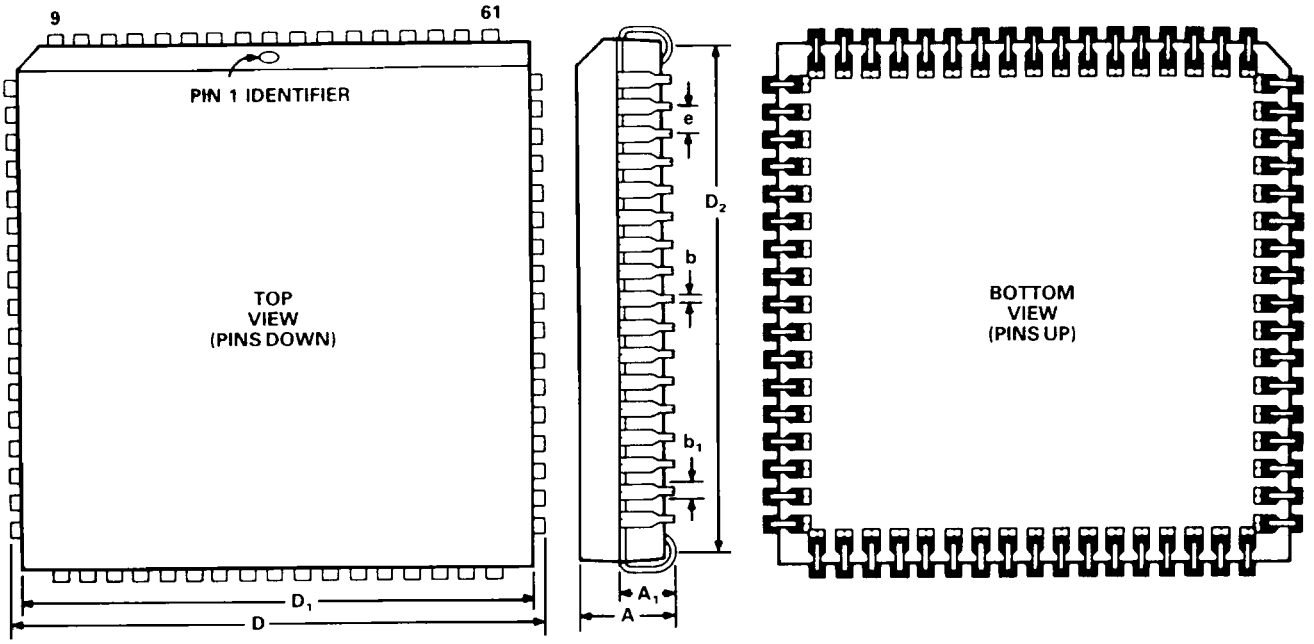
PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME
1	A5	41	NC
2	A6	42	NC
3	GND	43	NC
4	GND	44	D4
5	A7	45	D5
6	A8	46	D6
7	A9	47	D7
8	A10	48	D8
9	A11	49	D9
10	A12	50	D10
11	A13	51	D11
12	$\overline{PMS}$	52	GND
13	$\overline{DMS}$	53	GND
14	$\overline{BMS}$	54	D12
15	$\overline{BG}$	55	D13
16	XTAL	56	D14
17	CLKIN	57	D15
18	NC	58	D16
19	NC	59	D17
20	NC	60	D18
21	CLKOUT	61	GND
22	$\overline{WR}$	62	GND
23	$\overline{RD}$	63	D19
24	DT0	64	D20
25	TFS0	65	D21
26	RFS0	66	D22
27	GND	67	D23
28	GND	68	V_{DD}
29	DR0	69	V_{DD}
30	SCLK0	70	MMAP
31	DT1	71	$\overline{BR}$
32	TFS1	72	$\overline{IRQ2}$
33	RFS1	73	$\overline{RESET}$
34	DR1	74	A0
35	SCLK1	75	A1
36	V_{DD}	76	A2
37	D0	77	A3
38	D1	78	A4
39	D2	79	V_{DD}
40	D3	80	V_{DD}

68-Pin Grid Array



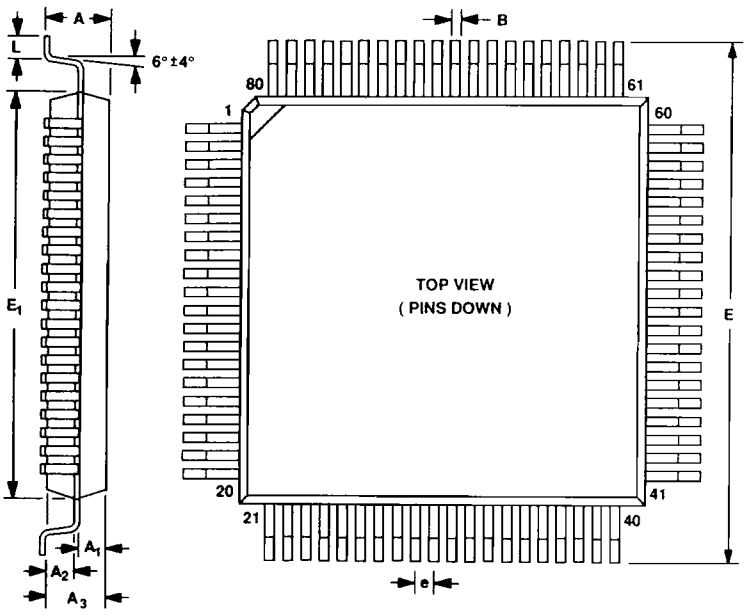
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.123	0.164	3.12	4.17
A_1	0.50 TYP		1.27 TYP	
ϕb	0.018 TYP		0.46 TYP	
ϕb_1	0.05 TYP		1.27 TYP	
D	1.086	1.110	27.58	28.19
e_1	0.988	1.012	25.10	25.70
e_2	0.788	0.812	20.02	20.62
e	0.100 TYP		2.54 TYP	
L_3	0.180 TYP		4.57 TYP	

68-Lead Plastic Leaded Chip Carrier



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.169	0.175	4.29	4.45
A_1	0.104 TYP		2.64 TYP	
b	0.017	0.019	0.43	0.48
b_1	0.027	0.029	0.69	0.74
D	0.885	0.995	22.48	25.27
D_1	0.950	0.954	24.13	24.23
D_2	0.895	0.925	22.73	23.50
e	0.050 TYP		1.27 TYP	

80-Lead Plastic Quad Flat Pack



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
E	0.67	0.68	0.69	16.95	17.2	17.45
B		0.012			0.30	
e		0.026			0.65	
E_1	0.547	0.551	0.555	13.90	14.0	14.10
A_3		0.079			2.0	
A			0.965			2.45
L	0.026	0.031	0.037	0.65	0.8	0.95
A_1	0.033	0.036	0.039	0.85	0.925	1.0
A_2	0.033	0.036	0.039	0.85	0.925	1.0

ORDERING GUIDE

Part Number*	Ambient Temperature Range	Instruction Rate (MHz)	Package
ADSP-2101KG-40	0°C to +70°C	10.24	68-Pin Grid Array
ADSP-2101KG-50	0°C to +70°C	12.5	68-Pin Grid Array
ADSP-2101KG-66	0°C to +70°C	16.67	68-Pin Grid Array
ADSP-2101KP-40	0°C to +70°C	10.24	68-Lead PLCC
ADSP-2101KP-50	0°C to +70°C	12.5	68-Lead PLCC
ADSP-2101KP-66	0°C to +70°C	16.67	68-Lead PLCC
ADSP-2101KS-40	0°C to +70°C	10.24	80-Lead PQFP
ADSP-2101KS-50	0°C to +70°C	12.5	80-Lead PQFP
ADSP-2101KS-66	0°C to +70°C	16.67	80-Lead PQFP
ADSP-2101BG-40	−40°C to +85°C	10.24	68-Pin Grid Array
ADSP-2101BG-50	−40°C to +85°C	12.5	68-Pin Grid Array
ADSP-2101BG-66	−40°C to +85°C	16.67	68-Pin Grid Array
ADSP-2101BP-40	−40°C to +85°C	10.24	68-Lead PLCC
ADSP-2101BP-50	−40°C to +85°C	12.5	68-Lead PLCC
ADSP-2101BP-66	−40°C to +85°C	16.67	68-Lead PLCC
ADSP-2101BS-40	−40°C to +85°C	10.24	80-Lead PQFP
ADSP-2101BS-50	−40°C to +85°C	12.5	80-Lead PQFP
ADSP-2101BS-66	−40°C to +85°C	16.67	80-Lead PQFP
ADSP-2101TG-40	−55°C to +125°C	10.24	68-Pin Grid Array
ADSP-2101TG/883B-40	−55°C to +125°C	10.24	68-Pin Grid Array
ADSP-2101TG-50	−55°C to +125°C	12.5	68-Pin Grid Array
ADSP-2101TG/883B-50	−55°C to +125°C	12.5	68-Pin Grid Array

*G = Ceramic Pin Grid Array; P = Plastic Leaded Chip Carrier; S = Plastic Quad Flat Pack.