16-Lane 4-Port Gen2 PCI Express® Switch

89HPES16T4BG2
Data Sheet

Device Overview

The 89HPES16T4BG2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES16T4BG2 is a 16-lane, 4-port Gen2 peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to three downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Sixteen 5 Gbps Gen2 PCI Express lanes*
  - *Four switch ports*
    - *One x4 upstream port*
    - *Three x4 downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 2.0 compliant*
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
    - *ARI ECN*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic per port link width negotiation to x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion*
  - *Ability to load device configuration from serial EEPROM*
- On-Die Temperature Sensor
  - *Range of 0 to 127.5 degrees Celsius*
  - *Three programmable temperature thresholds with over and under temperature threshold alarms*
  - *Automatic recording of maximum high or minimum low temperature*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Incorporates on-chip internal memory for packet buffering and queueing*

Block Diagram

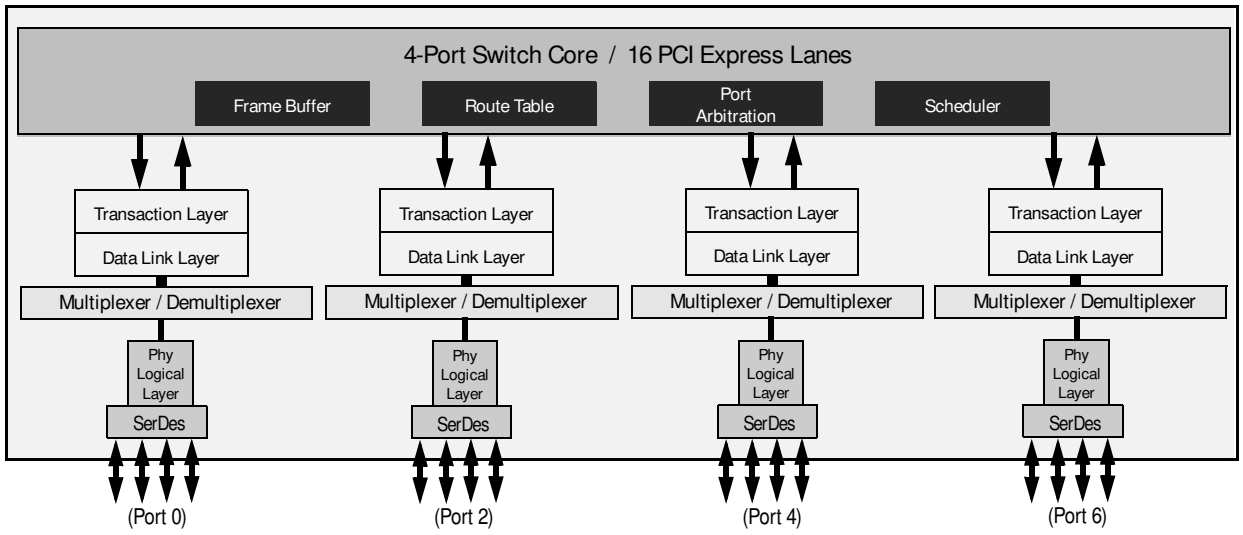


Figure 1 Internal Block Diagram

- *Integrates sixteen 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)*
  - *Receive equalization (RxEQ)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Support PCI Express Power Management Interface specification (PCI-PM 1.2)*
  - *Supports PCI Express Active State Power Management (ASPM) link state*
  - *Supports PCI Express Power Budgeting Capability*
  - *Supports the optional PCI Express SerDes Transmit Low-Swing Voltage Mode*
  - *Unused SerDes are disabled and can be powered-off*
- Testability and Debug Features
  - *Supports IEEE 1149.1 JTAG and IEEE 1149.6 AC JTAG*
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*
- Sixteen General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- Packaged in a 23mm x 23mm, 288-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES16T4BG2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 16 GBps (128 Gbps) of aggregated, full-duplex switching capacity through 16 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES16T4BG2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES16T4BG2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

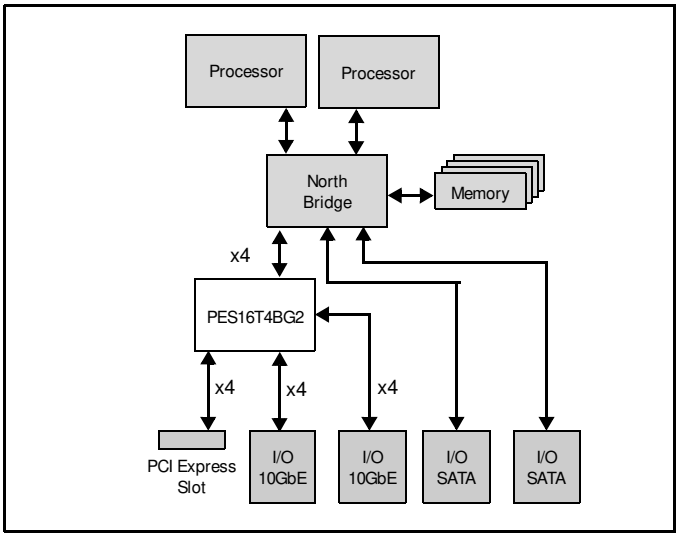


Figure 2 I/O Expansion Application

SMBus Interface

The PES16T4BG2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES16T4BG2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES16T4BG2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]

Table 1 Master and Slave SMBus Address Assignment

Bit	Slave SMBus Address	Master SMBus Address
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES16T4BG2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES16T4BG2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES16T4BG2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES16T4BG2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

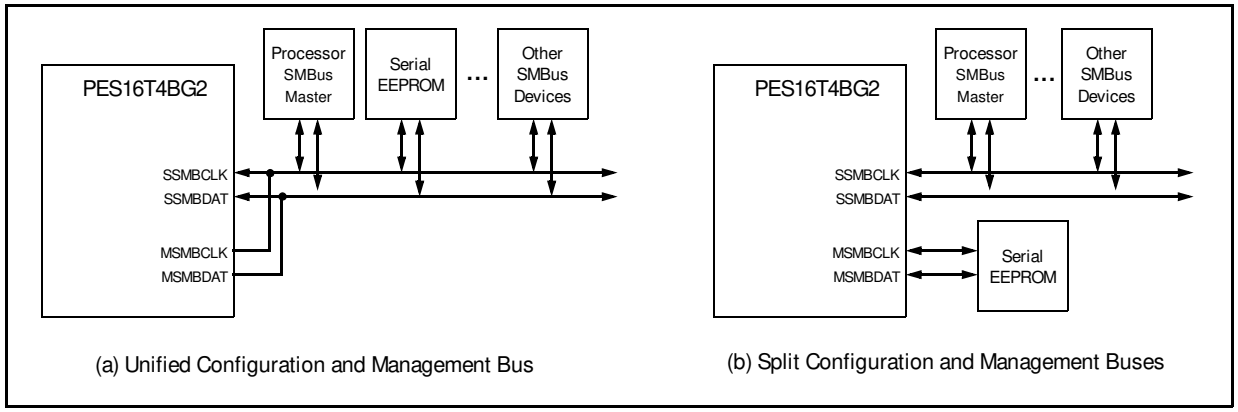


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES16T4BG2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES16T4BG2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES16T4BG2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES16T4BG2. In response to an I/O expander interrupt, the PES16T4BG2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES16T4BG2 provides 16 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES16T4BG2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES16T4BG2, the three downstream ports are labeled port 2, port 4, and port 6.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE2RP[3:0] PE2RN[3:0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2.
PE4RP[3:0] PE4RN[3:0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4.
PE6RP[3:0] PE6RN[3:0]	I	PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pairs for port 6.
PE6TP[3:0] PE6TN[3:0]	O	PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pairs for port 6.
PEREFCLKP[0] PEREFCLKN[0]	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz This pin should be static and not change following the negation of PERSTN.

Table 2 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.

Table 3 SMBus Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
SSMBADDR[5,3:1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O expander interrupt 0 input.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6.
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[15]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register.
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside PES16T4BG2 and initiates a PCI Express fundamental reset.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES16T4BG2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	Switch Mode. These configuration pins determine the PES16T4BG2 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN.

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode.** The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset.** This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
REFRES0	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES2	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES4	I/O	**Port 4 External Reference Resistor.** Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES6	I/O	**Port 6 External Reference Resistor.** Provides a reference for the Port 6 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the PES16T4BG2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PEREFCLKN[0]	I	HCSL	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[15:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I		Input	pull-up	
	MSMBSMODE	I		Input	pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[2:0]	I		Input	pull-down	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES0	I/O	Analog			
	REFRES2	I/O				
	REFRES4	I/O				
	REFRES6	I/O				

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.

2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

3. Schmitt Trigger Input (STI).

Logic Diagram — PES16T4BG2

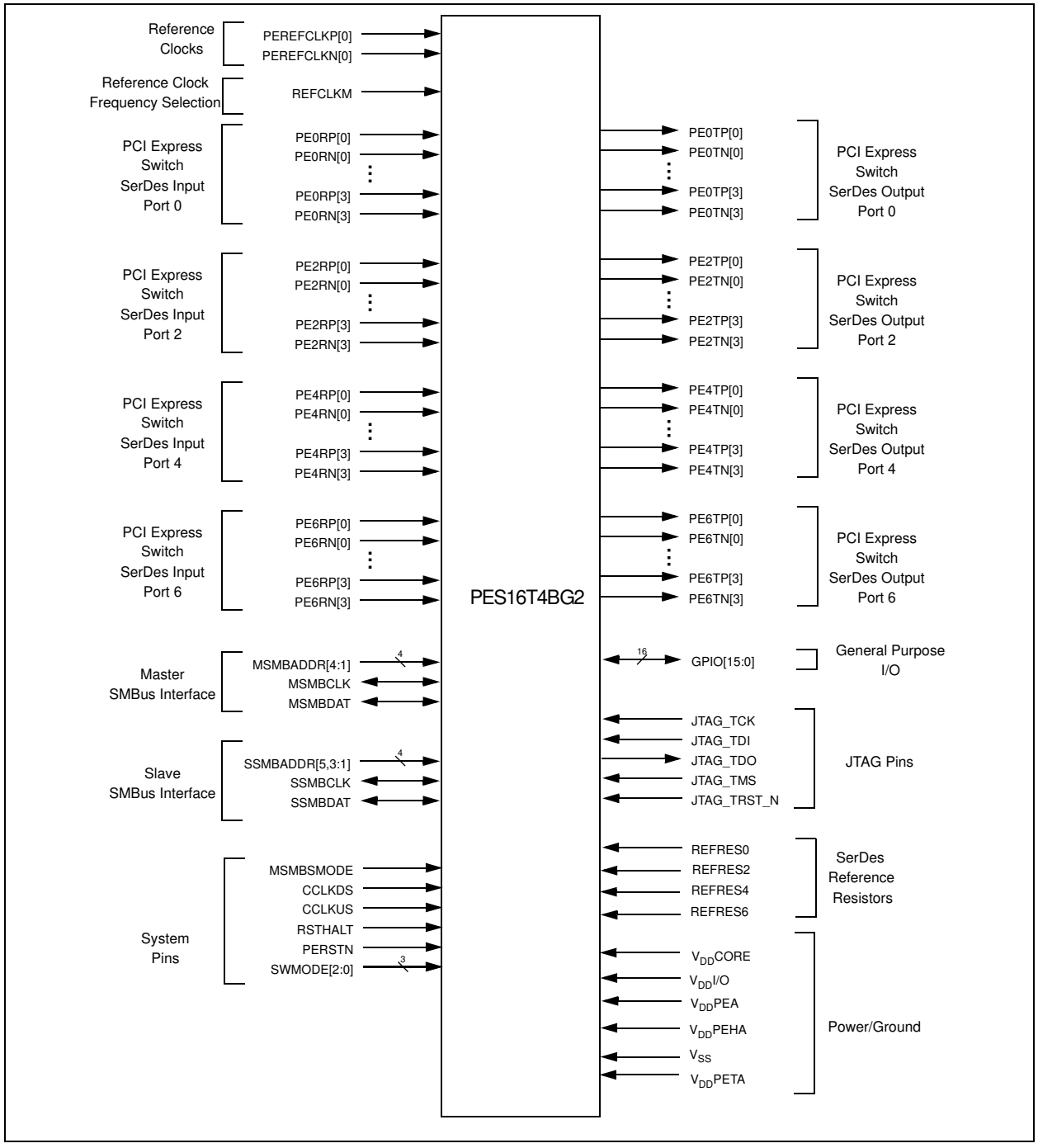


Figure 4 PES16T4BG2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[15:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

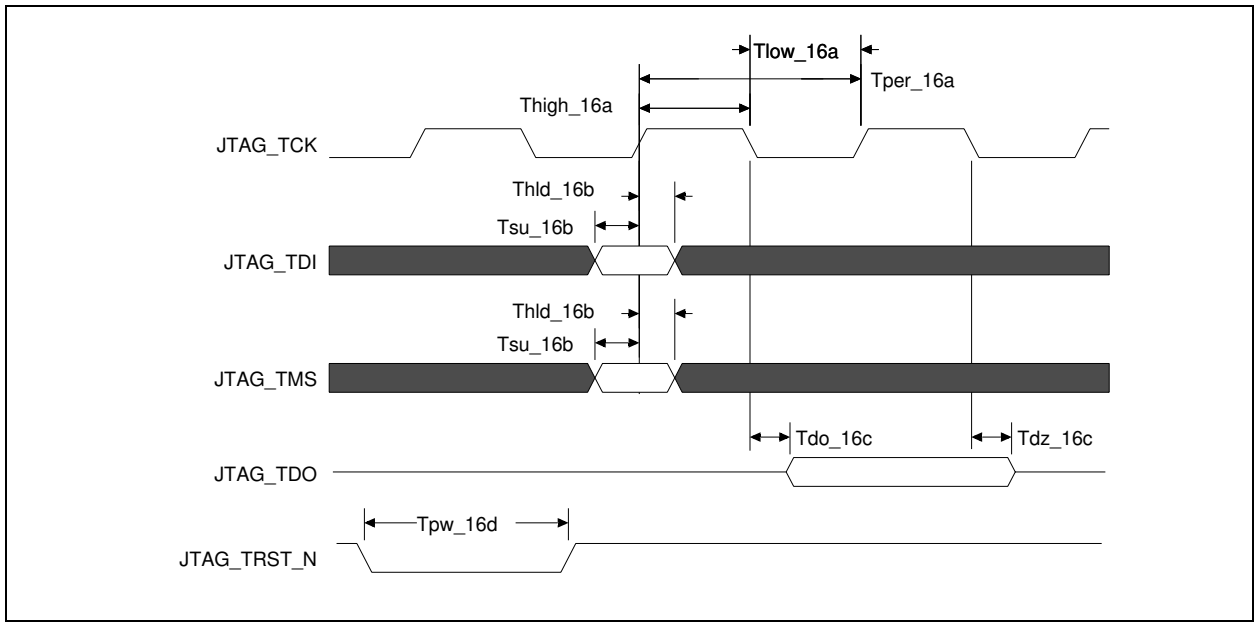


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES16T4BG2 Operating Voltages

1. V_{DD}PEA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 14 PES24T3G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 15 PES16T4BG2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
4/4/4/4 (Full swing)	mA	700	968	750	880	260	330	361	429	3	4		
	Watts	0.70	1.06	0.75	1.0	0.65	0.91	0.36	0.47	0.01	0.02	2.47	3.46
4/4/1/1 (Full swing)	mA	550	720	540	660	150	220	160	165	3	4		
	Watts	0.55	0.79	0.54	0.73	0.38	0.61	0.16	0.18	0.01	0.02	1.64	2.33

Table 16 PES16T4BG2 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES16T4BG2 (23mm^2 SBGA288 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES16T4BG2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	19.8	°C/W	Zero air flow
		13.3	°C/W	1 m/S air flow
		11.8	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	9.5	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	1.1	°C/W	
P	Power Dissipation of the Device	3.24	Watts	Maximum

Table 17 Thermal Specifications for PES16T4BG2, 23x23 mm SBGA288 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detec-tion			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Package Pinout — 288-BGA Signal Pinout for PES16T4BG2

The following table lists the pin numbers and signal names for the PES16T4BG2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B13	V_{DD}PEHA		D3	PE2TP00		F21	GPIO_06	
A2	V_{SS}		B14	V_{SS}		D4	V_{DD}PETA		F22	PE4RN03	
A3	V_{DD}I/O		B15	V_{SS}		D5	V_{DD}PEA		G1	V_{DD}CORE	
A4	V_{DD}CORE		B16	V_{DD}PEHA		D6	V_{SS}		G2	V_{DD}PEHA	
A5	PE6RP03		B17	V_{SS}		D7	V_{DD}PETA		G3	PE2TP01	
A6	PE6RN03		B18	V_{SS}		D8	V_{DD}PEA		G4	V_{DD}PEA	
A7	V_{DD}CORE		B19	V_{SS}		D9	V_{SS}		G19	V_{DD}PETA	
A8	PE6RP02		B20	REFCLKM		D10	V_{DD}PETA		G20	PE4TP03	
A9	PE6RN02		B21	GPIO_13		D11	V_{DD}PEA		G21	GPIO_05	
A10	V_{DD}CORE		B22	V_{SS}		D12	V_{SS}		G22	V_{SS}	
A11	V_{SS}		C1	SSMBCLK		D13	V_{DD}PEA		H1	PE2RN01	
A12	V_{SS}		C2	SSMBDAT		D14	V_{SS}		H2	V_{SS}	
A13	V_{DD}CORE		C3	MSMBSMODE		D15	V_{DD}PETA		H3	PE2TN01	
A14	PE6RP01		C4	MSMBDAT		D16	V_{DD}PEA		H4	V_{DD}PETA	
A15	PE6RN01		C5	MSMBADDR_4		D17	V_{SS}		H19	V_{DD}PEA	
A16	V_{DD}CORE		C6	PE6TN03		D18	V_{DD}CORE		H20	V_{DD}I/O	
A17	PE6RP00		C7	PE6TP03		D19	V_{DD}PETA		H21	GPIO_04	1
A18	PE6RN00		C8	V_{DD}I/O		D20	GPIO_09		H22	PE4RP02	
A19	V_{DD}I/O		C9	PE6TN02		D21	GPIO_11	1	J1	PE2RP01	
A20	GPIO_15		C10	PE6TP02		D22	V_{DD}CORE		J2	V_{SS}	
A21	GPIO_14		C11	V_{SS}		E1	PE2RN00		J3	V_{SS}	
A22	V_{SS}		C12	V_{DD}PEHA		E2	V_{SS}		J4	V_{SS}	
B1	SSMBADDR_5		C13	V_{SS}		E3	PE2TN00		J19	V_{SS}	
B2	SSMBADDR_3		C14	V_{SS}		E4	V_{DD}CORE		J20	PE4TN02	
B3	SSMBADDR_2		C15	PE6TN01		E19	V_{DD}PEA		J21	V_{DD}PEHA	
B4	SSMBADDR_1		C16	PE6TP01		E20	GPIO_07	1	J22	PE4RN02	
B5	MSMBCLK		C17	V_{DD}PEHA		E21	GPIO_08		K1	V_{DD}CORE	
B6	MSMBADDR_3		C18	PE6TN00		E22	PE4RP03		K2	V_{DD}PEHA	
B7	MSMBADDR_2		C19	PE6TP00		F1	PE2RP00		K3	V_{SS}	
B8	MSMBADDR_1		C20	GPIO_10		F2	V_{SS}		K4	V_{DD}PEA	
B9	V_{DD}PEHA		C21	GPIO_12		F3	V_{DD}PEHA		K19	V_{DD}PETA	
B10	NC		C22	V_{DD}I/O		F4	V_{SS}		K20	PE4TP02	
B11	REFRES6		D1	V_{SS}		F19	V_{SS}		K21	NC	
B12	V_{SS}		D2	V_{DD}I/O		F20	PE4TN03		K22	V_{DD}CORE	

Table 19 PES16T4BG2 288-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
L1	V_{SS}		R21	V_{SS}		W13	V_{DD}PETA		AA7	V_{DD}PEHA	
L2	V_{SS}		R22	PE4RN01		W14	V_{SS}		AA8	V_{SS}	
L3	V_{DD}PEHA		T1	V_{DD}CORE		W15	V_{DD}PEA		AA9	V_{SS}	
L4	V_{SS}		T2	JTAG_TRST_N		W16	V_{DD}PETA		AA10	V_{DD}PEHA	
L19	V_{DD}PEA		T3	PE2TP03		W17	V_{SS}		AA11	V_{SS}	
L20	V_{SS}		T4	JTAG_TDO		W18	V_{DD}PEA		AA12	REFRES0	
L21	REFRES4		T19	V_{DD}PEA		W19	V_{DD}PETA		AA13	NC	
L22	V_{SS}		T20	PE4TP01		W20	PE4TP00		AA14	V_{DD}PEHA	
M1	V_{SS}		T21	V_{DD}PEHA		W21	V_{DD}I/O		AA15	CCLKUS	
M2	REFRES2		T22	V_{DD}CORE		W22	V_{SS}		AA16	CCLKDS	
M3	V_{SS}		U1	PE2RN03		Y1	JTAG_TDI		AA17	SWMODE_0	
M4	V_{DD}PEA		U2	JTAG_TMS		Y2	V_{DD}I/O		AA18	SWMODE_2	
M19	V_{SS}		U3	PE2TN03		Y3	V_{DD}I/O		AA19	NC	
M20	V_{DD}PEHA		U4	V_{SS}		Y4	PE0TP00		AA20	NC	
M21	V_{SS}		U19	V_{SS}		Y5	PE0TN00		AA21	GPIO_00	1
M22	V_{SS}		U20	V_{DD}PEHA		Y6	V_{DD}PEHA		AA22	GPIO_01	1
N1	V_{DD}CORE		U21	V_{SS}		Y7	PE0TP01		AB1	V_{SS}	
N2	NC		U22	PE4RP00		Y8	PE0TN01		AB2	V_{SS}	
N3	PE2TP02		V1	PE2RP03		Y9	V_{SS}		AB3	V_{SS}	
N4	V_{DD}PETA		V2	V_{SS}		Y10	V_{SS}		AB4	V_{DD}CORE	
N19	V_{DD}PEA		V3	V_{SS}		Y11	V_{DD}PEHA		AB5	PE0RN00	
N20	V_{SS}		V4	V_{DD}PEA		Y12	V_{SS}		AB6	PE0RP00	
N21	V_{DD}PEHA		V19	V_{DD}CORE		Y13	PE0TP02		AB7	V_{DD}CORE	
N22	V_{DD}CORE		V20	PE4TN00		Y14	PE0TN02		AB8	PE0RN01	
P1	PE2RN02		V21	V_{SS}		Y15	V_{DD}I/O		AB9	PE0RP01	
P2	V_{DD}PEHA		V22	PE4RN00		Y16	PE0TP03		AB10	V_{DD}CORE	
P3	PE2TN02		W1	JTAG_TCK		Y17	PE0TN03		AB11	PEREFCLKP0	
P4	V_{SS}		W2	V_{SS}		Y18	SWMODE_1		AB12	PEREFCLKN0	
P19	V_{SS}		W3	V_{SS}		Y19	PERSTN		AB13	V_{DD}CORE	
P20	V_{SS}		W4	V_{DD}PETA		Y20	RSTHALT		AB14	PE0RN02	
P21	V_{SS}		W5	V_{DD}CORE		Y21	GPIO_03		AB15	PE0RP02	
P22	PE4RP01		W6	V_{SS}		Y22	GPIO_02	1	AB16	V_{DD}CORE	
R1	PE2RP02		W7	V_{DD}PEA		AA1	V_{SS}		AB17	PE0RN03	
R2	V_{DD}I/O		W8	V_{DD}PETA		AA2	V_{SS}		AB18	PE0RP03	
R3	V_{DD}PETA		W9	V_{SS}		AA3	V_{SS}		AB19	V_{SS}	
R4	V_{DD}PEA		W10	V_{DD}PEA		AA4	V_{SS}		AB20	V_{DD}I/O	
R19	V_{DD}PETA		W11	V_{SS}		AA5	V_{SS}		AB21	V_{SS}	

Table 19 PES16T4BG2 288-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
R20	PE4TN01		W12	V_{DD}PEA		AA6	V_{SS}		AB22	V_{SS}	

Table 19 PES16T4BG2 288-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
AA21	GPIO_00	P2RSTN
AA22	GPIO_01	P4RSTN
Y22	GPIO_02	IOEXPINTN0
H21	GPIO_04	IOEXPINTN2
E20	GPIO_07	GPEN
D21	GPIO_11	P6RSTN

Table 20 PES16T4BG2 Alternate Signal Functions

No Connection Pins

NC Pins
B10
K21
N2
AA13
AA19
AA20

Table 21 PES16T4BG2 No Connection Pins

Power Pins

V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEHA	V_{DD}PETA
A4	A3	D5	B9	D4
A7	A19	D8	B13	D7
A10	C8	D11	B16	D10
A13	C22	D13	C12	D15
A16	D2	D16	C17	D19
D18	H20	E19	F3	G19
D22	R2	G4	G2	H4
E4	W21	H19	J21	K19
G1	Y2	K4	K2	N4
K1	Y3	L19	L3	R3
K22	Y15	M4	M20	R19
N1	AB20	N19	N21	W4
N22		R4	P2	W8
T1		T19	T21	W13
T22		V4	U20	W16
V19		W7	Y6	W19
W5		W10	Y11	
AB4		W12	AA7	
AB7		W15	AA10	
AB10		W18	AA14	
AB13				
AB16				

Table 22 PES16T4BG2 Power Pins

Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}
A1	D17	M21	W17
A2	E2	M22	W22
A11	F2	N20	Y9
A12	F4	P4	Y10
A22	F19	P19	Y12
B12	G22	P20	AA1
B14	H2	P21	AA2
B15	J2	R21	AA3
B17	J3	U4	AA4
B18	J4	U19	AA5
B19	J19	U21	AA6
B22	K3	V2	AA8
C11	L1	V3	AA9
C13	L2	V21	AA11
C14	L4	W2	AB1
D1	L20	W3	AB2
D6	L22	W6	AB3
D9	M1	W9	AB19
D12	M3	W11	AB21
D14	M19	W14	AB22

Table 23 PES16T4BG2 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	AA16	System
CCLKUS	I	AA15	
GPIO_00	I/O	AA21	General Purpose Input/Output
GPIO_01	I/O	AA22	
GPIO_02	I/O	Y22	
GPIO_03	I/O	Y21	
GPIO_04	I/O	H21	
GPIO_05	I/O	G21	
GPIO_06	I/O	F21	
GPIO_07	I/O	E20	
GPIO_08	I/O	E21	
GPIO_09	I/O	D20	
GPIO_10	I/O	C20	
GPIO_11	I/O	D21	
GPIO_12	I/O	C21	
GPIO_13	I/O	B21	
GPIO_14	I/O	A21	
GPIO_15	I/O	A20	
JTAG_TCK	I	W1	JTAG
JTAG_TDI	I	Y1	
JTAG_TDO	O	T4	
JTAG_TMS	I	U2	
JTAG_TRST_N	I	T2	
MSMBADDR_1	I	B8	SMBus
MSMBADDR_2	I	B7	
MSMBADDR_3	I	B6	
MSMBADDR_4	I	C5	
MSMBCLK	I/O	B5	
MSMBDAT	I/O	C4	
MSMBSMODE	I	C3	System
No Connection	See Table 21		

Table 24 89PES16T4BG2 Alphabetical Signal List (Part 1 of 5)

Signal Name	I/O Type	Location	Signal Category
PE0RN00	I	AB5	PCI Express
PE0RN01	I	AB8	
PE0RN02	I	AB14	

Table 24 89PES16T4BG2 Alphabetical Signal List (Part 2 of 5)

Signal Name	I/O Type	Location	Signal Category
PE0RN03	I	AB17	PCI Express (Cont.)
PE0RP00	I	AB6	
PE0RP01	I	AB9	
PE0RP02	I	AB15	
PE0RP03	I	AB18	
PE0TN00	O	Y5	
PE0TN01	O	Y8	
PE0TN02	O	Y14	
PE0TN03	O	Y17	
PE0TP00	O	Y4	
PE0TP01	O	Y7	
PE0TP02	O	Y13	
PE0TP03	O	Y16	
PE2RN00	I	E1	
PE2RN01	I	H1	
PE2RN02	I	P1	
PE2RN03	I	U1	
PE2RP00	I	F1	
PE2RP01	I	J1	
PE2RP02	I	R1	
PE2RP03	I	V1	
PE2TN00	O	E3	
PE2TN01	O	H3	
PE2TN02	O	P3	
PE2TN03	O	U3	
PE2TP00	O	D3	
PE2TP01	O	G3	
PE2TP02	O	N3	
PE2TP03	O	T3	
PE4RN00	I	V22	
PE4RN01	I	R22	
PE4RN02	I	J22	
PE4RN03	I	F22	
PE4RP00	I	U22	
PE4RP01	I	P22	
PE4RP02	I	H22	

Table 24 89PES16T4BG2 Alphabetical Signal List (Part 3 of 5)

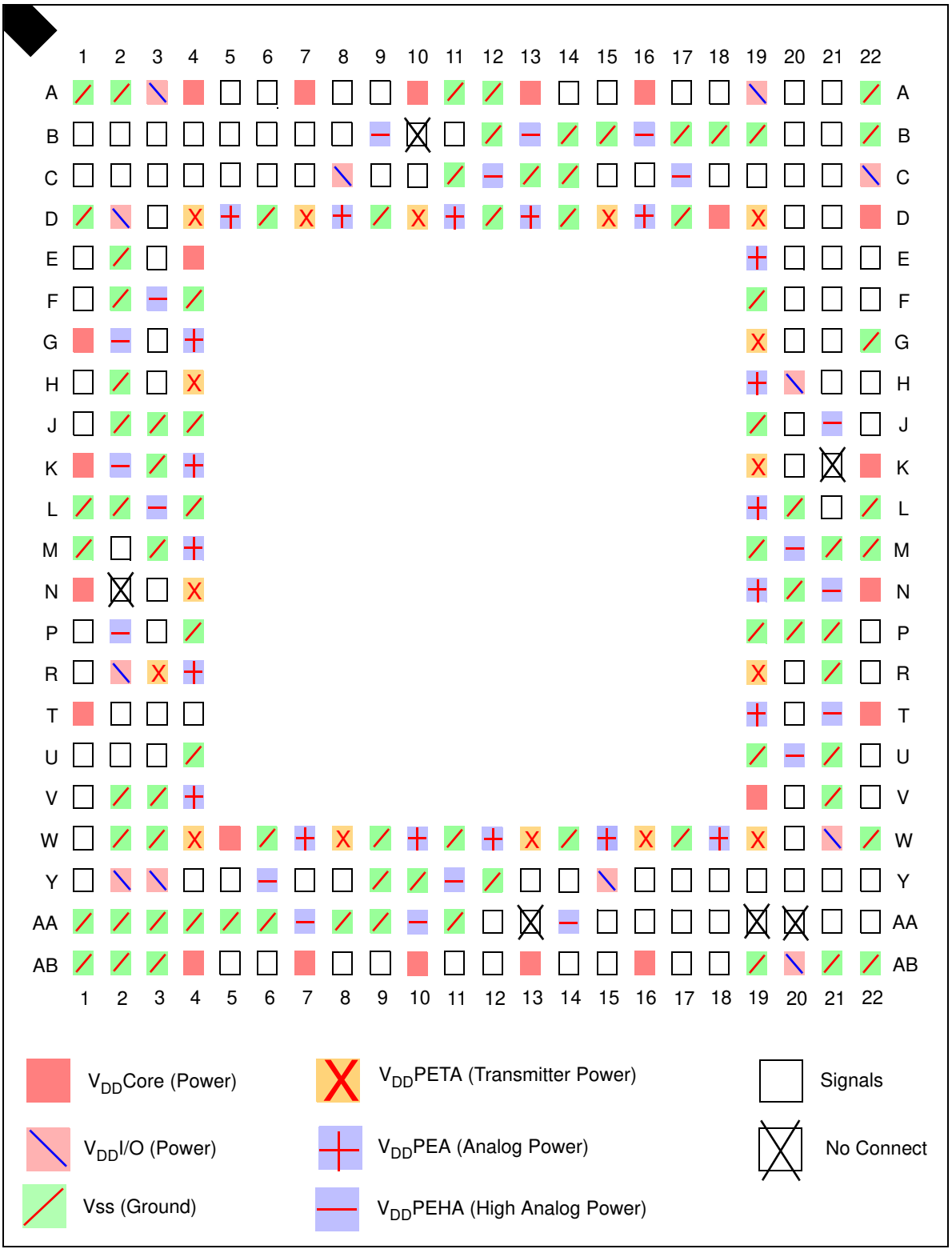
Signal Name	I/O Type	Location	Signal Category
PE4RP03	I	E22	PCI Express (Cont.)
PE4TN00	O	V20	
PE4TN01	O	R20	
PE4TN02	O	J20	
PE4TN03	O	F20	
PE4TP00	O	W20	
PE4TP01	O	T20	
PE4TP02	O	K20	
PE4TP03	O	G20	
PE6RN00	I	A18	
PE6RN01	I	A15	
PE6RN02	I	A9	
PE6RN03	I	A6	
PE6RP00	I	A17	
PE6RP01	I	A14	
PE6RP02	I	A8	
PE6RP03	I	A5	
PE6TN00	O	C18	
PE6TN01	O	C15	
PE6TN02	O	C9	
PE6TN03	O	C6	
PE6TP00	O	C19	
PE6TP01	O	C16	
PE6TP02	O	C10	
PE6TP03	O	C7	
PEREFCLKN0	I	AB12	
PEREFCLKP0	I	AB11	
PERSTN	I	Y19	System
REFCLKM	I	B20	PCI Express
REFRES0	I/O	AA12	SerDes Reference Resistors
REFRES2	I/O	M2	
REFRES4	I/O	L21	
REFRES6	I/O	B11	
RSTHALT	I	Y20	System

Table 24 89PES16T4BG2 Alphabetical Signal List (Part 4 of 5)

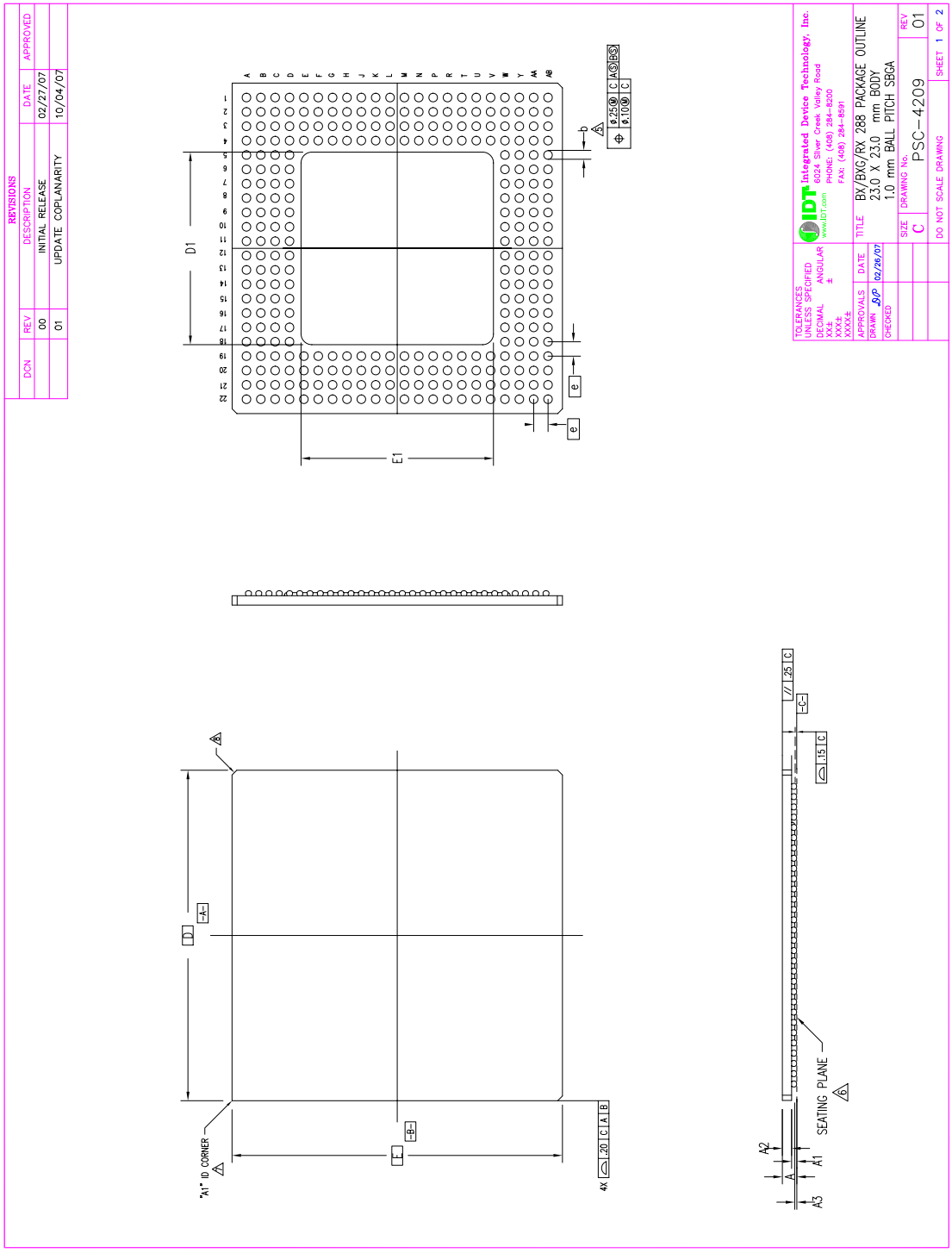
Signal Name	I/O Type	Location	Signal Category
SSMBADDR_1	I	B4	SMBus
SSMBADDR_2	I	B3	
SSMBADDR_3	I	B2	
SSMBADDR_5	I	B1	
SSMBCLK	I/O	C1	SMBus
SSMBDAT	I/O	C2	
SWMODE_0	I	AA17	System
SWMODE_1	I	Y18	
SWMODE_2	I	AA18	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Table 22 for a listing of power pins.		
V_{SS}	See Table 23 for a listing of ground pins.		

Table 24 89PES16T4BG2 Alphabetical Signal List (Part 5 of 5)

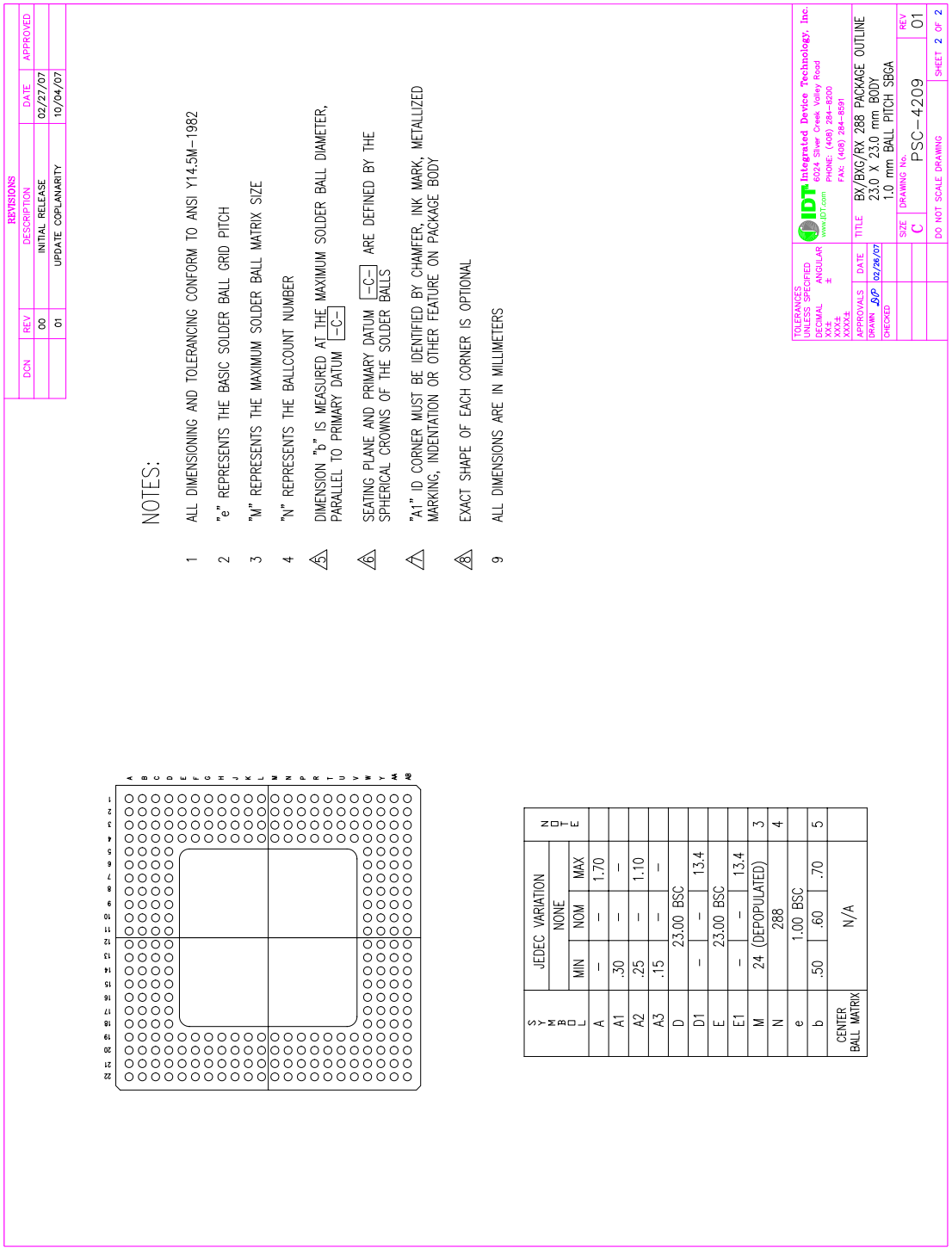
PES16T4BG2 Pinout — Top View



PES16T4BG2 Package Drawing — 288-Pin BX288/BXG288



PES16T4BG2 Package Drawing — Page Two



Revision History

July 1, 2009: Initial publication of Advance data sheet.

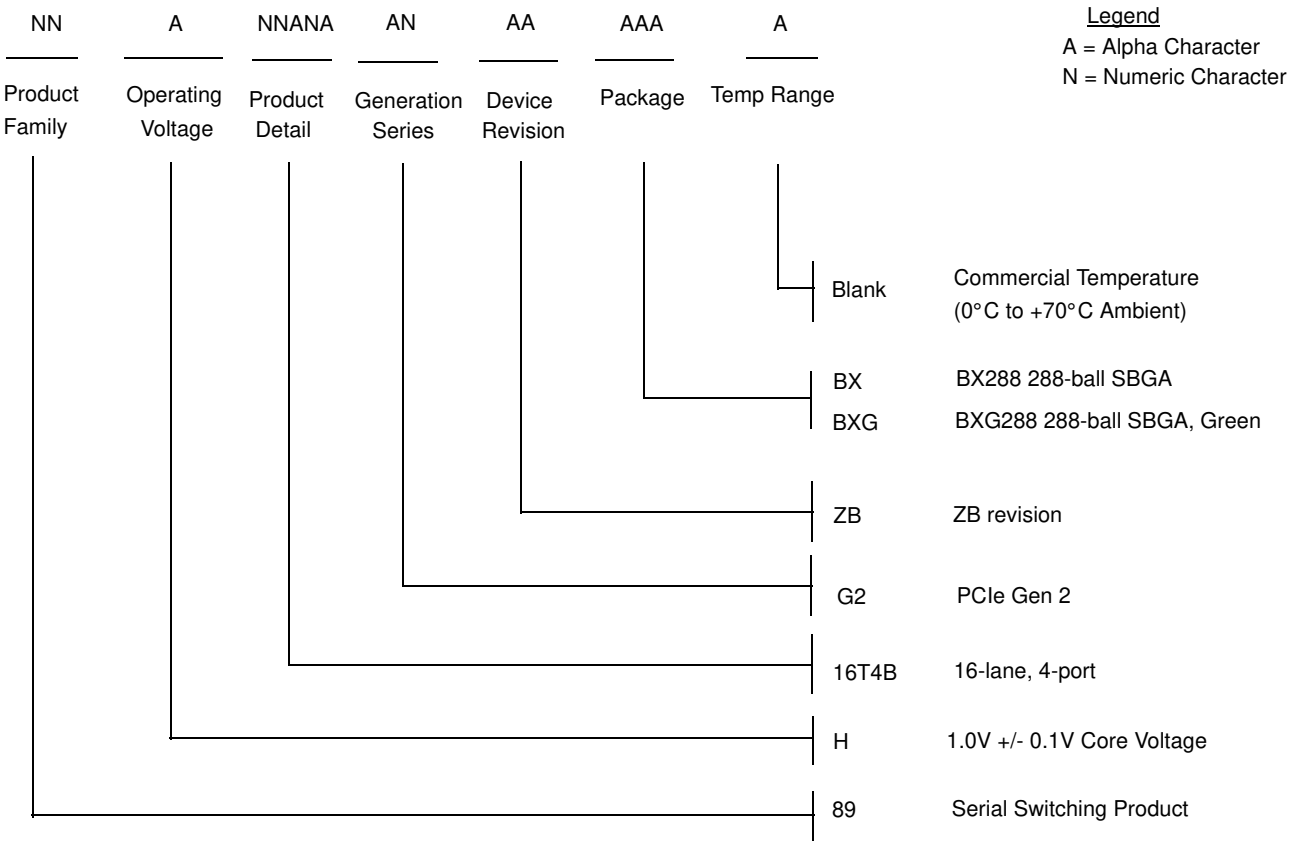
July 29, 2009: In Features section, added new bullet “Implements the following optional PCI Express features.”

January 18, 2010: Revised Power Management list in Features section.

February 2, 2010: Added new section Absolute Maximum Voltage Rating with table. Replaced ZA with ZB silicon in the Ordering Information section.

September 13, 2010: In Table 8, changed Buffer type for PCI Express from CML to PCIe differential and changed reference clocks to HCSL.

Ordering Information



Valid Combinations

89H16T4BG2ZBBX	288-ball SBGA package, Commercial Temperature
89H16T4BG2ZBBXG	288-ball Green SBGA package, Commercial Temperature

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