Click here for production status of specific part numbers.

MAX17498A/ MAX17498B/ MAX17498C

AC-DC and DC-DC Peak Current-Mode Converters for Flyback/Boost Applications

General Description

The MAX17498A/MAX17498B/MAX17498C devices are current-mode fixed-frequency flyback/boost converters with a minimum number of external components. They contain all the control circuitry required to design wide input voltage isolated and nonisolated power supplies. The MAX17498A has its rising/falling undervoltage lockout (UVLO) thresholds optimized for universal offline (85V AC to 265V AC) applications, while the MAX17498B/MAX17498C support UVLO thresholds suitable to low-voltage DC-DC applications.

The switching frequency of the MAX17498A/MAX17498C is 250kHz, while that of the MAX17498B is 500kHz. These frequencies allow the use of tiny magnetic and filter components, resulting in compact, cost-effective power supplies. An EN/UVLO input allows the user to start the power supply precisely at the desired input voltage, while also functioning as an on/off pin. The OVI pin enables implementation of an input overvoltage-protection scheme that ensures that the converter shuts down when the DC input voltage exceeds the desired maximum value.

The devices incorporate a flexible error amplifier and an accurate reference voltage (REF) to enable the end user to regulate both positive and negative outputs. Programmable current limit allows proper sizing and protection of the primary switching FET. The devices support a maximum duty cycle greater than 92% and provide programmable slope compensation to allow optimization of control loop performance. The devices provide an open-drain PGOOD pin that serves as a power-good indicator and enters the high-impedance state to indicate that the flyback/boost converter is in regulation. An SS pin allows programmable soft-start time for the flyback/boost converter. Hiccup-mode overcurrent protection and thermal shutdown are provided to minimize dissipation under overcurrent and overtemperature fault conditions. The devices are available in a space-saving, 16-pin (3mm x 3mm) TQFN package with 0.5mm lead spacing.

Benefits and Features

- Peak Current-Mode Converter
- Current-Mode Control Provides Excellent Transient Response
- Fixed Switching Frequency
  - 250kHz: MAX17498A/MAX17498C
  - 500kHz: MAX17498B
- Flexible Error Amplifier to Regulate Both Positive and Negative Outputs
- Programmable Voltage or Current Soft-Start
- Power-Good Signal (PGOOD)
- Reduced Power Dissipation Under Fault
  - Overcurrent Protection
  - Thermal Shutdown with Hysteresis
- Robust Protection Features
  - Programmable Current Limit
  - Input Overvoltage Protection
- Optimized Loop Performance
  - Fixed Default Slope Compensation in Current Soft-Start
  - Fixed Default and Programmable Slope Compensation in Voltage Soft-Start
- High Efficiency
  - Low R_{DSON}, 175mΩ, 65V Rated Internal n-Channel MOSFET
  - No Current-Sense Resistor
- Optional Spread Spectrum
- Space-Saving, 16-Pin (3mm x 3mm) TQFN Package

Applications

- Front-End AC-DC Power Supplies for Industrial Applications (Isolated and Nonisolated)
- Telecom Power Supplies
- Wide Input Range DC Input Flyback/Boost Industrial Power Supplies

***Ordering Information* and *Typical Application Circuits* appear at end of data sheet.**

19-6043; Rev 4; 10/20

maxim integrated™

Absolute Maximum Ratings

IN to SGND .....-0.3V to +40V
EN/UVLO to SGND .....-0.3V to IN + 0.3V
OVI to SGND.....-0.3V to V_{CC} + 0.3V
V_{CC} to SGND .....-0.3V to +6V
SS, LIM, EA-, EA+, COMP, SLOPE,
REF to SGND.....-0.3V to (V_{CC} + 0.3V)
LX to SGND.....-0.3V to +70V
PGOOD to SGND.....-0.3V to +6V
PGND to SGND.....-0.3V to +0.3V
Continuous Power Dissipation (Single-Layer Board)
TQFN (derate 20.8mW/°C above +70°C).....1700mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +160°C
Junction Temperature (continuous).....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 TQFN	
Package Code	T1633+5
Outline Number	**21-0136**
Land Pattern Number	**90-0032**

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})					
IN Voltage Range (V_{IN})	MAX17498A	4.5		29	V
	MAX17498B/MAX17498C	4.5		36	
IN Supply Startup Current Under UVLO	$I_{INSTARTUP}$, V_{IN} < UVLO or EN/UVLO = SGND		22	36	µA
IN Supply Current (I_{IN})	Switching, f_{SW} = 250kHz (MAX17498A/MAX17498C)		1.8	3	mA
	Switching, f_{SW} = 500kHz (MAX17498B)		2	3.25	
IN Boostrap UVLO Rising Threshold	MAX17498A	19	20.5	22	V
	MAX17498B/MAX17498C	3.85	4.15	4.4	
IN Bootstrap UVLO Falling Threshold		3.65	3.95	4.25	V
IN Clamp Voltage	EN/UVLO = SGND, I_{IN} = 1mA (MAX17498A) (Note 2)	31	33.5	36	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (V_{CC})					
V_{CC} Output Voltage Range	6V < V_{IN} < 29V, 0mA < I_{VCC} < 50mA	4.8	5	5.2	V
V_{CC} Dropout Voltage	V_{IN} = 4.5V, I_{VCC} = 20mA		160	300	mV
V_{CC} Current Limit	V_{CC} = 0V, V_{IN} = 6V	50	100		mA
ENABLE (EN/UVLO)					
EN/UVLO Threshold	Rising	1.18	1.23	1.28	V
	Falling	1.11	1.17	1.21	
EN/UVLO Input Leakage Current	0V < $V_{EN/UVLO}$ < 1.5V, T_A = +25°C	-100	0	+100	nA
OVERVOLTAGE PROTECTION (OVI)					
OVI Threshold	Rising	1.18	1.23	1.28	V
	Falling	1.11	1.17	1.21	
OVI Masking Delay			2		µs
OVI Input Leakage Current	0V < V_{OVI} < 1.5V, T_A = +25°C	-100	0	+100	nA
SWITCHING FREQUENCY AND MAXIMUM DUTY CYCLE (f_{SW} and DMAX)					
Switching Frequency	MAX17498A/MAX17498C	235	250	265	kHz
	MAX17498B	470	500	530	
Maximum Duty Cycle	MAX17498A/MAX17498C	92	94.5	97	%
	MAX17498B	90	92	94	
Minimum Controllable On Time	t_{ONMIN}		110		ns
SOFT-START (SS)					
SS Set-Point Voltage		1.2	1.22	1.24	V
SS Pullup Current	V_{SS} = 400mV	9	10	11	µA
SS Peak Current-Limit-Enable Threshold	SSDONE	1.11	1.17	1.21	V
ERROR AMPLIFIER (EA+, EA-, and COMP)					
EA+ Input Bias Current	V_{EA+} = 1.5V, T_A = +25°C	-100		+100	nA
EA- Input Bias Current	V_{EA-} = 1.5V, T_A = +25°C	-100		+100	nA
Error-Amplifier Open-Loop Voltage Gain			90		dB
Error-Amplifier Transconductance	V_{COMP} = 2V, V_{LIM} = 1V	1.5	1.8	2.1	mS
Error-Amplifier Source Current	V_{COMP} = 2V, EA- < EA+	80	120	210	µA
Error-Amplifier Sink Current	V_{COMP} = 2V, EA- > EA+	80	120	210	µA
Current-Sense Transresistance		0.45	0.5	0.55	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL SWITCH					
DMOS Switch On-Resistance (R_{DSON})	I_{LX} = 200mA		175	380	mΩ
DMOS Peak Current Limit	LIM = 100K	1.62	1.9	2.23	A
DMOS Runaway Current Limit	LIM = 100K	1.9	2.3	2.6	A
LX Leakage Current	V_{LX} = 65V, T_A = +25°C		0.1	1	µA
CURRENT LIMIT (LIM)					
LIM Reference Current		9	10	11	µA
Peak Switch Current Limit with LIM Open		0.39	0.45	0.54	A
Runaway Switch Current Limit with LIM Open		0.39	0.5	0.6	A
Number of Runaway Current-Limit Hits Before Hiccup Timeout			1		#
Overcurrent Hiccup Timeout			32		ms
SLOPE COMPENSATION (SLOPE)					
SLOPE Pullup Current		9	10	11	µA
SLOPE-Compensation Resistor Range	MAX17498B	30		150	kΩ
Default SLOPE-Compensation Ramp	SLOPE = open, SLOPE = SGND, or SLOPE = V_{CC}		60		mV/µs
POWER-GOOD SIGNAL (PGOOD)					
PGOOD Output-Leakage Current (Off State)	V_{PGOOD} = 5V, T_A = +25°C	-1		+1	µA
PGOOD Output Voltage (On State)	I_{PGOOD} = 10mA	0		0.4	V
PGOOD Higher Threshold	EA- rising	93.5	95	96.5	%
PGOOD Lower Threshold	EA- falling	90.5	92	93.5	%
PGOOD Delay After EA- Reaches 95% Regulation			4		ms
THERMAL SHUTDOWN					
Thermal-Shutdown Threshold	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis			20		°C

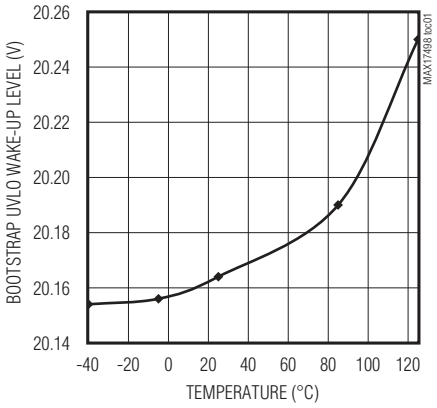
Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: The MAX17498A is intended for use in universal input power supplies. The internal clamp circuit at IN is used to prevent the bootstrap capacitor from charging to a voltage beyond the absolute maximum rating of the device when EN/UVLO is low (shutdown mode). Externally limit the maximum current to IN (hence to clamp) to 2mA (max) when EN/UVLO is low.

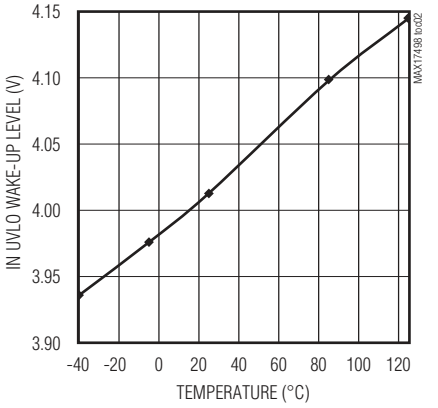
Typical Operating Characteristics

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

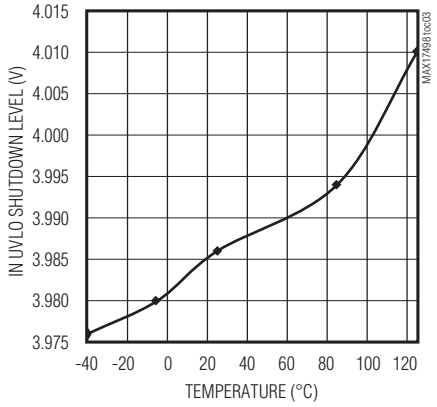
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17498A)



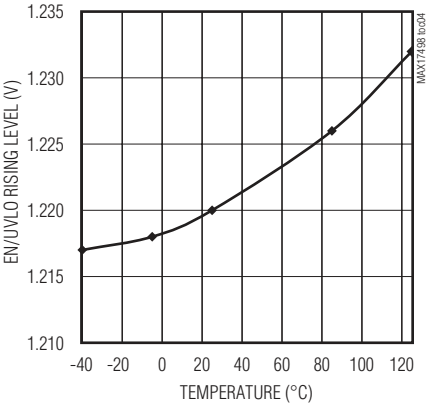
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17498B/MAX17498C)



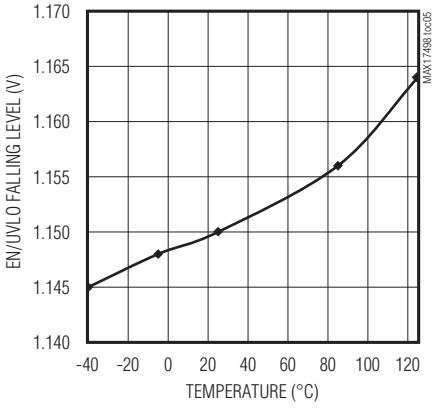
IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE



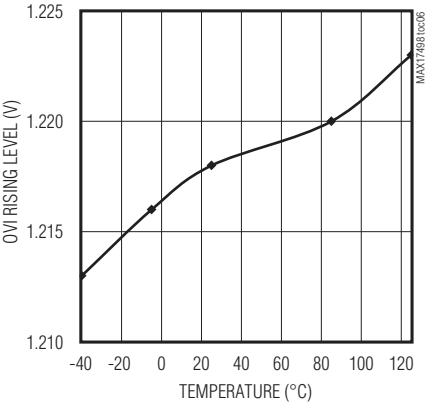
EN/UVLO RISING LEVEL vs. TEMPERATURE



EN/UVLO FALLING LEVEL vs. TEMPERATURE



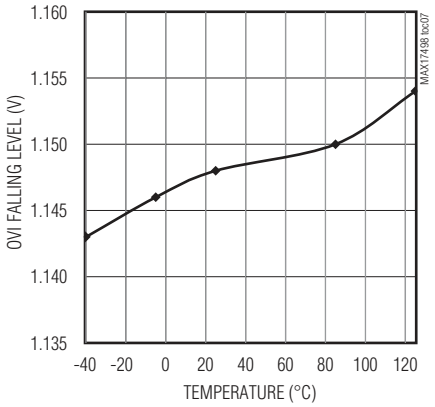
OVI RISING LEVEL vs. TEMPERATURE



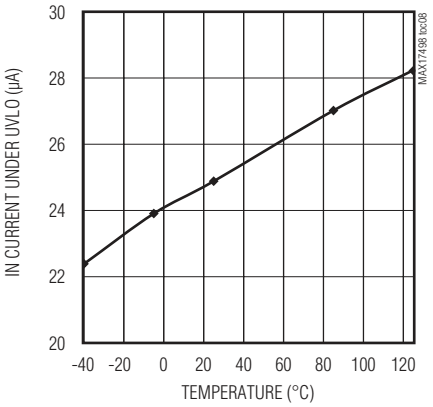
Typical Operating Characteristics (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

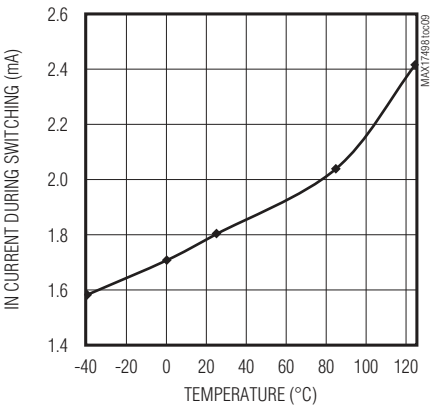
OVI FALLING LEVEL vs. TEMPERATURE



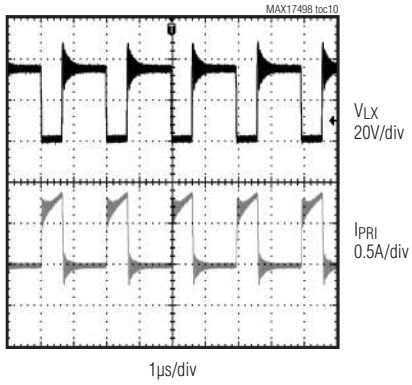
IN CURRENT UNDER UVLO vs. TEMPERATURE



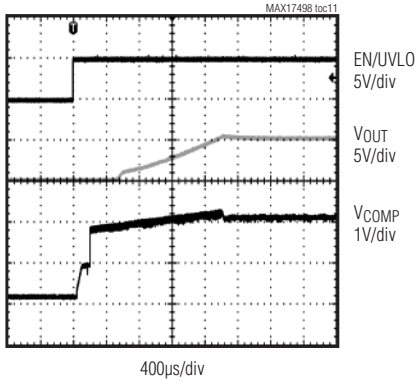
IN CURRENT DURING SWITCHING vs. TEMPERATURE



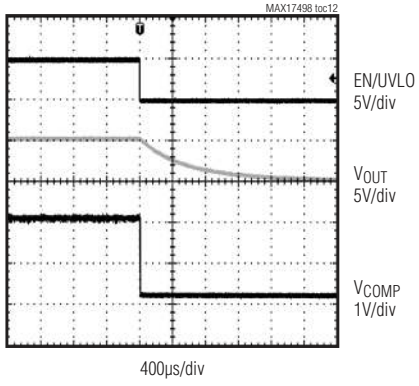
LX AND PRIMARY CURRENT WAVEFORM



EN STARTUP WAVEFORM



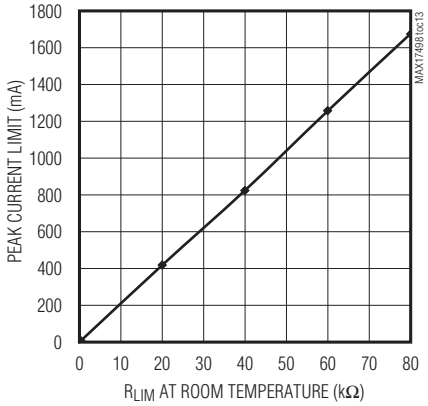
EN SHUTDOWN WAVEFORM



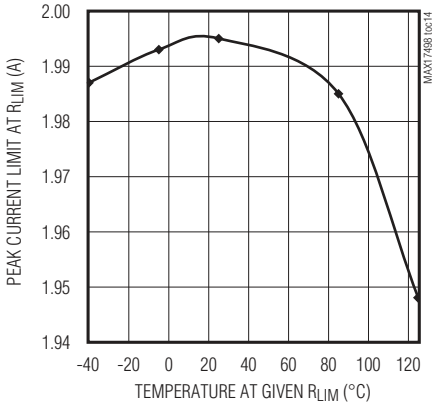
Typical Operating Characteristics (continued)

(V_{IN} = +15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{IN} = 1µF, C_{VCC} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

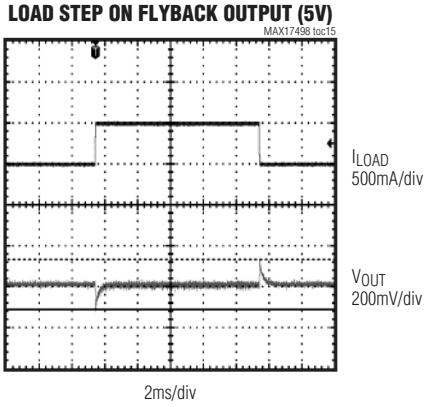
PEAK CURRENT LIMIT (I_{LIM}) vs. R_{LIM} AT ROOM TEMPERATURE



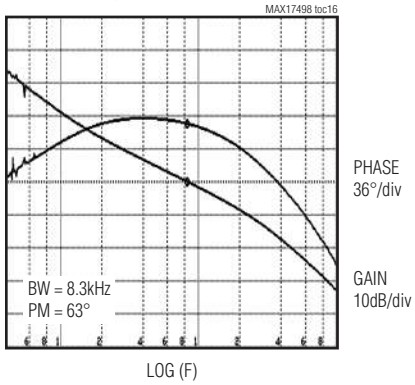
PEAK CURRENT LIMIT AT R_{LIM} = 100kΩ vs. TEMPERATURE



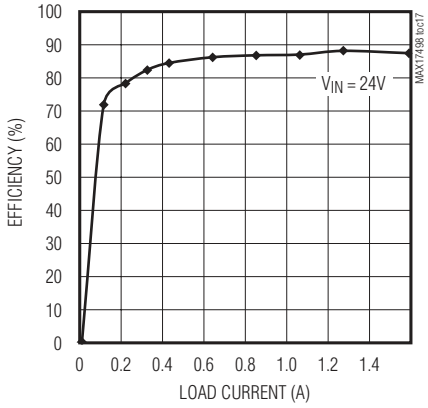
TRANSIENT RESPONSE FOR 50% LOAD STEP ON FLYBACK OUTPUT (5V)



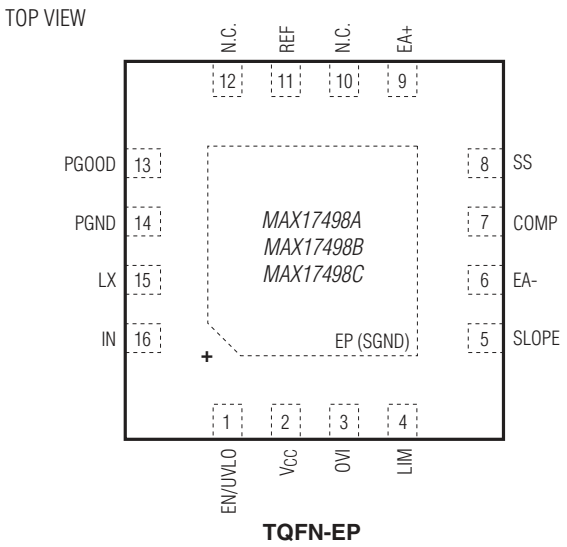
BODE PLOT - (5V OUTPUT AT 24V INPUT)



EFFICIENCY GRAPH AT 24V INPUT (FLYBACK REGULATOR)



Pin Configuration



TQFN-EP

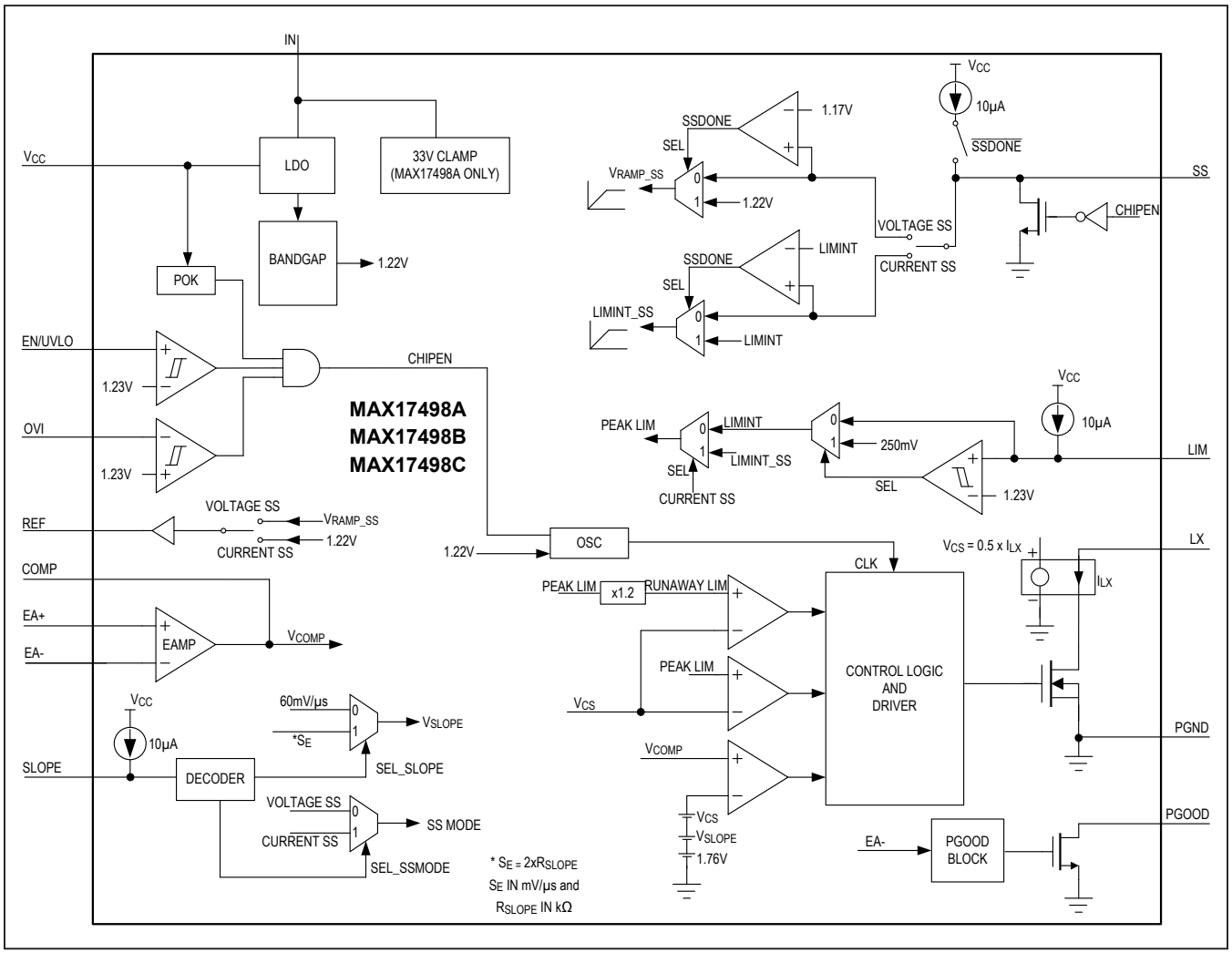
Pin Description

PIN	NAME	FUNCTION
1	EN/UVLO	Enable/Undervoltage-Lockout Pin. Drive to > 1.23V to start the devices. To externally program the UVLO threshold of the input supply, connect a resistor-divider between input supply EN/UVLO and SGND.
2	V_{CC}	Linear Regulator Output. Connect input bypass capacitor of at least 2.2µF from V_{CC} to SGND as close as possible to the IC.
3	OVI	Overvoltage Comparator Input. Connect a resistor-divider between the input supply (OVI) and SGND to set the input overvoltage threshold.
4	LIM	Current-Limit Setting Pin. Connect a resistor between LIM and SGND to set the peak-current limit for nonisolated flyback converter. Peak-current limit defaults to 500mA if unconnected.
5	SLOPE	Slope Compensation Input Pin. SLOPE is a dual function pin. This pin is used to select the soft-start mode, and the slope value. Connect the SLOPE pin to SGND for a fixed default slope of 60mV/µs and the current soft-start mode. Connect the SLOPE pin to V_{CC} or leave the SLOPE pin OPEN for a default slope of 60mV/µs and the voltage soft-start mode. Connecting a resistor value in the range of 30kΩ–150kΩ from the SLOPE pin to SGND provides programmable slope and the voltage soft-start mode. Slope is not programmable in the current soft-start mode. See the *Programming Slope Compensation (SLOPE)* section.
6	EA-	Inverting Input of the Flexible Error Amplifier. Connect to mid-point of resistor-divider from the positive terminal output to SGND.
7	COMP	Flexible Error-Amplifier Output. Connect the frequency-compensation network between COMP and SGND.
8	SS	Soft-Start Pin. Connect a capacitor from SS to SGND to set the soft-start time interval.
9	EA+	Noninverting Input of the Flexible Error Amplifier. Connect EA+ to REF for positive output voltage design. See the *Programming Output Voltage* section for negative output-voltage design.

Pin Description (continued)

PIN	NAME	FUNCTION
10, 12	N.C.	No Connection
11	REF	Internal 1.22V Reference Output Pin. Connect a 100pF capacitor from REF to SGND.
13	PGOOD	Open-Drain Output. PGOOD goes high when EA- is within 5% of the set point. PGOOD pulls low when EA- falls below 92% of its set-point value.
14	PGND	Power Ground for Converter
15	LX	External Transformer/Inductor Connection for the Converter
16	IN	Internal Linear Regulator Input. Connect IN to the input-voltage source. Bypass IN to PGND with a 1µF (min) ceramic capacitor.
—	EP (SGND)	Exposed Pad. Internally connected to SGND. Connect EP to a large copper plane at SGND potential to provide adequate thermal dissipation. Connect EP (SGND) to PGND at a single point.

Block Diagram



Detailed Description

The MAX17498A offers a bootstrap UVLO wakeup level of 20V with a wide hysteresis of 15V (min) optimized for implementing an isolated and nonisolated universal (85V AC to 265V AC) offline single-switch flyback converter or telecom (36V to 72V) power supplies. The MAX17498B/MAX17498C offer a UVLO wakeup level of 4.4V and are well suited for low-voltage DC-DC flyback/boost power supplies. An internal reference (1.22V) can be used to regulate the output down to 1.23V in non-isolated flyback and boost applications. Additional semi-regulated outputs, if needed, can be generated by using additional secondary windings on the flyback converter transformer. A flexible error amplifier and REF allow the end-user selection between regulating positive and negative outputs.

The devices utilize peak current-mode control and external compensation for optimizing the loop performance for various inductors and capacitors. The devices include a runaway current limit feature that triggers hiccup mode operation to protect the external component by halting switching for 32ms before restart. The devices include voltage soft-start for nonisolated designs and current soft-start for isolated designs to allow monotonic rise of the output voltage. The voltage or current soft-start can be selected using the SLOPE pin.

Input Voltage Range

The MAX17498A has different rising and falling UVLO thresholds on the IN pin than those of the MAX17498B/MAX17498C. The thresholds for the MAX17498A are optimized for implementing power-supply startup schemes typically used for offline AC-DC power supplies. The MAX17498A is therefore well suited for operation from the rectified DC bus in AC-DC power-supply applications typically encountered in front-end industrial power-supply applications. As such, the MAX17498A has no limitation on the maximum input voltage as long as the external components are rated suitably and the maximum operating voltages of the MAX17498A are respected. The MAX17498A can successfully be used in universal input-rectified (85V to 265V AC) bus applications, rectified 3-phase DC bus applications, and telecom (36V to 72V DC) applications.

The MAX17498B/MAX17498C are intended for implementing a flyback (isolated and nonisolated) and boost converter with an on-board 65V rated n-channel MOSFET. The IN pin of the MAX17498B/MAX17498C has a maximum operating voltage of 36V. The MAX17498B/MAX17498C implement rising and falling thresholds on the IN pin that assume power-supply startup schemes, typical of lower voltage DC-DC applications, down to an input voltage of 4.5V DC. Therefore, flyback converters with a 4.5V to 36V supply voltage range can be implemented with the MAX17498B/MAX17498C.

Internal Linear Regulator (V_{CC})

The internal functions and driver circuits are designed to operate from a 5V ±5% power-supply voltage. The devices have an internal linear regulator that is powered from the IN pin and generates a 5V power rail. The output of the linear regulator is connected to the V_{CC} pin and should be decoupled with a 2.2µF capacitor to ground for stable operation. The V_{CC} converter output supplies the operating current for the devices. The maximum operating voltage of the IN pin is 29V for the MAX17498A and 36V for the MAX17498B/MAX17498C.

Configuring the Power Stage (LX)

The devices use an internal n-channel MOSFET to implement internal current sensing for current-mode control and overcurrent protection of the flyback/boost converter. To facilitate this, the drain of the internal nMOSFET is connected to the source of the external MOSFET in the MAX17498A high-input-voltage applications. The gate of the external MOSFET is connected to the IN pin. Ensure by design that the IN pin voltage does not exceed the maximum operating gate-voltage rating of the external MOSFET. The external MOSFET gate-source voltage is controlled by the switching action of the internal nMOSFET, while also sensing the source current of the external MOSFET. In the MAX17498B/MAX17498C-based applications, the LX pin is directly connected to either the flyback transformer primary winding or to the boost-converter inductor.

Maximum Duty Cycle

The MAX17498A/MAX17498C operate at a maximum duty cycle of 94%. The MAX17498B offers a maximum duty cycle of 92%. The devices can be used to implement flyback and boost converters involving large input-to-output voltage ratios in DC-DC applications.

Power-Good Signal (PGOOD)

The devices include a PGOOD signal that serves as a power-good signal to the system. PGOOD is an open-drain signal and requires a pullup resistor to the preferred supply voltage. The PGOOD signal monitors EA- and pulls high when EA- is 95% (typ) of its regulation value (1.22V). For isolated power supplies, PGOOD cannot serve as a power-good signal.

Soft-Start

The devices implement soft-start operation for the flyback/boost converter. A capacitor connected to the SS pin programs the soft-start period for the flyback/boost converter. The soft-start feature reduces the input inrush current. These devices allow the end user to select between voltage soft-start usually preferred in nonisolated applications and current soft-start, which is useful in isolated applications to get a monotonic rise in the output voltage. See the *Programming Soft-Start of the Flyback/Boost Converter (SS)* section.

Spread-Spectrum Factory Option

For EMI-sensitive applications, a spread-spectrum-enabled version of the device can be requested from the factory. The frequency-dithering feature modulates the switching frequency by ±10% at a rate of 4kHz. This spread-spectrum-modulation technique spreads the energy of switching-frequency harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

Applications Information

Startup Voltage and Input Overvoltage-Protection Setting (EN/UVLO, OVI)

The devices' EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The devices do not commence startup operation unless the EN/UVLO pin voltage exceeds 1.23V (typ). The devices turn off if the EN/UVLO pin voltage falls below 1.17V (typ). A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.23V (typ) turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 1. When voltage at the OVI pin exceeds 1.23V (typ), the devices stop switching and resume switching operations only if voltage at the OVI pin falls below 1.17V (typ). For given values of startup DC input voltage (V_{START}), and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 24.9kΩ resistor for R_{OVI}:

$$R_{EN} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1\right] k\Omega$$

where R_{OVI} is in kΩ while V_{START} and V_{OVI} are in volts.

$$R_{SUM} = \left[R_{OVI} + R_{EN}\right] \times \left[\frac{V_{START}}{1.23} - 1\right] k\Omega$$

where R_{EN} and R_{OVI} are in kΩ. In universal AC input applications, R_{SUM} might need to be implemented as equal resistors in series (R_{DC1}, R_{DC2}, R_{DC3}) so that voltage across each resistor is limited to its maximum operation voltage.

$$R_{DC1} = R_{DC2} = R_{DC3} = \frac{R_{SUM}}{3} k\Omega$$

For low-voltage DC-DC applications based on the MAX17498B/MAX17498C, a single resistor can be used in the place of R_{SUM}, as the voltage across it is approximately 40V.

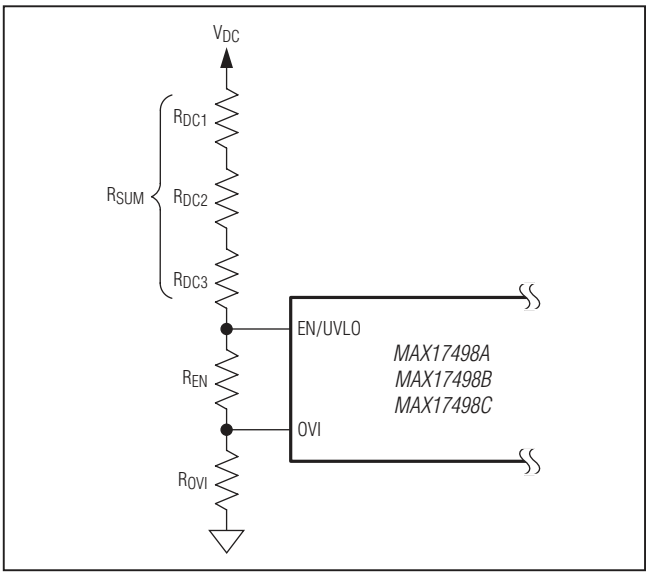


Figure 1. Programming EN/UVLO and OVI

Startup Operation

The MAX17498A is optimized for implementing an offline single-switch flyback converter and has a 20V IN UVLO wake-up level with hysteresis of 15V (min). In offline applications, a simple cost-effective RC startup circuit is used. When the input DC voltage is applied, the startup resistor (R_{START}) charges the startup capacitor (C_{START}), causing the voltage at the IN pin to increase towards the wake-up IN UVLO threshold (20V typ). During this time, the MAX17498A draws a low startup current of 20µA (typ) through R_{START}. When the voltage at IN reaches the wake-up IN UVLO threshold, the MAX17498A commences switching operations and drives the internal n-channel MOSFET whose drain is connected to the LX pin. In this condition, the MAX17498A draws 1.8mA current from C_{START}, in addition to the current required to switch the gate of the external nMOSFET. Since this current cannot be supported by the current through RSTART, the voltage on C_{START} starts to drop. When suitably configured, as shown in the Figure 2 the external nMOSFET is switched by the LX pin and the flyback converter generates pulses in bias winding NB. The soft-start period of the converter should be programmed so the bias winding pulses sustain the voltage on C_{START} before it falls below 5V, thus allowing continued operation. The large hysteresis (15V typ) of the MAX17498A allows for a small startup capacitor (C_{START}). The low startup current (20µA typ) allows the use of a large start resistor (R_{START}); thus, reducing power dissipation at higher DC bus voltages. Figure 2 shows the typical RC startup scheme for the MAX17498A. R_{START} might need to be implemented as equal, multiple resistors in series (R_{IN1}, R_{IN2}, and R_{IN3}) to share the applied high DC voltage in offline applications so that the voltage across each resistor is limited to the maximum continuous operating-voltage rating. R_{START} and C_{START} can be calculated as:

$$C_{START} = 0.75 \left(C_{VCC} + I_{IN} \times t_{SS} \times 0.1 + \frac{0.04 \times t_{SS} \times Q_G \times f_{sw}}{10^6} \right) \mu F$$

where I_{IN} is the supply current drawn at the IN pin in mA, Q_G is the gate charge of the external nMOSFET in nC, f_{SW} is the switching frequency of the converter in Hz, and t_{SS} is the soft-start time programmed for the flyback converter in ms. C_{VCC} is the cumulative capacitor used in VCC node. See the *Programming Soft-Start of the Flyback/Boost Converter (SS)* section.

$$R_{START} = \frac{(V_{START} - 10) \times 50}{[1 + C_{START}]} k\Omega$$

where C_{START} is the startup capacitor in µF.

For designs that cannot accept power dissipation in the startup resistors at high DC input voltages in offline applications, the startup circuit can be set up with a current source instead of a startup resistor as shown in Figure 3. Resistors R_{SUM} and R_{ISRC} can be calculated as:

$$R_{SUM} = \frac{V_{START}}{10} M\Omega$$

$$R_{ISRC} = \frac{V_{BEQ1}}{70} M\Omega$$

The IN UVLO wakeup threshold of the MAX17498B/MAX17498C is set to 3.9V (typ) with a 200mV hysteresis, optimized for low-voltage DC-DC applications down to 4.5V. For applications where the input DC

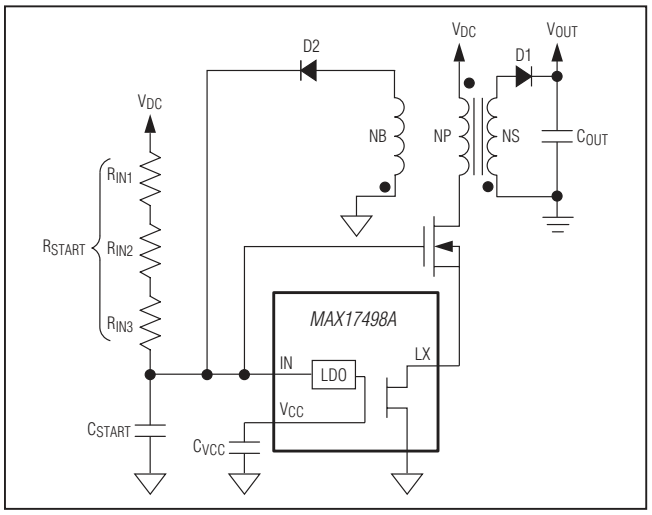


Figure 2. MAX17498A RC-Based Startup Circuit

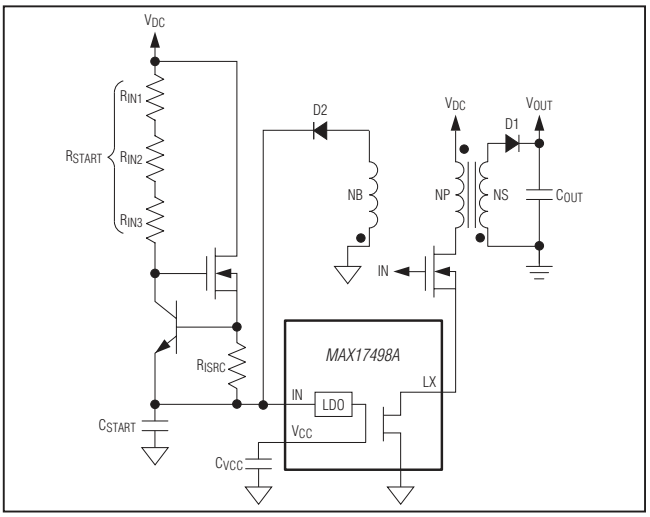


Figure 3. MAX17498A Current Source-Based Startup Circuit

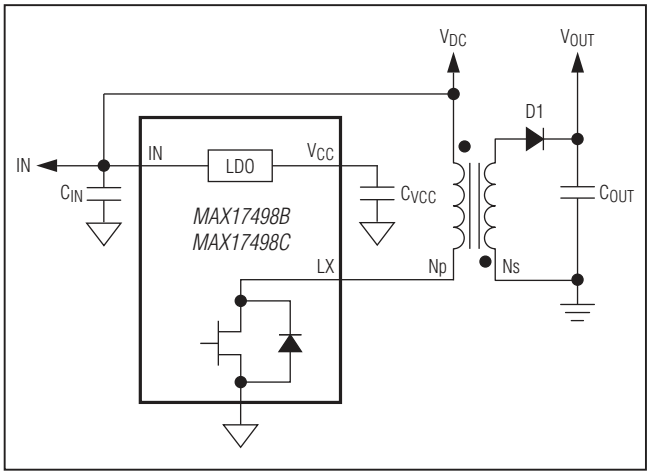


Figure 4. MAX17498B/MAX17498C Typical Startup Circuit with IN Connected Directly to DC Input

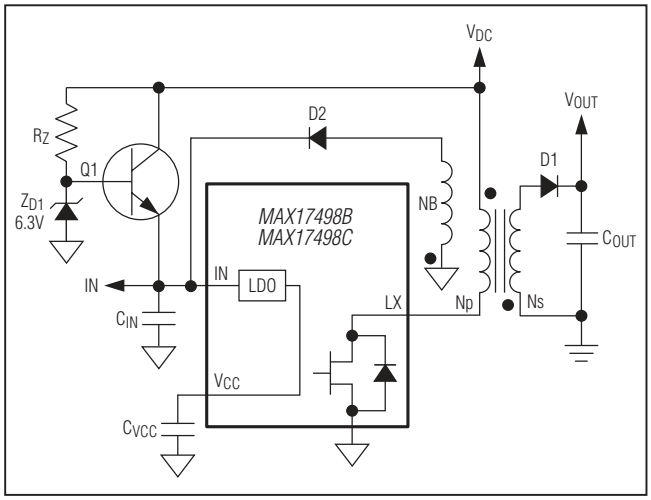


Figure 5. MAX17498B/MAX17498C Typical Startup Circuit with Bias Winding to Turn Off Q1 and Reduce Power Dissipation

voltage is low enough (e.g., 4.5V to 5.5V DC) that the power loss incurred to supply the operating current of the MAX17498B/MAX17498C can be tolerated, the IN pin is directly connected to the DC input, as shown in Figure 4. In the case of higher DC input voltages (e.g., 16V to 32V DC), a startup circuit, such as that shown in Figure 5, can be used to minimize power dissipation. In this startup scheme, the transistor (Q1) supplies the switching current until a bias winding NB comes up and turns off Q1. The resistor (R_Z) can be calculated as:

$$R_Z = 2 \times (V_{INMIN} - 6.3)\,k\Omega$$

where V_{INMIN} is the minimum input DC voltage.

Programming Soft-Start of the Flyback/Boost Converter (SS)

During the soft-start period (t_{SS}), a 10µA current source at the SS pin charges the SS capacitor such that the voltage at the SS pin is increased monotonically from zero to 1.22V. Refer to the *Block Diagram*.

In the voltage soft-start scheme, the MAX17498 connects the SS pin directly to the REF pin until the SSDONE (soft-start complete) signal is low. Since the REF pin is connected to the EA+ pin, the output voltage increases monotonically to the regulation point during t_{SS}. When SSDONE is high, the REF pin is switched over to a fixed 1.22V reference.

In applications where it is desired to ramp up the peak current, the current soft-start scheme can be used. In the current soft-start scheme, the REF pin is directly connected to a fixed 1.22V reference. During the soft-start period, the input of the peak current-limit comparator is increased gradually using the SS pin voltage as a peak current-limit reference (LIMINT_SS). During this ramp interval, the output voltage increases monotonically to the regulation point. When SSDONE is high, the peak current-limit comparator reference is switched over to LIMINT. In this scheme, for a given peak current limit setting, the duration needed for the output voltage to ramp from zero to its regulation set point depends on the load on the output.

Programming Output Voltage

The devices incorporate a flexible error amplifier that allows regulating to both the positive and negative outputs. The positive output voltage of the converter can be programmed by selecting the correct values for the resistor-divider connected from V_{OUT}, the flyback/boost output to ground, with the midpoint of the divider connected to the EA- pin (Figure 6). With R_B selected in the range of 20kΩ to 50kΩ, R_U can be calculated as:

$$R_U = R_B \times \left[\frac{V_{OUT}}{1.22} - 1\right] k\Omega$$

where R_B is in kΩ.

The negative output voltage of the converter can be programmed by selecting the correct values for the resistor-divider connected from V_{OUT}, the flyback/boost output to REF with the midpoint of the divider connected to the EA+ pin (Figure 7). With R1 selected in the range of 20kΩ to 50kΩ, R2 can be calculated as:

$$R2 = R1 \times \left[\frac{V_{OUT}}{1.22}\right] k\Omega$$

where R1 is in kΩ.

Current-Limit Programming (LIM)

The devices include a robust overcurrent-protection scheme that protects the device under overload and short-circuit conditions. For the flyback/boost converter, the devices include a cycle-by-cycle peak current limit that turns off the driver whenever the current into the LX pin exceeds an internal limit that is programmed by the resistor connected from the LIM pin to GND. The devices include a runaway current limit that protects the device under short-circuit conditions. One occurrence of the runaway current limit triggers a hiccup mode that protects the converter by immediately suspending switching for a period of time (32ms). This allows the overload current to decay due to power loss in the converter resistances, load, and the output diode of the flyback/boost converter before soft-start is attempted again. The resistor at the LIM pin for a desired current limit (I_{PK}) can be calculated as:

$$R_{LIM} = 50 \times I_{PK}\ k\Omega$$

where I_{PK} is expressed in amperes.

For a given peak current-limit setting, the runaway current limit is typically 20% higher. The runaway current-limit-triggered hiccup operation is always enabled even during soft-start.

Programming Slope Compensation (SLOPE)

To avoid subharmonic instability that occurs naturally over all specified load and line conditions in peak current-mode-controlled converters operating at duty cycles greater than 50% and continuous conduction mode designs, the converter needs slope compensation. A minimum amount of slope signal is added to the sensed current signal even for converters operating below 50% duty or discontinuous-mode designs to provide stable, jitter-free operation. Connect the SLOPE pin to SGND for a fixed default slope of 60mV/µs and current soft-start mode. Slope is not programmable in current soft-start mode. Connect the SLOPE pin to V_{CC} or leave the SLOPE pin OPEN for a default slope of 60mV/µs, and voltage soft-start mode. In voltage soft-start mode, the SLOPE pin allows the user to program the necessary slope compensation by setting the value of the resistor (RSLOPE) connected from SLOPE pin to ground.

$$R_{SLOPE} = 0.5 \times S_E\ k\Omega$$

where the slope (S_E) is expressed in millivolts per microsecond.

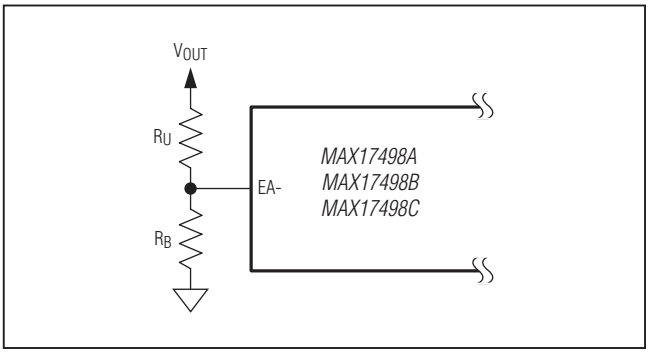


Figure 6. Programming the Positive Output Voltage

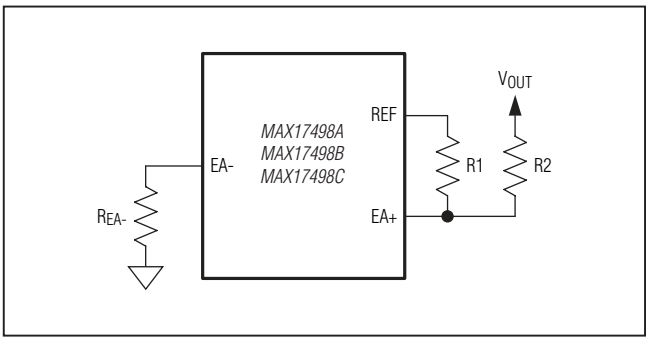


Figure 7. Programming the Negative Output Voltage

Thermal Considerations

It should be ensured that the junction temperature of the devices does not exceed +125°C under the operating conditions specified for the power supply. The power dissipated in the devices to operate can be calculated using the following equation:

$$P_{IN} = V_{IN} \times I_{IN}$$

where V_{IN} is the voltage applied at the IN pin and I_{IN} is operating supply current (see the *Electrical Characteristics* table).

The conduction loss in the internal n-channel MOSFET can be calculated using the formula below:

$$P_{CONDUCTION} = I_{LXRMS}^2 \times R_{DSON}$$

where,

R_{DSON} = DMOS switch on resistance

I_{LXRMS} = Switch RMS current

When the converter is operating in continuous conduction mode (CCM), the switch experiences transition loss when it is turned-on. Since the switch current stats from zero, transition loss doesn't exist in discontinuous conduction

mode (DCM) design. The transition loss in CCM design can be calculated using the equation given below:

$$P_{TRANSITION} = \frac{1}{2} \times V_{SW} \times I_{SW} \times t_f \times f_{SW}$$

where,

V_{SW} = Voltage across the internal MOSFET before it is turned on.

- $V_{SW} = V_{OUT}$ in CCM boost converter,
- $V_{SW} = V_{INMAX} + V_{OUT}$ x transformer primary turns/tranformer secondary turns in CCM flyback converter.

I_{SW} = Switch current. Inductor valley current in boost converter, and transformer primary valley current in flyback converter.

t_f = Switch voltage fall-time when it is turned-on. The t_f can be calculated using the 5V/ns falling slew-rate on the switch voltage.

When the converter is operating in continuous conduction mode (CCM), the switch experiences reverse recovery loss due to the diode rectifier. Since the switch current stats from zero, reverse recovery loss doesn't exist in discontinuous conduction mode (DCM) converters. The reverse recovery loss in CCM design can be calculated using the equation given below:

$$P_{RR} = Q_{RR} \times V_{SW} \times f_{SW}$$

where,

Q_{RR} = reverse recovery charge of the rectifier diode.

When the switch is turned-on there exists additional capacitive loss due to LX node capacitance. This loss can be calculated using the equation below:

$$P_{CAP} = \frac{1}{2} \times C_{LX} \times V_{SW}^{\ 2} \times f_{SW}$$

where C_{LX} is the LX node capacitance, which includes the drain-to-source capacitance (82pF typ) of the internal MOSFET, and the transformer or inductor parasitic winding capacitance.

The total loss in the device can be calculated using the equation below:

$$P_{LOSS} = P_{IN} + P_{CONDUCTION} + P_{TRANSITION} + P_{RR} + P_{CAP}$$

The maximum power that can be dissipated in the devices is 1666mW at +70°C temperature. The power-dissipation capability should be derated as the temperature rises above +70°C at 21mW/°C. For a multilayer board, the thermal-performance metrics for the package are given below:

$$\theta_{JA} = 48°C / W$$
$$\theta_{JC} = 10°C / W$$

The junction-temperature rise of the devices can be estimated at any given maximum ambient temperature (T_{AMAX}) from the following equation:

$$T_{JMAX} = T_{AMAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the devices is maintained at a given temperature (T_{EPMAX}) by using proper heatsinks, then the junction-temperature rise of the devices can be estimated at any given maximum ambient temperature from the following equation:

$$T_{JMAX} = T_{EPMAX} + (\theta_{JC} \times P_{LOSS})$$

Layout, Grounding, and Bypassing

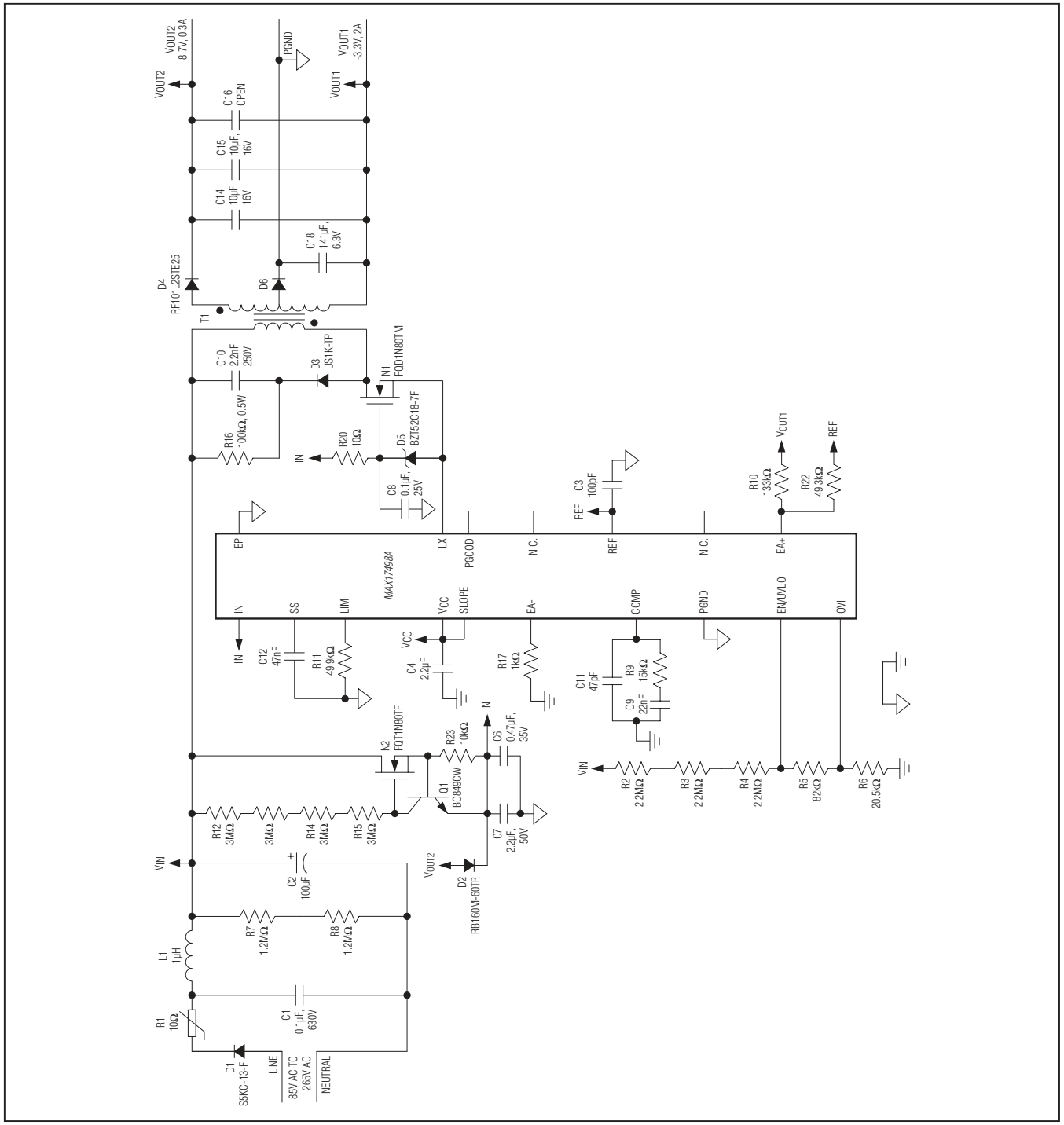
All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency switching power converters. This implies that the loop areas for forward and return pulsed currents in various parts of the circuit should be minimized. Additionally, small-current loop areas reduce radiated EMI. Similarly, the heatsink of the main MOSFET presents a dV/dt source, and therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least noisy section of the power ground plane, typically the return of the input filter capacitor. The negative terminal of the filter capacitor, ground return of the power switch, and current-sensing resistor must be close together. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation. For a sample layout that ensures first-pass success, refer to the MAX17498B Evaluation Kit.

For universal AC input designs, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

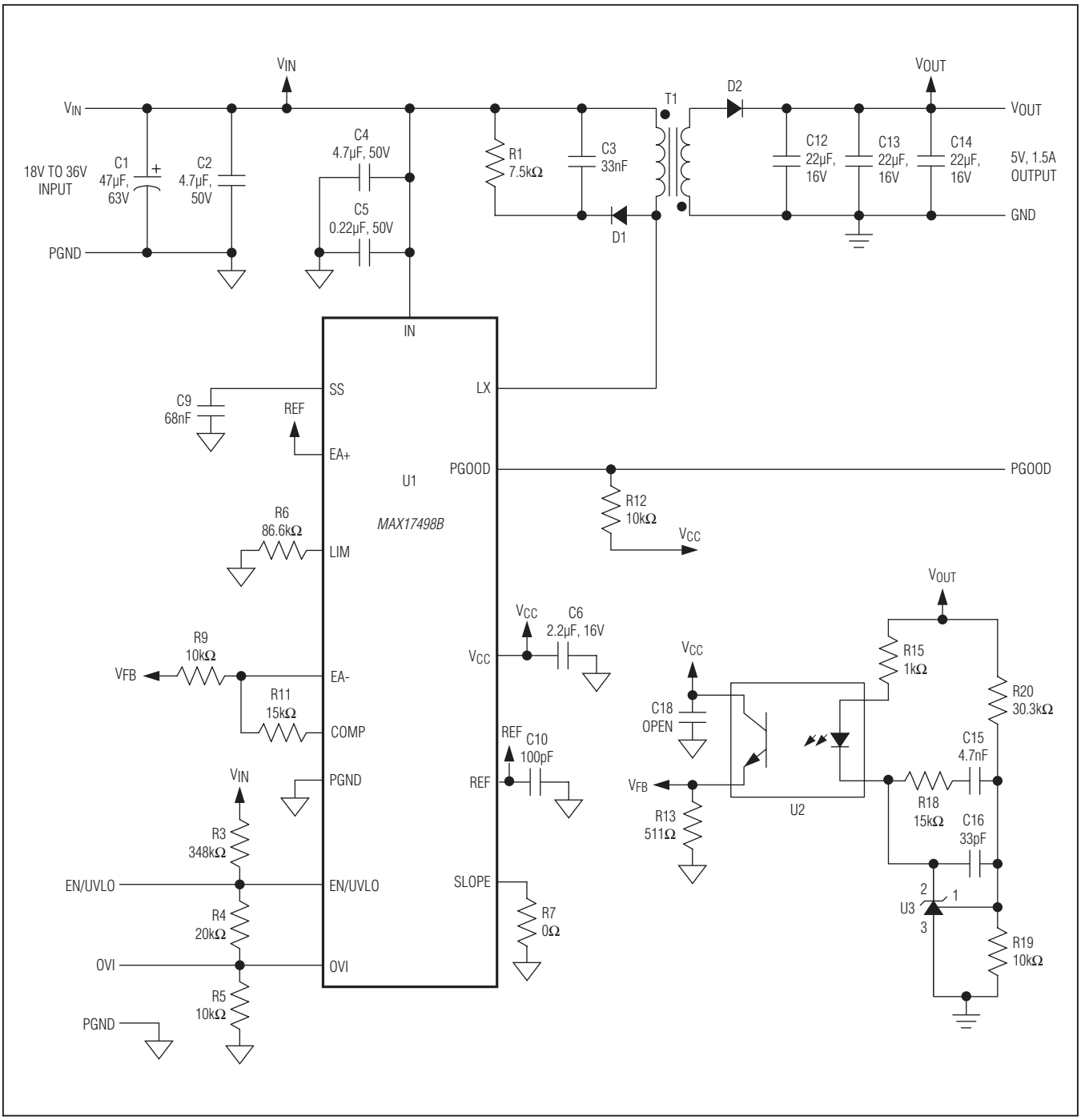
Typical Application Circuits

MAX17498A Nonisolated Multiple-Output AC-DC Power Supply



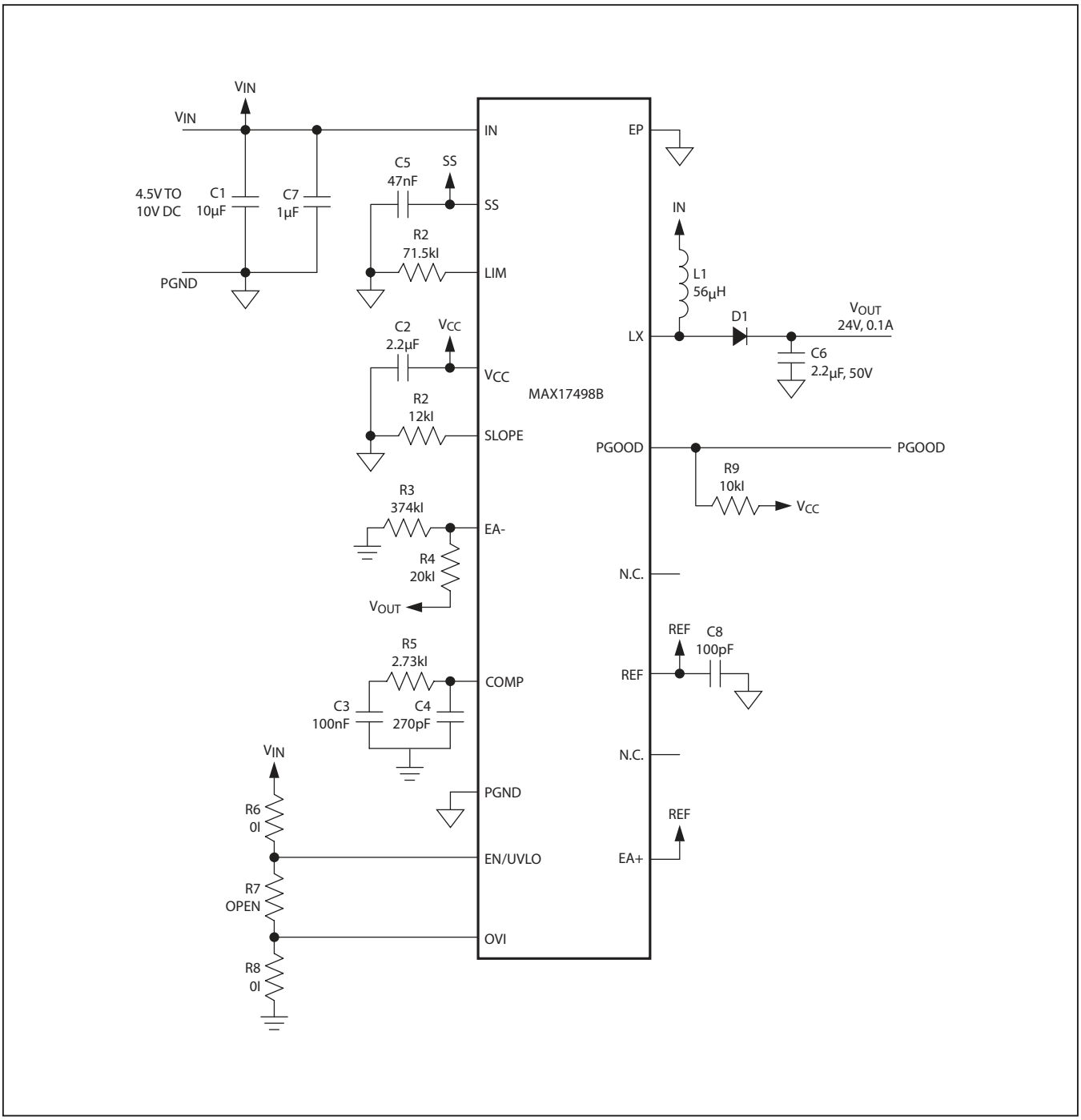
Typical Application Circuits (continued)

MAX17498B Isolated DC-DC Power Supply



Typical Application Circuits (continued)

MAX17498B Boost Power Supply



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX17498AATE+	-40°C to +125°C	16 TQFN-EP*	250kHz, Offline Flyback Converter
MAX17498BATE+	-40°C to +125°C	16 TQFN-EP*	500kHz, Low-Voltage DC-DC Flyback/Boost Converter
MAX17498CATE+	-40°C to +125°C	16 TQFN-EP*	250kHz, Low-Voltage DC-DC Flyback Converter

+Denotes lead(Pb)-free/RoHS-compliance.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	3/12	Removed future product references for MAX17498B and MAX17498C	27
2	2/13	Changed the maximum duty cycle for the A/C variants to 92% (min), 94.5% (typ), and 97% (max); updated General Description, Benefits and Features, Detailed Description, Maximum Duty Cycle, Current-Limit Programming (LIM), Programming Slope Compensation (SLOPE), and Peak/RMS-Current Calculation secondary RMS current equation	1, 3, 9, 10, 14, 15
3	4/13	Updated the Benefits and Features, removed sections on pages 15–21, updated Figures 1, 3–6, 11, 12	1, 10, 12, 13, 15–22, 24, 25
4	10/20	Updated the *Benefits and Features, Electrical Characteristics, Pin Description, Detailed Description, Startup Operation, Programming Slope Compensation (SLOPE)* and *Thermal Considerations* sections, and *MAX17498B Boost Power Supply*; replaced the *Block Diagram* and the *Programming Soft-Start of the Flyback/Boost Converter (SS)*	1, 3–4, 8–10 12–15, 18