ALPHA & OMEGA SEMICONDUCTOR

AON6906A

30V Dual Asymmetric N-Channel MOSFET

General Description

The AON6906A is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization.It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET is desgined to minimze switching losses. The Q2 "Low Side" MOSFET is desgined for low $R_{DS(ON)}$ to reduce conduction losses.Power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Crss.In addition,switching behavior is well controlled with a "Schottky style" soft recovery body diode.

Product Summary

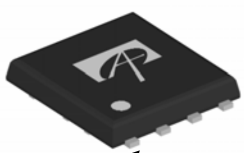
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	37A	48A
$R_{DS(ON)}$ (at V_{GS}=10V)	<14.4mΩ	<11.7mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	<21.3mΩ	<17.5mΩ

100% UIS Tested

100% Rg Tested

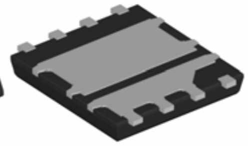
DFN5X6

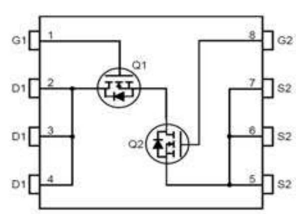
Top View



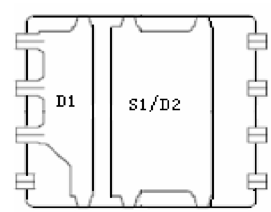
PIN1

Bottom View





Top View



Bottom View

Absolute Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**Max Q1**	**Max Q2**	**Units**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current	T_C=25°C	I_D	37	48	A
	T_C=100°C		23	30	
Pulsed Drain Current [C]		I_{DM}	85	100	
Continuous Drain Current	T_A=25°C	I_{DSM}	9.1	10	A
	T_A=70°C		7.2	8.1	
Avalanche Current [C]		I_{AS}, I_{AR}	21	23	A
Avalanche Energy L=0.1mH [C]		E_{AS}, E_{AR}	22	26	mJ
Power Dissipation [B]	T_C=25°C	P_D	31	45	W
	T_C=100°C		12.5	18	
Power Dissipation [A]	T_A=25°C	P_{DSM}	1.9	2	W
	T_A=70°C		1.2	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics							
Parameter		**Symbol**	**Typ Q1**	**Typ Q2**	**Max Q1**	**Max Q2**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	29	27	35	32	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		56	51	67	61	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.3	2.3	4	2.8	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1.3	1.8	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		85			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=9.1A			12	14.4	mΩ
			T_J=125°C		17.5	21	
		V_{GS}=4.5V, I_D=9.1A			17	21.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=9.1A			30		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.73	1	V
I_S	Maximum Body-Diode Continuous Current					33	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		400	510	670	pF
C_{oss}	Output Capacitance			150	220	310	pF
C_{rss}	Reverse Transfer Capacitance			13	22	38	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.9	1.8	2.7	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=9.1A		5.9	7.4	9	nC
Q_g(4.5V)	Total Gate Charge			2.6	3.3	4.0	nC
Q_{gs}	Gate Source Charge			1.2	1.5	1.8	nC
Q_{gd}	Gate Drain Charge			0.8	1.4	2	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			4.3		ns
t_r	Turn-On Rise Time				8		ns
$t_{D(off)}$	Turn-Off DelayTime				15.8		ns
t_f	Turn-Off Fall Time				3.4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=9.1A, dI/dt=500A/µs		7.2	9	11	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=9.1A, dI/dt=500A/µs		11.8	14.7	17.7	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by package.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

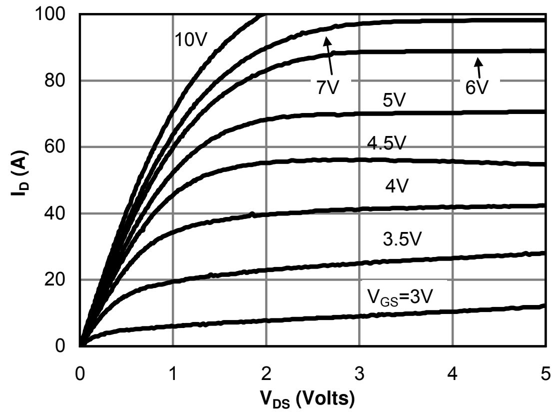


Fig 1: On-Region Characteristics (Note E)

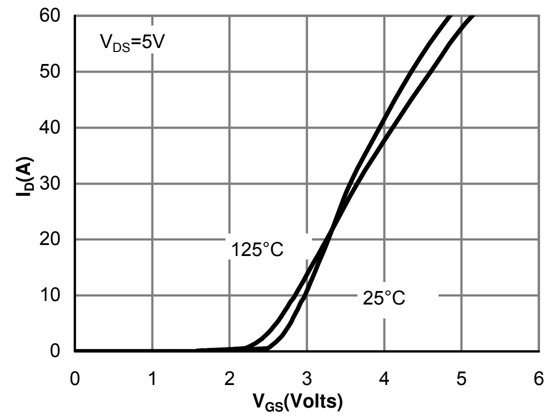


Figure 2: Transfer Characteristics (Note E)

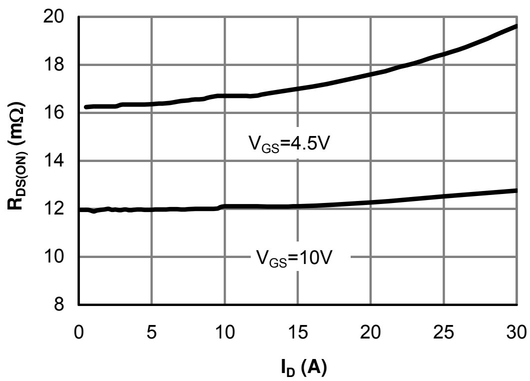


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

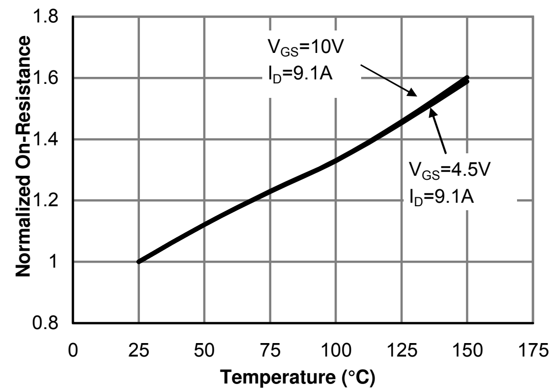


Figure 4: On-Resistance vs. Junction Temperature (Note E)

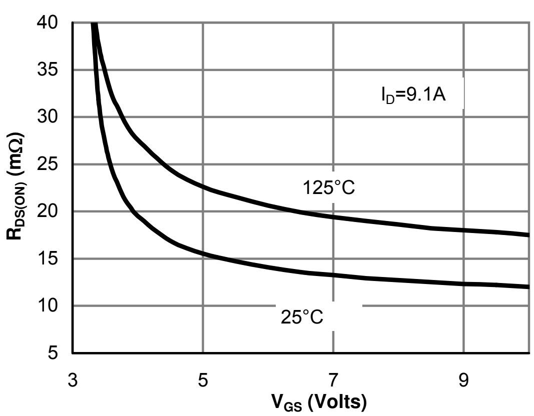


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

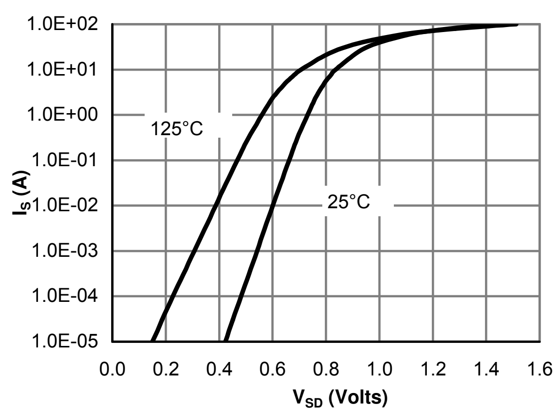


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

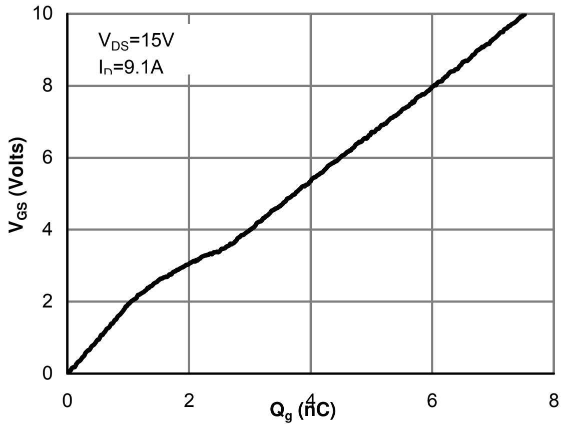


Figure 7: Gate-Charge Characteristics

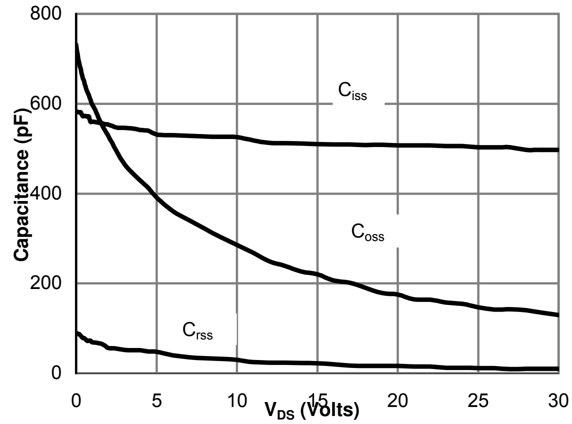


Figure 8: Capacitance Characteristics

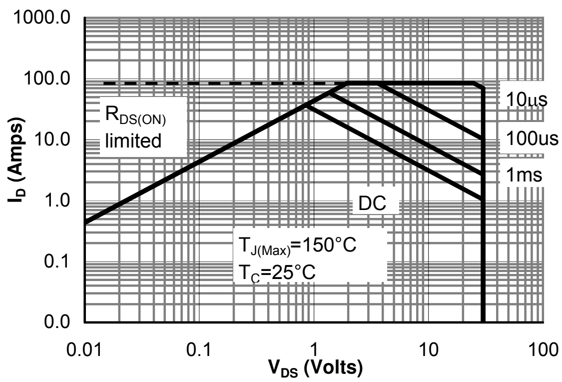


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

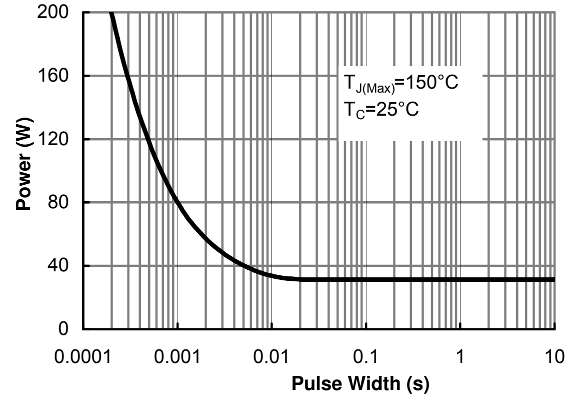


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

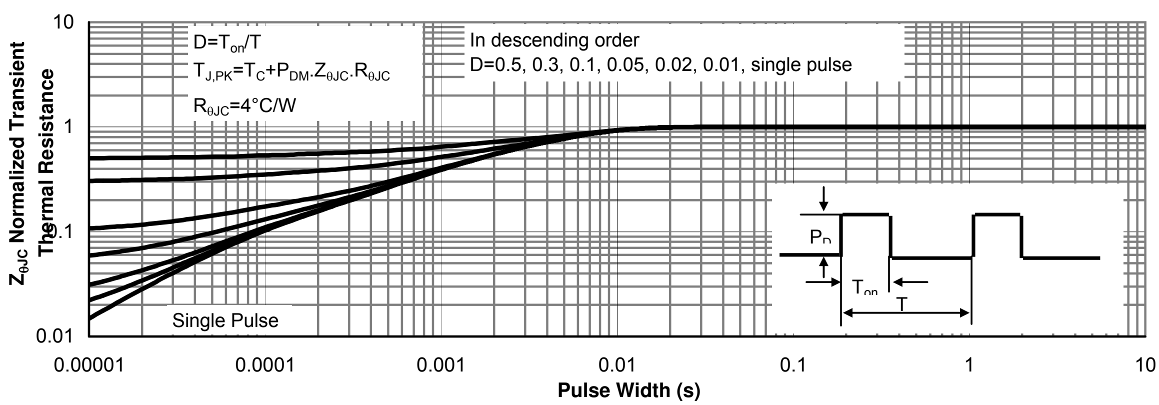


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

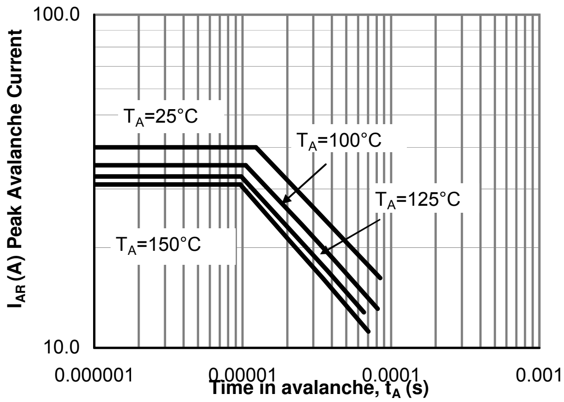


Figure 12: Single Pulse Avalanche capability (Note C)

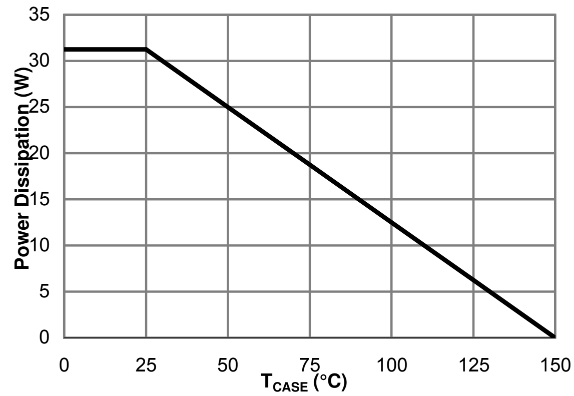


Figure 13: Power De-rating (Note F)

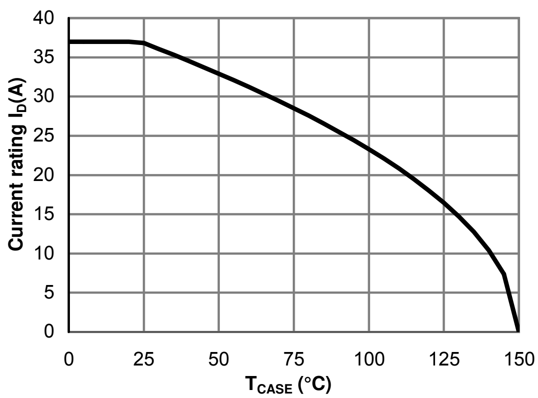


Figure 14: Current De-rating (Note F)

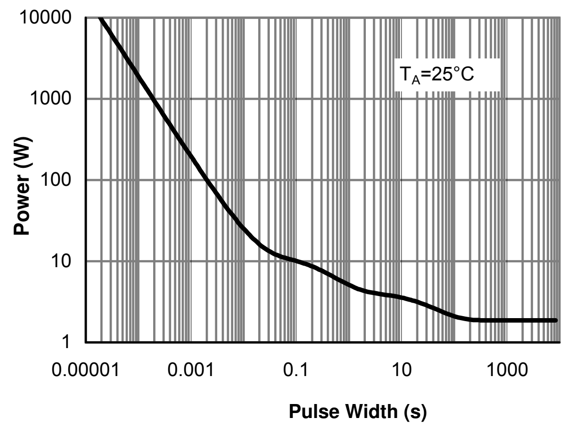


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

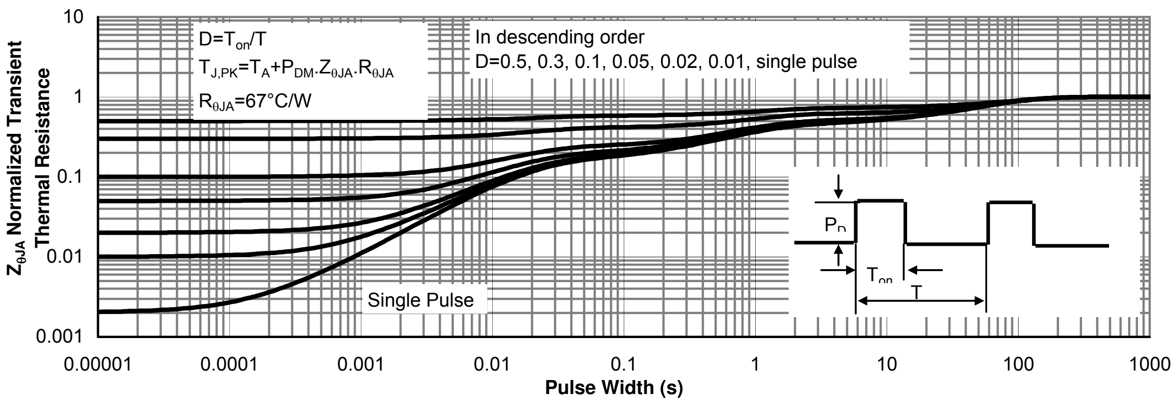


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1.3	1.8	2.3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=10A			9.7	11.7	mΩ
			T_J=125°C		15.1	18.2	
		V_{GS}=4.5V, I_D=10A			14	17.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A			25		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.72	1	V
I_S	Maximum Body-Diode Continuous Current					48	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		450	570	750	pF
C_{oss}	Output Capacitance			180	260	370	pF
C_{rss}	Reverse Transfer Capacitance			12	20	35	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.9	1.8	2.7	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=10A		6.5	8.2	10	nC
Q_g(4.5V)	Total Gate Charge			2.8	3.5	4.2	nC
Q_{gs}	Gate Source Charge			1.2	1.6	2	nC
Q_{gd}	Gate Drain Charge			0.8	1.4	2	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			4.1		ns
t_r	Turn-On Rise Time				7.8		ns
$t_{D(off)}$	Turn-Off DelayTime				15.2		ns
t_f	Turn-Off Fall Time				3.3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=500A/µs		6.8	8.6	10	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10A, dI/dt=500A/µs		11.3	14.1	17	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by package.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

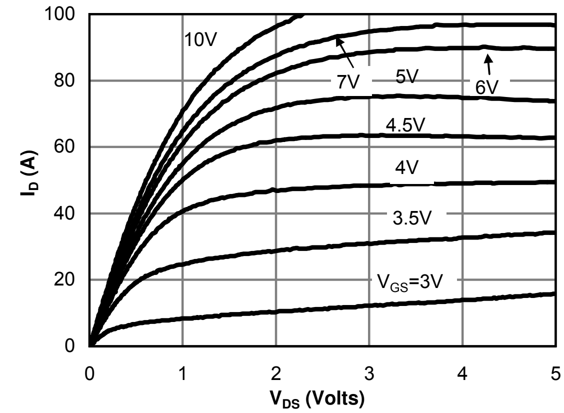


Fig 1: On-Region Characteristics (Note E)

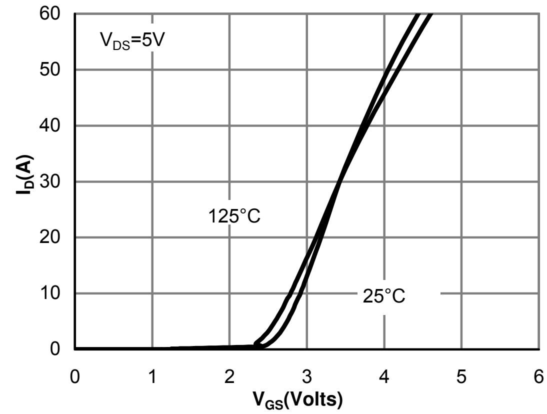


Figure 2: Transfer Characteristics (Note E)

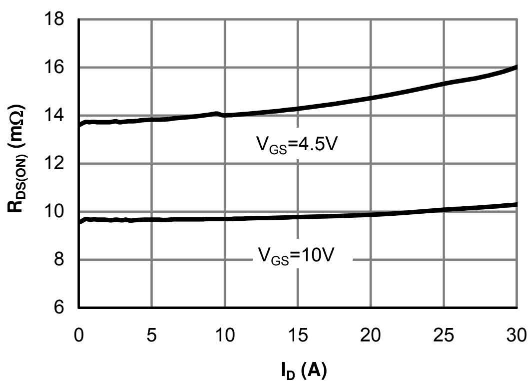


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

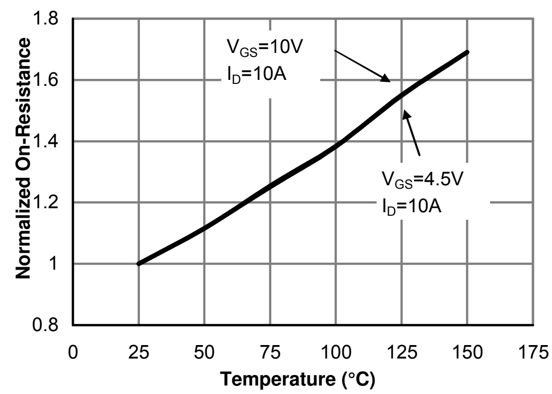


Figure 4: On-Resistance vs. Junction Temperature (Note E)

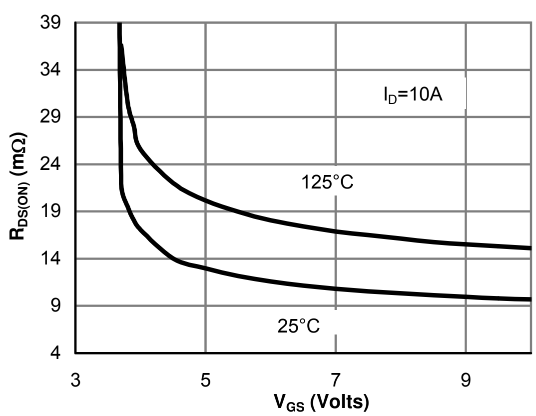


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

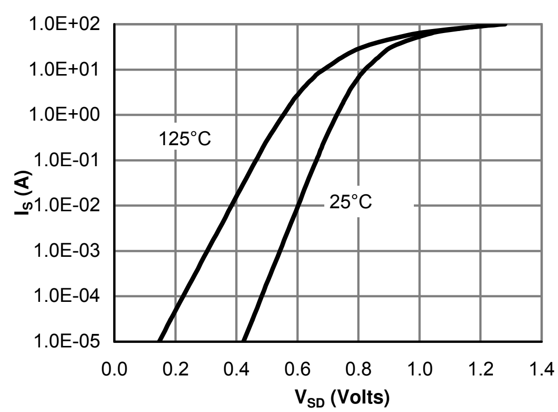


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

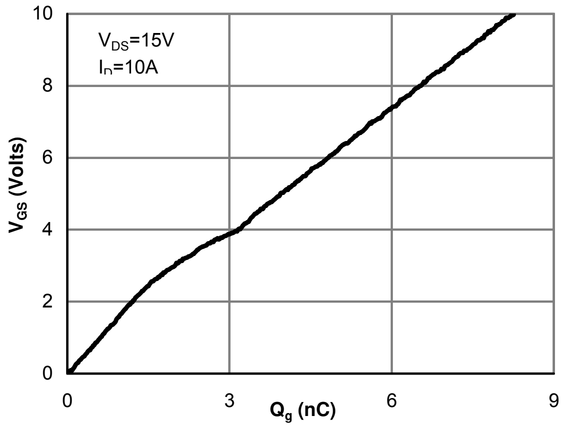


Figure 7: Gate-Charge Characteristics

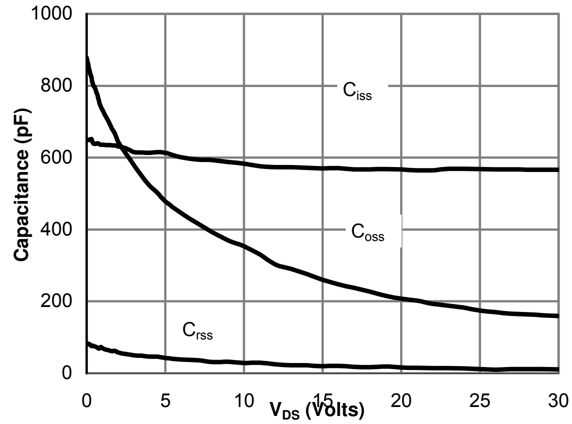


Figure 8: Capacitance Characteristics

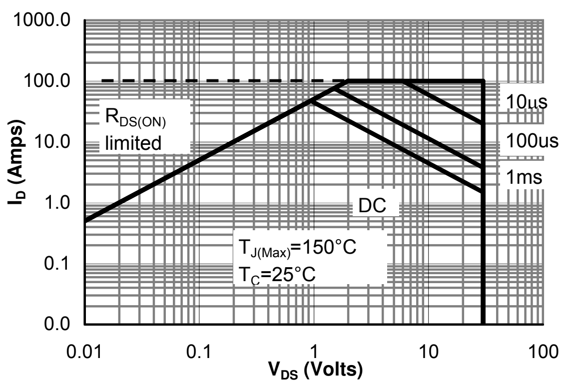


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

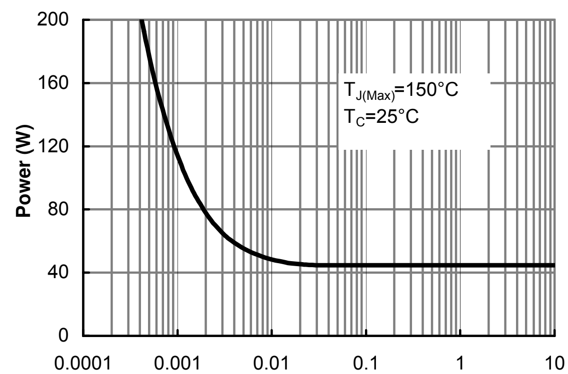


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

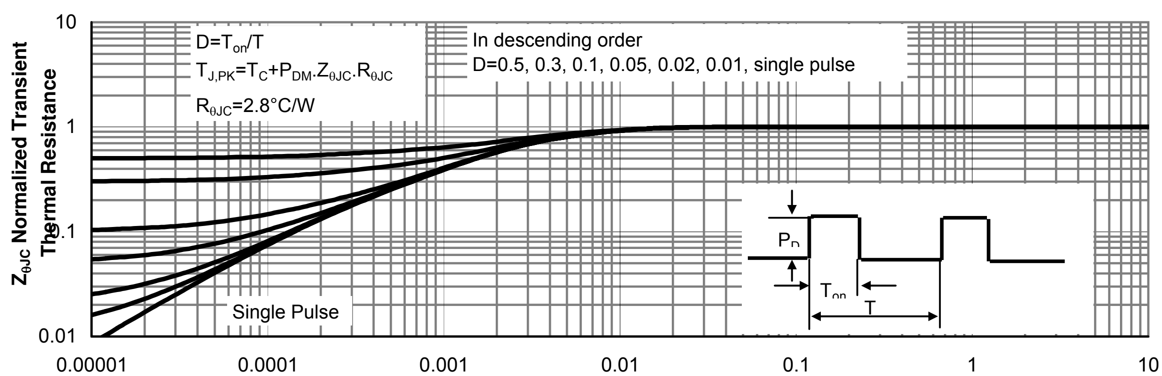


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

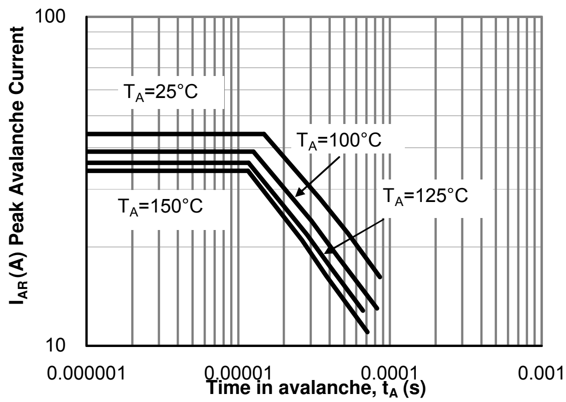


Figure 12: Single Pulse Avalanche capability (Note C)

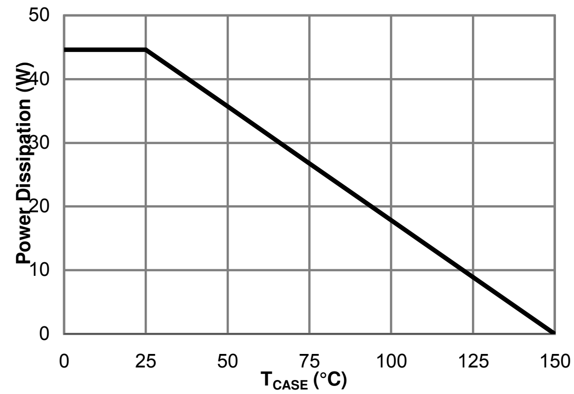


Figure 13: Power De-rating (Note F)

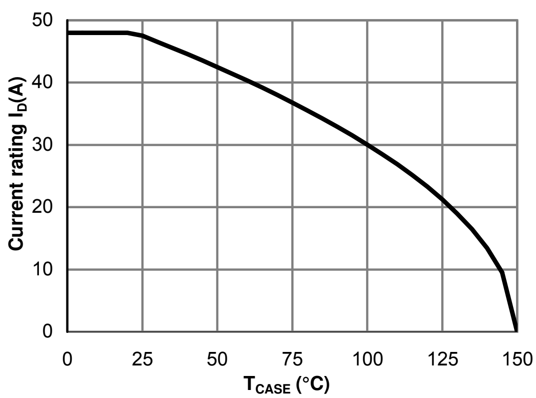


Figure 14: Current De-rating (Note F)

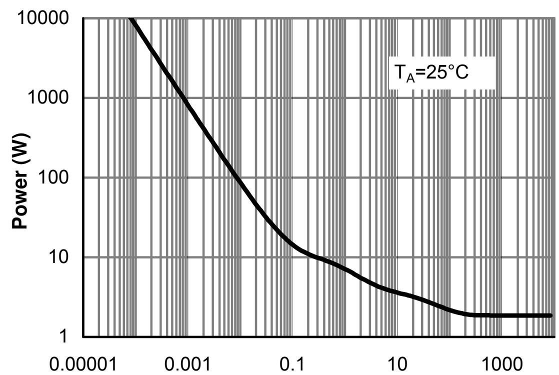


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

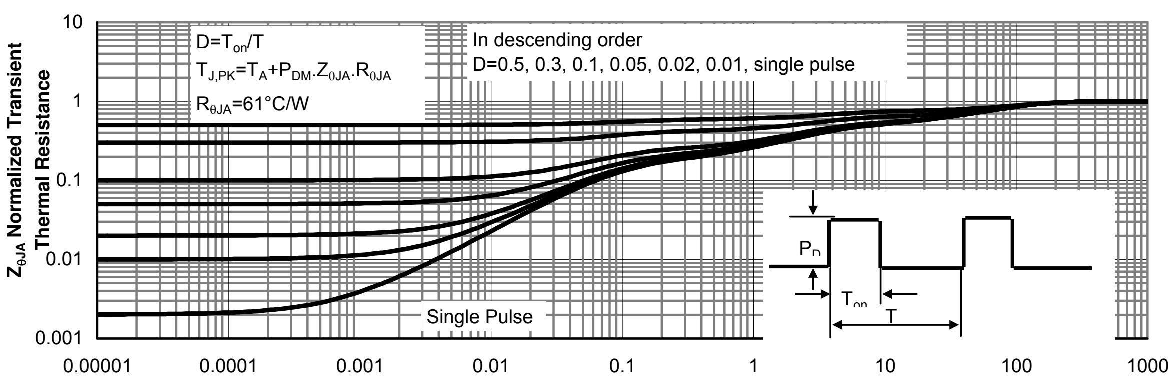
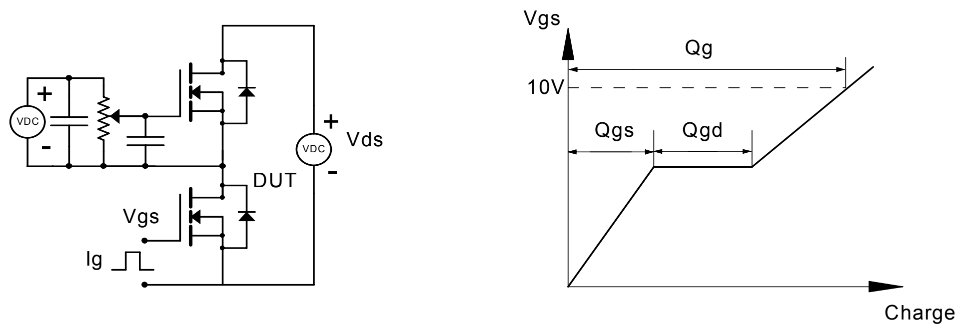
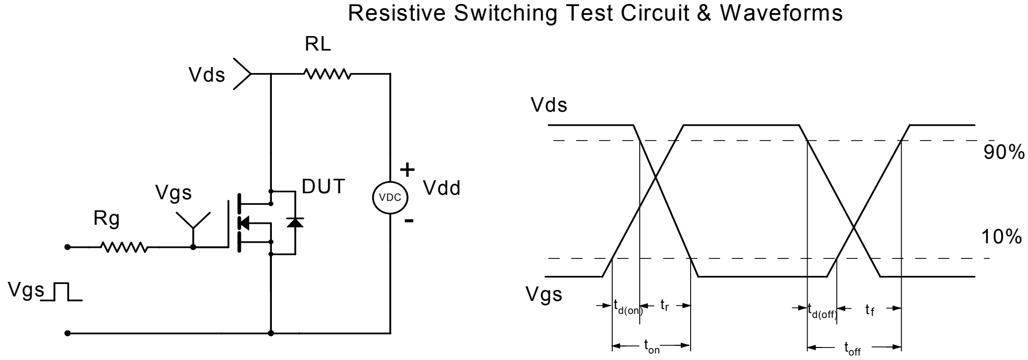


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

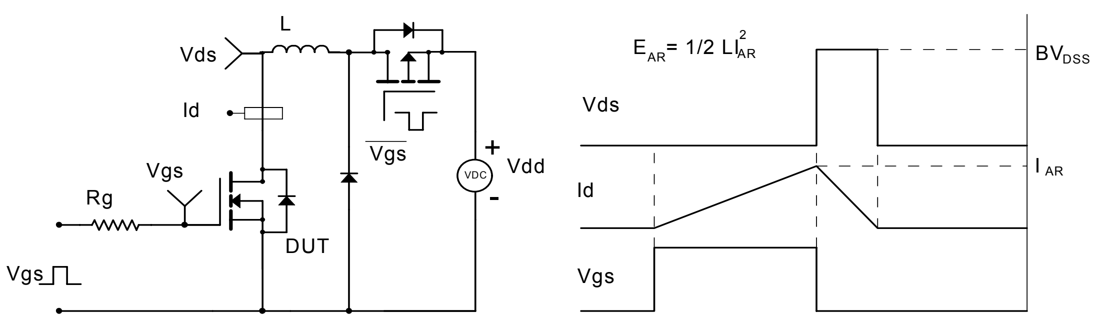
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms