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NL3HS3124A

3.3 V, 2 Channel, 2:1 Differential Mux/Demux

The NL3HS3124A is a 2 channel, 2-to-1 differential multiplexer / demultiplexer for USB 3.0, PCI Express Generation 3, or other high-speed serial interface applications. The NL3HS3124A can switch two differential signals to one of two locations. The device has minimal channel-to-channel skew as well as minimal channel-to-channel crosstalk, making the device ideal for high-speed serial interface applications.

Features

- 2 Bidirectional Channel, 2 : 1 Differential Multiplexer/Demultiplexer
- High-speed Signal Switching for 8 Gbps Applications
- High Bandwidth: > 6.3 GHz at -3 dB
- Low Insertion Loss:
 - ◆ -0.5 dB at 100 MHz
 - ◆ -2.8 dB at 4.0 GHz
- Low Return Loss: -9.27 dB at 4 GHz
- Low Crosstalk: -35 dB at 4 GHz
- Low Off-state Isolation: -19 dB at 4 GHz
- Low Intra-pair Skew: 5 ps Typical
- Low Inter-pair Skew: 35 ps Maximum
- V_{DD} Operating Range: 3.0 V to 3.6 V
- Shutdown Pin (SD) for Power-saving Mode
- Standby Current less than 1 μA
- ESD Tolerance:
 - ◆ 4000 V HBM
 - ◆ 300 V MM
 - ◆ 2000 V CDM
- 2.5 mm x 4.5 mm QFN20 Package
- This Device is Pb-Free, Halogen-Free/BFR-Free and is RoHS-Compliant

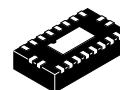
Applications

- Routing of High-speed Differential Signals
 - ◆ USB 3.0
 - ◆ PCIe Gen3
 - ◆ DisplayPort 1.2
 - ◆ SATA 6 Gbps



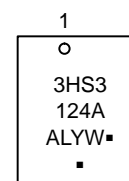
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QFN20
MN SUFFIX
CASE 485AA

MARKING DIAGRAM



3HS3124A = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|--------------------|-----------------------|
| NL3HS3124AMNTWG | QFN20 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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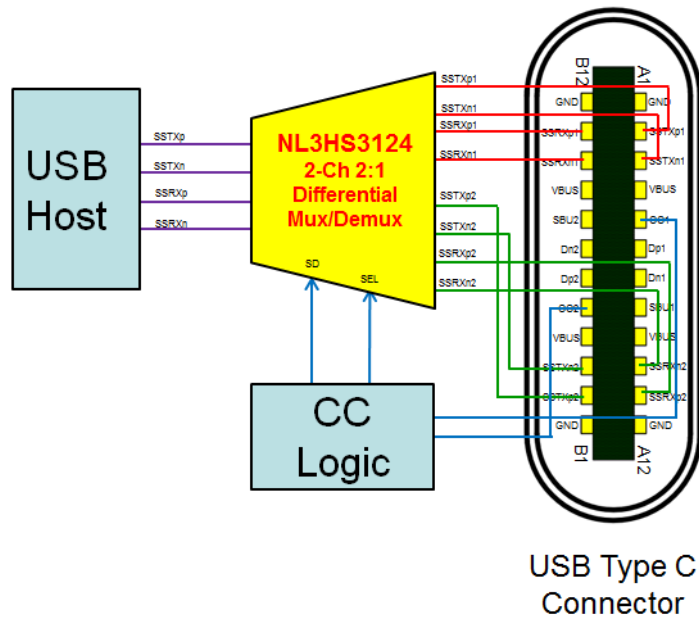


Figure 1. Typical Application

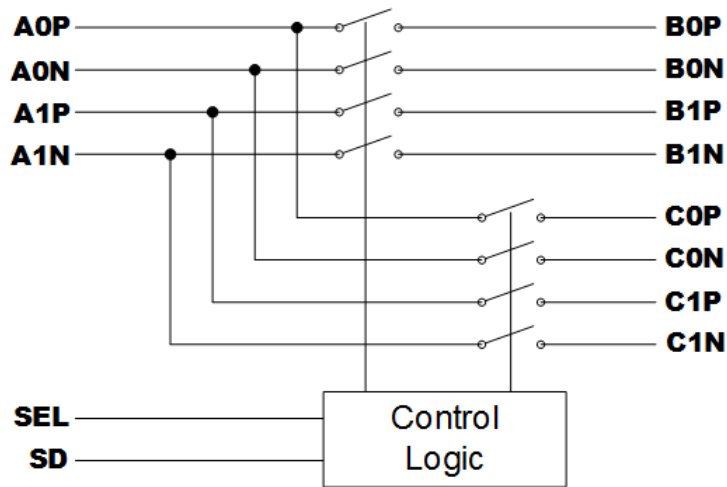


Figure 2. Block Diagram

Table 1. FUNCTION TABLE

| SD | SEL | Function |
|----|-----|---|
| L | L | An connected to Bn |
| L | H | An connected to Cn |
| H | X | An, Bn and Cn in Hi-Z, Device in Shutdown |

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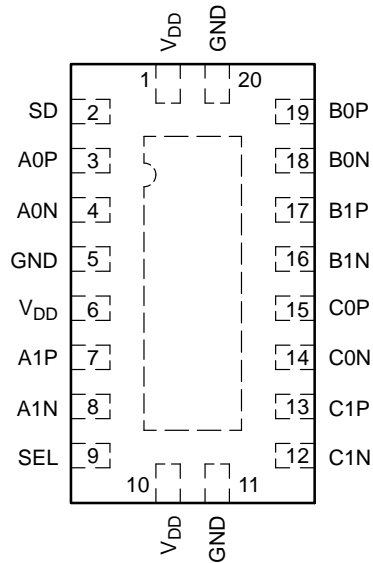


Figure 3. Pinout (Top Through View)

Table 2. PIN ASSIGNMENT

| Pin Name | Pin | Type | Description |
|-----------------|-----------------------|--------------|---|
| A0P | 3 | I/O | Channel 0, Port A Differential Signal I/O |
| A0N | 4 | I/O | |
| A1P | 7 | I/O | |
| A1N | 8 | I/O | |
| B0P | 19 | I/O | Channel 0, Port B Differential Signal I/O |
| B0N | 18 | I/O | |
| B1P | 17 | I/O | |
| B1N | 16 | I/O | |
| C0P | 15 | I/O | Channel 0, Port C Differential Signal I/O |
| C0N | 14 | I/O | |
| C1P | 13 | I/O | |
| C1N | 12 | I/O | |
| SEL | 9 | Input (CMOS) | Mux/Demux Select Pin |
| SD | 2 | Input (CMOS) | Shutdown Pin |
| V _{DD} | 1, 6, 10 | Power | Power |
| GND | 5, 11, 20, Center Pad | Power | Ground |

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Table 3. MAXIMUM RATINGS

| Symbol | Rating | Value | Unit | |
|-----------------|---|------------------------------|------|------|
| V _{DD} | Positive DC Supply Voltage | -0.5 to +4.6 | V | |
| V _{IN} | Digital Control Input Voltage (SEL, SD) | -0.5 to V _{DD} +0.5 | V | |
| T _s | Storage Temperature | -65 to +150 | °C | |
| ESD | ESD Performance | | V | |
| | HBM (JESD22-A114) | All Pins | | 4000 |
| | MM (JESD22-A115-A) | All Pins | | 300 |
| | CDM (JESD22-C101) | All Pins | | 2000 |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|---|-----|-----|-----------------|------|
| V _{DD} | Positive DC Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{IN} | Digital Control Input Voltage (SEL, SD) (Note 1) | 0 | | V _{DD} | V |
| V _{IS} | Differential Pin Input Voltage (An, Bn, Cn) | 0 | | 2.4 | V |
| V _{IC} | Common-Mode Input Voltage (An, Bn, Cn) | 0 | | 2 | V |
| V _{ID} | Differential Input Voltage (An, Bn, Cn), peak-to-peak | 0 | | 1.6 | V |
| T _A | Operating Temperature | -40 | | 85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Control input must be held High or Low. It must not float.

Table 5. DC ELECTRICAL CHARACTERISTICS

Voltages referenced to GND. All typical values are at T_A = 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = -40°C to +85°C | | | Unit |
|-----------------|------------------------------|---|---------------------|---------------------------------|-----|-----|------|
| | | | | Min | Typ | Max | |
| V _{IH} | Input Voltage High | SEL, SD | 3.0 – 3.6 | 2.0 | | | V |
| V _{IL} | Input Voltage Low | SEL, SD | 3.0 – 3.6 | | | 0.5 | V |
| I _{IN} | Input Leakage Current | SEL, SD: V _{IN} = 0 V or V _{DD} | 3.6 | | | ±5 | μA |
| I _{IS} | Switch Input Leakage Current | An, Bn, Cn: V _{IS} = 0 V or 2.4 V | 3.6 | | | ±10 | μA |
| I _{DD} | Supply Current | Operating mode: SD = L | 3.6 | | 0.2 | 1 | mA |
| | | Shutdown mode: SD = H | 3.6 | | | 1 | μA |

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Table 6. DYNAMIC CHARACTERISTICS Voltages referenced to GND. All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise specified.

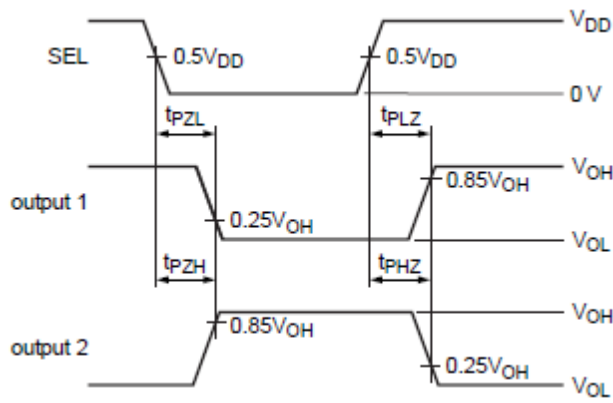
| Symbol | Parameter | Condition | V_{CC} (V) | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | | Unit |
|--------------|-----------------------------------|--|--------------|---|-------|-----|----------|
| | | | | Min | Typ | Max | |
| DDIL | Differential Insertion Loss | Channel OFF | 3.0 – 3.6 | | | | dB |
| | | f = 4 GHz | | | -19 | | |
| | | f = 100 MHz | | | -47 | | |
| | | Channel ON | | | | | |
| | | f = 4 GHz | | | -2.8 | | |
| | | f = 100 MHz | | | -0.5 | | |
| DDNEXT | Differential Near-End Crosstalk | Adjacent Channels ON | 3.0 – 3.6 | | | | dB |
| | | f = 4 GHz | | | -26 | | |
| | | f = 100 MHz | | | -62 | | |
| BW | -3 dB Bandwidth | | 3.0 – 3.6 | | 6.3 | | GHz |
| DDRL | Differential Return Loss | f = 4 GHz | 3.0 – 3.6 | | -9.27 | | dB |
| | | f = 100 MHz | | | -23.2 | | |
| R_{ON} | Switch ON Resistance (Note 2) | $V_{IS} = 2\text{ V}, I_{IS} = 19\text{ mA}$ | 3.3 | | 6 | | Ω |
| $C_{IO(ON)}$ | ON-State Input/Output Capacitance | f = 2.5 GHz | 3.0 – 3.6 | | 2.03 | | pF |

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltage on the two (A or B ports).

Table 7. SWITCHING CHARACTERISTICS All typical values are for $V_{CC} = 3.3\text{ V}$ at $T_A = 25^\circ\text{C}$ unless otherwise specified.

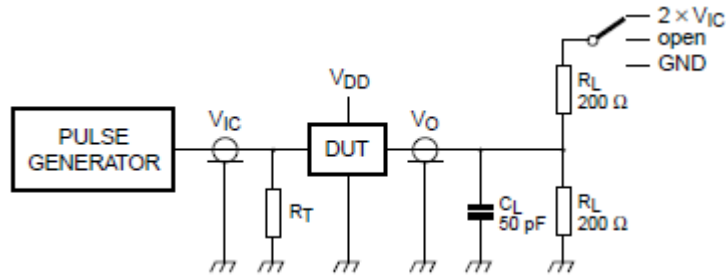
| Symbol | Parameter | Condition | V_{CC} (V) | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | | Unit |
|---------------|-------------------------------------|---|--------------|---|-----|-----|------|
| | | | | Min | Typ | Max | |
| $t_{STARTUP}$ | Startup Time | Supply Voltage Valid, or SD going Low to channel specified operating conditions | 3.0 – 3.6 | | | 10 | ms |
| t_{PD} | Propagation Delay | Port A to Port B or C, or vice-versa | 3.0 – 3.6 | | 60 | | ps |
| t_{PZH} | OFF-State to High Propagation Delay | | 3.0 – 3.6 | | | 300 | ns |
| t_{PZL} | OFF-State to Low Propagation Delay | | 3.0 – 3.6 | | | 70 | ns |
| t_{PHZ} | High to OFF-State Propagation Delay | | 3.0 – 3.6 | | | 50 | ns |
| t_{PLZ} | Low to OFF-State Propagation Delay | | 3.0 – 3.6 | | | 50 | ns |
| $t_{sk(dif)}$ | Differential Skew | Intra-pair | 3.0 – 3.6 | | 5 | | ps |
| t_{sk} | Skew | Inter-pair | 3.0 – 3.6 | | | 35 | ps |

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Output 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
 Output 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
 The outputs are measured one at a time with one transition per measurement.

Figure 4. Voltage Waveforms, Enable and Disable Times



C_L = load capacitance; includes jig and probe capacitance.
 R_T = termination resistance; should be equal to Z_o of the pulse generator.
 All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 5$ MHz; $Z_o = 50 \Omega$; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns.

Figure 5. Test Circuit for Switching Times

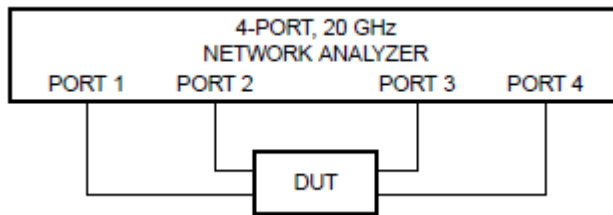


Figure 6. Test Circuit

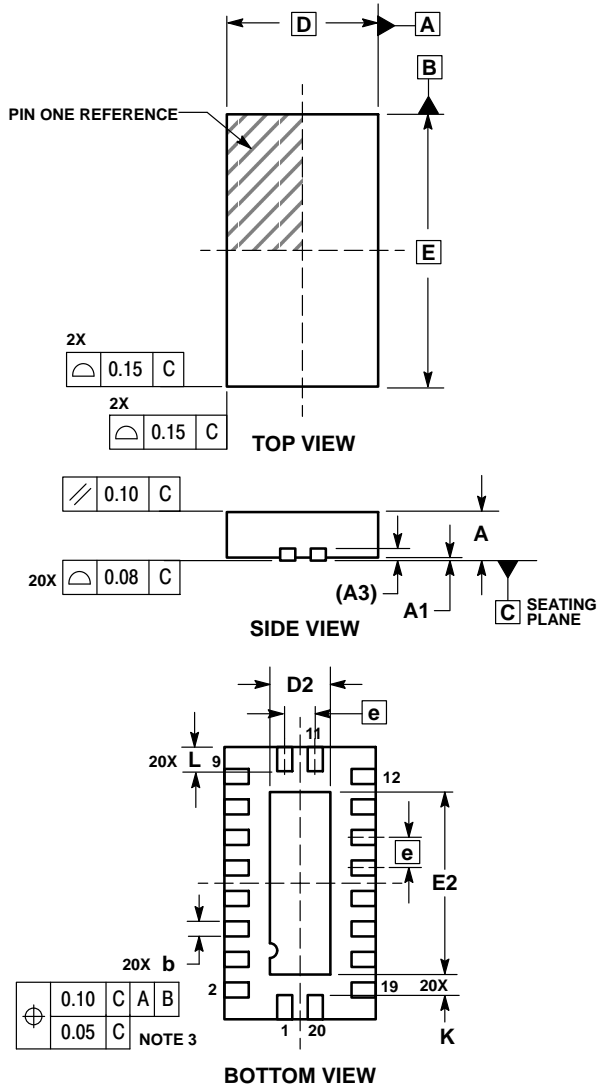
Table 8. LOADING CONDITIONS FOR SWITCHING/TIMING TESTS

| Test | Load | | Switch |
|--|-------|--------------|-------------------|
| | C_L | R_L | |
| t_{PLZ} , t_{PZL} (Output on B Side) | 50 pF | 200 Ω | $2 \times V_{IC}$ |
| t_{PHZ} , t_{PZH} (Output on B Side) | 50 pF | 200 Ω | GND |
| t_{PD} | | 200 Ω | Open |

NL3HS3124A

PACKAGE DIMENSIONS

QFN20, 2.5x4.5 MM
CASE 485AA
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 4.50 BSC | |
| E2 | 2.85 | 3.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

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