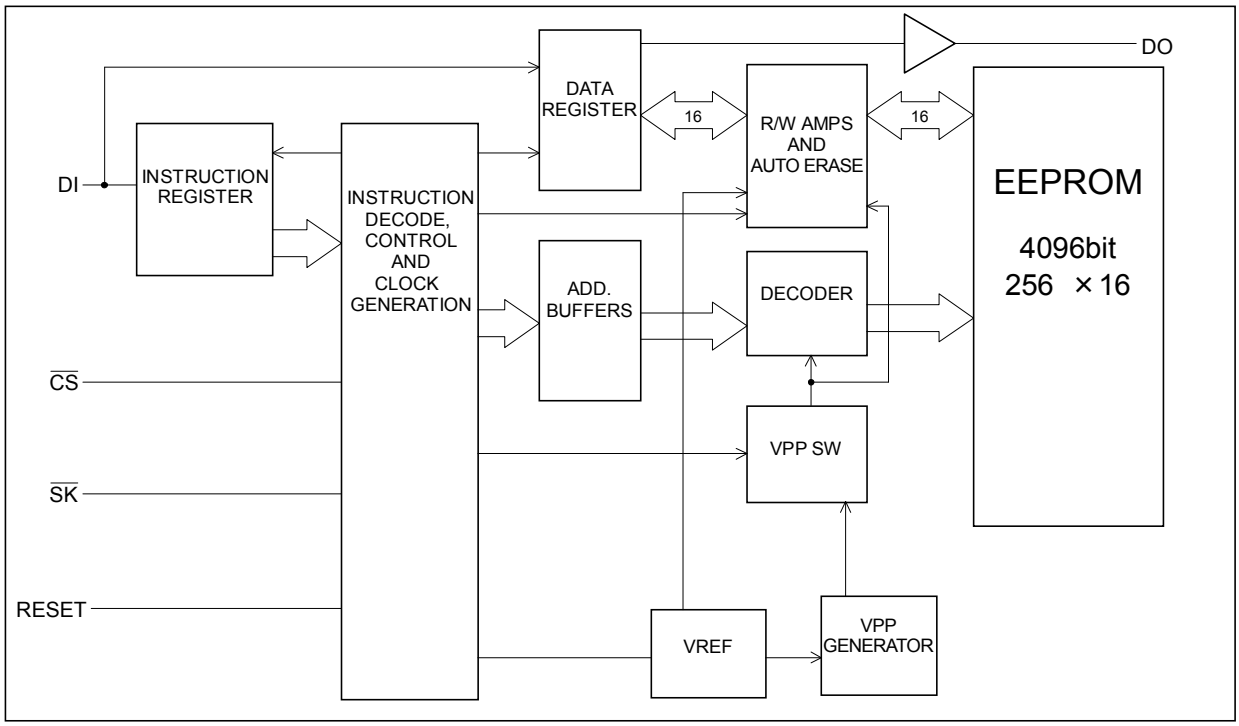
AK6440B

4096bit Serial CMOS EEPROM

Features

- ☐ ADVANCED CMOS EEPROM TECHNOLOGY
- ☐ Wide VCC (1.8V ~ 5.5V) operation
- ☐ 4096 bits: 256×16 organization
- ☐ ONE CHIP MICROCOMPUTER INTERFACE
  - Interface with one chip microcomputer's serial communication port directly
- ☐ LOW POWER CONSUMPTION
  - 0.75mA Max. (Read operation)
  - 0.8μA Max. (Standby mode)
- ☐ HIGH RELIABILITY
  - Endurance : 100K cycles
  - Data Retention : 10 years
- ☐ SPECIAL FEATURES
  - High speed operation (f_{MAX}=1MHz: VCC=2.5V)
  - Automatic write cycle time-out with auto-ERASE
  - Automatic address increment (READ)
  - Software and Hardware controlled write protection
- ☐ IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (MSOP, SON)



Block diagram

General Description

The AK6440B is a 4096bit, serial, read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. The AK6440B has 4096bits of memory organized into 256 registers of 16 bits each. The AK6440B can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.
The AK6440B can connect to the serial communication port of popular one chip microcomputer directly (3 line negative clock synchronous interface). At write operation, AK6440B takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin ($\overline{SK}$). And at read operation, AK6440B takes out the read data from a register to data output pin (DO) synchronously with falling edge of $\overline{SK}$.
The AK6440B has 4 instructions such as READ, WRITE, WREN (write enable) and WRDS (write disable). Each instruction is organized by op-code block (8bits), address block (8bits) and data (8bits×2). When input level of SK pin is high level and input level of chip select ($\overline{CS}$) pin is changed from high level to low level, AK6440B can receive the instructions.
Special features of the AK6440B include : automatic write time-out with auto-ERASE, Ready/$\overline{Busy}$ status signal output and ultra-low standby power mode when deselected ($\overline{CS}$=high).

・ Software and Hardware controlled write protection

The AK6440B has 2 (hardware and software) write protection functions.
After power on or after execution of WRDS (write disable) instruction, execution of WRITE instruction will be disabled. This write protection condition continues until WREN instruction is executed or VCC is removed from the part.
Execution of READ instruction is independent of both WREN and WRDS instructions.
Reset pin should be low level when WRITE instruction is executed. When the Reset pin is high level, the WRITE instruction is not executed.

・ Ready/$\overline{Busy}$ status signal

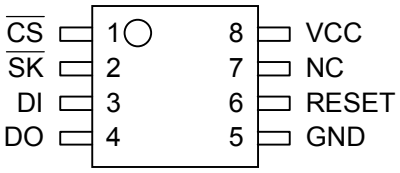
The DO pin indicates the $\overline{Busy}$ status. When input level of $\overline{SK}$ pin is low level and input level of $\overline{CS}$ pin is changed from high level to low level, the AK6440B is in the status output mode and the DO pin indicates the Ready/$\overline{Busy}$ status. The Ready/$\overline{Busy}$ status outputs on DO pin until $\overline{CS}$ pin is changed from low level to high level, or first bit ("1") of op-code of next instruction is given to the part. Except when the device is in the status output mode or outputs data, the DO pin is in the high impedance state.

■ Type of Products

Model	Memory Size	Temp.Range	VCC	Package
AK6440BH	4Kbits	-40°C ~ +85°C	1.8V ~ 5.5V	8pin Plastic MSOP
AK6440BL		-40°C ~ +85°C	1.8V ~ 5.5V	8 pin Plastic SON

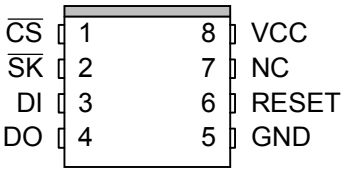
Pin Arrangement

AK6440BH



8pin MSOP

AK6440BL



8pin SON

Pin Name	Function
$\overline{CS}$	Chip Select
$\overline{SK}$	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
RESET	RESET Input
VCC	Power Supply
GND	Ground
NC	Not Connected *1

*1: Please Open NC pin.

Pin Description

$\overline{\text{CS}}$ (Chip Select)
When $\overline{\text{SK}}$ is high level and $\overline{\text{CS}}$ is changed from high level to low level, AK6440B can receive the instructions. $\overline{\text{CS}}$ should be kept low level while receiving op-code, address and data and while outputting data.
If $\overline{\text{CS}}$ is changed to high level during the above period, AK6440B stops the instruction execution.
When $\overline{\text{SK}}$ is low and $\overline{\text{CS}}$ is changed from high level to low level, AK6440B will be in status output mode. The $\overline{\text{CS}}$ need not be low level during the automatic write time-out period ($\overline{\text{BUSY}}$ status).

$\overline{\text{SK}}$ (Serial Clock)
The $\overline{\text{SK}}$ clock pin is the synchronous clock input for input/output data. At write operation, AK6440B takes in the write data from data input pin (DI) synchronously with rising edge of input pulse of serial clock pin ($\overline{\text{SK}}$). And at read operation, AK6440B takes out the read data to data output pin (DO) synchronously with falling edge of $\overline{\text{SK}}$. The SK clock is not needed during the automatic write time-out period ($\overline{\text{BUSY}}$ status), the status output period and when the device isn't selected ($\overline{\text{CS}}$ = high level).

DI (Data Input)
The op-code, address and write data is input to the DI pin.

DO (Data Output)
The DO pin outputs the read data and status signal and will be high impedance except for this timing.

RESET (Reset)
The AK6440B stops executing the write instruction when the RESET pin is high level. The RESET pin should be low level while the write instruction input period and the automatic write time-out period. If the RESET pin is high level while the automatic write time-out period, the AK6440B stops execution of internal programming and the device returns to ready status. In this case the word data of the specified address will be incomplete. When inputting the new instruction after RESET, the $\overline{\text{CS}}$ pin should be set to high level. The read, write enable and write disable instructions are not affected by RESET pin status.

VCC (Power Supply)

GND (Ground)

Functional Description

The AK6440B has 4 instructions such as READ, WRITE, WREN (write enable) and WRDS (write disable). Each instruction is organized by op-code block (8bits), address block (8bits) and data (8bits×2). When input level of $\overline{SK}$ pin is high level and input level of chip select ($\overline{CS}$) pin is changed from high level to low level, AK6440B can receive the instructions.
When the instructions are executed consecutively, the $\overline{CS}$ pin should be brought to high level for a minimum of 250ns(tCS) between consecutive instruction cycle.

■ Instruction Set

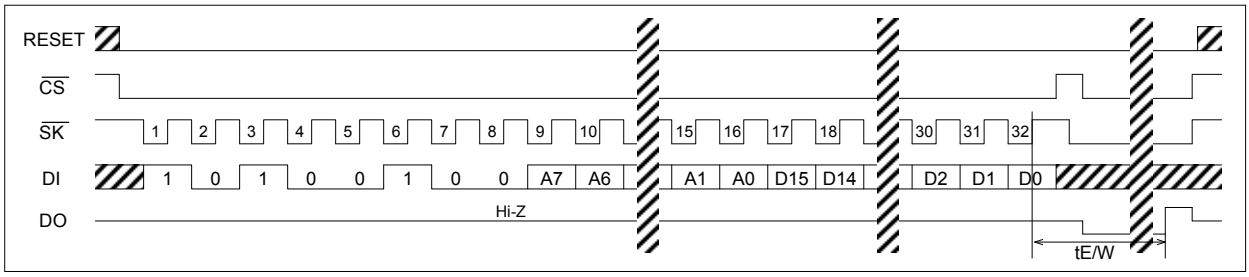
Instruction	Op-Code	Address	Data
WRITE	10100100	A7 A6 A5 A4 A3 A2 A1 A0	D15-D0(IN)
READ	10101000	A7 A6 A5 A4 A3 A2 A1 A0	D15-D0(OUT)
WREN	10100011	X X X X X X X X	
WRDS	10100000	X X X X X X X X	
(WRAL)	10101111	X X X X X X X X	D15-D0(IN)

X: don't care

(Note) The WRAL instruction is used for factory function test only. User can't use this instruction.

Write

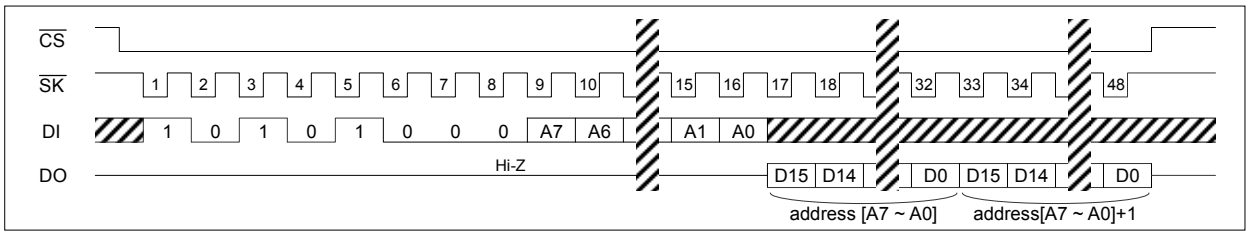
The write instruction is followed by 16 bits of data to be written into the specified address. After the 32nd rising edge of $\overline{SK}$ to read D0 in, the AK6440B will be put into the automatic write time-out period. During the automatic write time-out period ($\overline{Busy}$ status) and while entering write instruction, the RESET pin should be low level. If the RESET pin is set to high level during the automatic write time-out period, the AK6440B stops execution of internal programming and the device returns to ready status. In this case the word data of the specified address will be incomplete. When inputting the new instruction after RESET, the $\overline{CS}$ pin should be set to high level. When the RESET pin is kept at high level, the write is not executed. This becomes write protection function.
The $\overline{CS}$ pin need not be high level during automatic write time-out period ($\overline{BUSY}$ status).



WRITE

Read

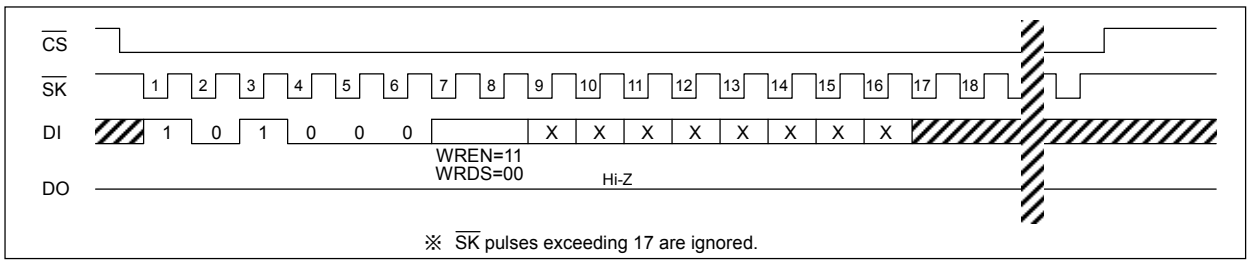
The read instruction is the only instruction which outputs serial data on the DO pin. When the 17th falling edge of $\overline{SK}$ is received, the DO pin will come out of high impedance state and shift out the data from D15 first in descending order which is located at the address specified in the instruction.
The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out.
When the highest address is reached ($FF), the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely.



READ

WREN / WRDS (Write Enable and Write Disable)

When VCC is applied to the part, it powers up in the programming disable (WRDS) state. Programming must be preceded by a programming enable (WREN) instruction.
Programming remains enabled until a programming disable (WRDS) instruction is executed or VCC is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is not affected by both WREN and WRDS instructions.



WREN / WRDS

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+7.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient Storage Temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(1.8V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V,tSKP=500ns *1		4.0	mA
	ICC2	VCC=2.5V,tSKP=500ns *1		2.5	mA
	ICC3	VCC=1.8V,tSKP=1.5μs *1		2.0	mA
Current Dissipation (READ, WREN, WRDS)	ICC4	VCC=5.5V,tSKP=500ns *1		0.75	mA
	ICC5	VCC=2.5V,tSKP=500ns *1		0.3	mA
	ICC6	VCC=1.8V,tSKP=1.5μs *1		0.15	mA
Current Dissipation (Standby)	ICCS	VCC=5.5V *2		0.8	μA
Input High Voltage1 $\overline{CS}$, $\overline{SK}$, RESET pin	VIH1	1.8V≤VCC≤5.5V	0.8×VCC	VCC+0.5	V
Input High Voltage2 DI pin	VIH2	2.5V≤VCC≤5.5V	0.7×VCC	VCC+0.5	V
	VIH3	1.8V≤VCC<2.5V	0.8×VCC	VCC+0.5	V
Input Low Voltage1 $\overline{CS}$, $\overline{SK}$, RESET pin	VIL1	1.8V≤VCC≤5.5V	0	0.2×VCC	V
Input Low Voltage2 DI pin	VIL2	2.5V≤VCC≤5.5V	0	0.3×VCC	V
	VIL3	1.8V≤VCC<2.5V	0	0.2×VCC	V
Output High Voltage	VOH1	2.5V≤VCC≤5.5V IOH=-50μA	VCC-0.3		V
	VOH2	1.8V≤VCC<2.5V IOH=-50μA	VCC-0.3		V
Output Low Voltage	VOL1	2.5V≤VCC≤5.5V IOL=1.0mA		0.4	V
	VOL2	1.8V≤VCC<2.5V IOL=0.1mA		0.4	V
Input Leakage	ILI	VCC=5.5V,VIN=5.5V		±1.0	μA
Output Leakage	ILO	VCC=5.5V,VOUT=5.5V $\overline{CS}$=VCC		±1.0	μA

*1 : VIN=VIH/VIL, DO=Open

*2 : $\overline{CS}$=VCC, $\overline{SK}$/DI/RESET=VCC/GND, DO=Open

(2) A.C. ELECTRICAL CHARACTERISTICS

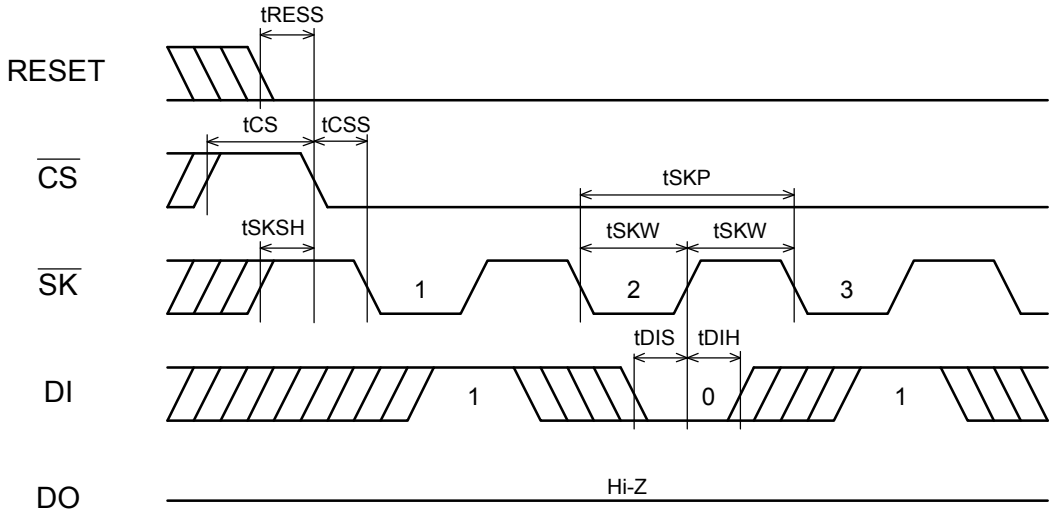
(1.8V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{SK}$ Cycle Time	tSKP1	2.5V≤VCC≤5.5V	500		ns
	tSKP2	1.8V≤VCC<2.5V	1.5		μs
$\overline{SK}$ Pulse Width	tSKW1	2.5V≤VCC≤5.5V	250		ns
	tSKW2	1.8V≤VCC<2.5V	750		ns
$\overline{SK}$ High Pulse Width	tSKH1	4.5V≤VCC≤5.5V	250		
	tSKH2	2.5V≤VCC<4.5V	500		
*3	tSKH3	1.8V≤VCC<2.5V	750		
$\overline{CS}$ Setup Time	tCSS		100		ns
$\overline{CS}$ Hold Time	tCSH		100		ns
$\overline{SK}$ Setup Time	tSKSH / tSKSL		100		ns
RESET Setup Time	tRESS		0		ns
Data Setup Time	tDIS1	4.5V≤VCC≤5.5V	100		ns
	tDIS2	1.8V≤VCC<4.5V	200		ns
Data Hold Time	tDIH1	4.5V≤VCC≤5.5V	100		ns
	tDIH2	1.8V≤VCC<4.5V	200		ns
DO pin Output delay	tPD1	4.5V≤VCC≤5.5V, *4		150	ns
	tPD2	2.5V≤VCC<4.5V, *4		300	ns
	tPD3	1.8V≤VCC<2.5V, *4		500	ns
Selftimed Programaing Time	tE/W			10	ms
Min $\overline{CS}$ High Time	tCS		250		ns
DO High-Z Time	tOZ			500	ns

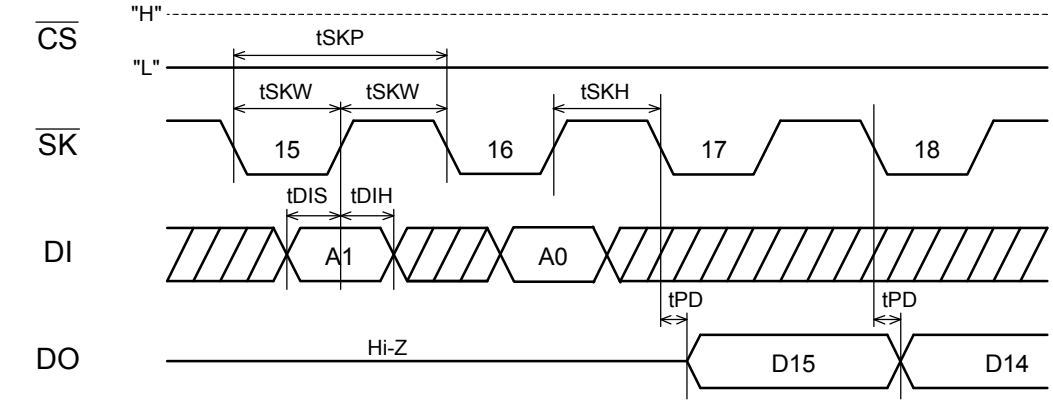
*3: tSKH is the high pulse width of 16th $\overline{SK}$ pulse in READ operation. When the data in the next address are read sequentially by continuing to provide clock, tSKH are applied to the high pulse width of 32nd and 48th (multiple of 16) SK pulse in READ operation.

*4: CL=100pF

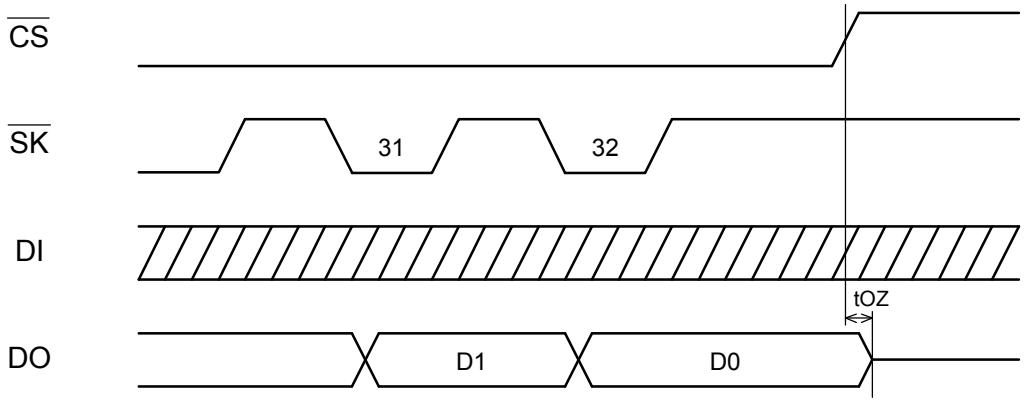
Synchronous Data Timing



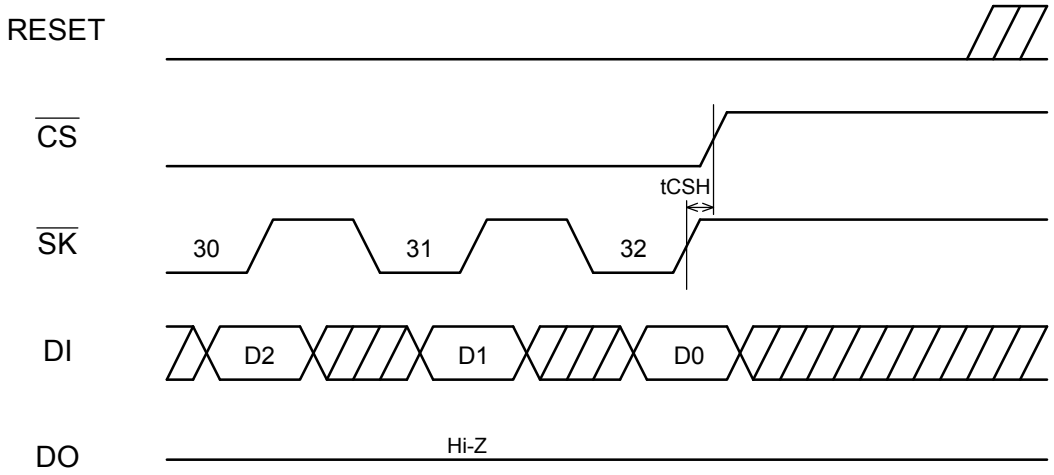
Instruction Input



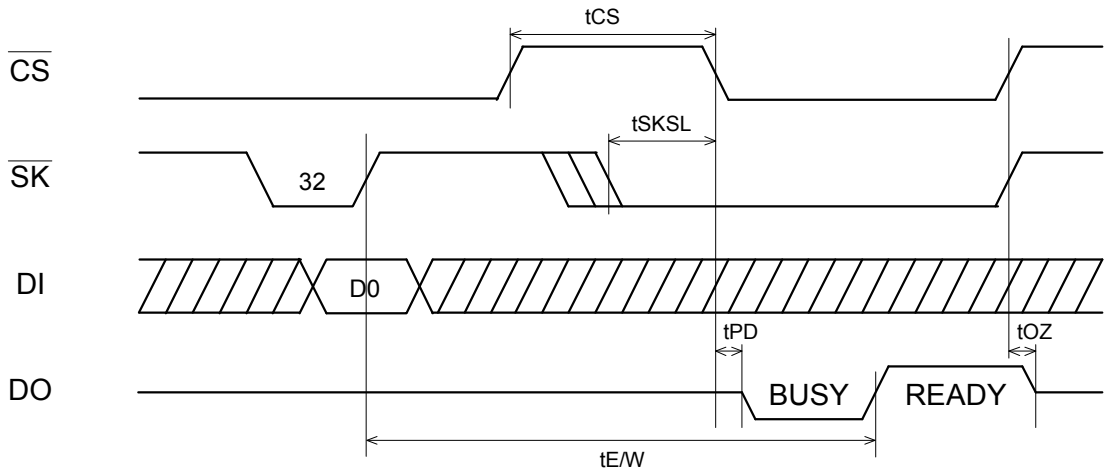
Data Output (READ)



Data Output (READ)



Data Input (WRITE)



Ready / $\overline{\text{BUSY}}$ Signal Output (DO pin)

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