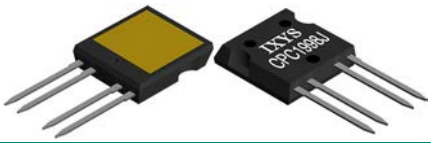
CPC1998J
AC Power Switch



Characteristics

Parameter	Rating	Units
AC Operating Voltage	20-240	V_{rms}
Load Current		
With 5°C/W Heat Sink	20	A_{rms}
No Heat Sink	5	
On-State Voltage Drop	1.1	V_P (at I_L=2A_P)
Blocking Voltage	800	V_P
Thermal Impedance, Junction-to-Case, θ_{JC}	0.35	°C/W

Features

- Load Current up to 20A_{rms} with 5°C/W Heat Sink
- 800V_P Blocking Voltage
- 5mA Control Current
- Zero-Cross Switching
- Isolated, Low Thermal Impedance Ceramic Pad for Heat Sink Applications
- 2500V_{rms} Isolation, Input to Output
- DC Control, AC Output
- Optically Isolated
- Low EMI and RFI Generation
- High Noise Immunity
- Flammability Rating UL 94 V-0

Applications

- Programmable Control
- Process Control
- Power Control Panels
- Remote Switching
- Gas Pump Electronics
- Contactors
- Large Relays
- Solenoids
- Motors
- Heaters

Approvals

- UL 508 Recognized Component: File E69938

Description

CPC1998J is an AC Solid State Switch utilizing dual power SCR outputs. This device also includes zero-cross turn-on circuitry and is specified with an 800V_P blocking voltage.

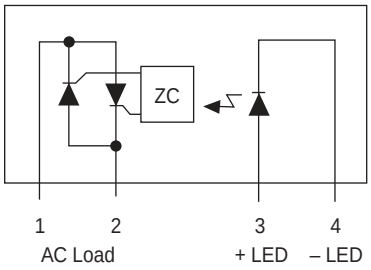
Tightly controlled zero-cross circuitry ensures low noise switching of AC loads by minimizing the generation of transients. The optically coupled input and output circuits provide exceptional noise immunity and 2500V_{rms} of isolation between the control and the output. As a result, the CPC1998J is well suited for industrial environments where electromagnetic interference would disrupt the operation of plant facility communications and control systems.

The unique i4-PAC package pioneered by IXYS allows Solid State Relays to achieve the highest load current and power ratings. This package features a unique IXYS process in which the silicon chips are soft soldered onto the Direct Copper Bond (DCB) substrate instead of the traditional copper leadframe. The DCB ceramic, the same substrate used in high power modules, not only provides 2500V_{rms} isolation but also very low junction-to-case thermal impedance (0.35 °C/W).

Ordering Information

Part	Description
CPC1998J	i4-PAC Package (25 per tube)

Pin Configuration



1 Specifications

1.1 Absolute Maximum Ratings @ 25°C

Symbol	Min	Max	Units
Blocking Voltage	-	800	V_P
Reverse Input Voltage	-	5	V
Input Control Current	-	50	mA
Peak (10ms)	-	1	A
Input Power Dissipation [1]	-	150	mW
Total Power Dissipation [2]	-	3.5	W
I^2t for Fusing (1/2 Sine Wave, 60Hz)	-	200	A^2S
Isolation Voltage, Input to Output	-	2500	V_{rms}
ESD, Human Body Model	-	8	kV
Operational Temperature	- 40	+85	°C
Storage Temperature	- 40	+125	°C

[1] Derate linearly 1.33mW / °C.

[2] Free air, no heat sink.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

1.2 Electrical Characteristics @ 25°C

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Output Characteristics						
Load Current						
Continuous	No Heat Sink, V_L=20-240V_{rms}	I_L	0.1	-	5	A_{rms}
Continuous	T_C=25°C		0.1	-	50	
Maximum Surge Current	1/2 Sine Wave, 60Hz	I_P	-	-	150	A
Off-State Leakage Current	V_L=800V	I_{LEAK}	-	-	100	μA_P
On-State Voltage Drop [1]	I_L=2A_P	-	-	0.85	1.1	V_P
Off-State dV/dt	I_F=0mA	dV/dt	1000	-	-	V/µs
Switching Speeds						
Turn-On	I_F=5mA	t_{on}	-	-	0.5	cycles
Turn-Off		t_{off}	-	-	0.5	
Zero-Cross Turn-On Voltage [2]	1st half-cycle	-	-	5	20	V
	subsequent half-cycle	-	-	-	5	
Holding Current	-	I_H	-	44	50	mA
Latching Current	-	I_L	-	48	75	mA
Operating Frequency	-	-	20	-	500	Hz
Load Power Factor for Guaranteed Turn-On [3]	f=60Hz	PF	0.25	-	-	-
Input Characteristics						
Input Control Current to Activate [4]	I_L=1A Resistive, f=60Hz	I_F	-	-	5	mA
Input Dropout Voltage	-	-	0.8	-	-	V
Input Voltage Drop	I_F=5mA	V_F	0.9	1.2	1.5	V
Reverse Input Current	V_R=5V	I_R	-	-	10	µA
Input/Output Characteristics						
Capacitance, Input-to-Output	V_{IO}=0V, f=1MHz	C_{IO}	-	-	3	pF

[1] Tested at a peak value equivalent.
[2] Zero-cross first half-cycle @ < 100Hz.
[3] Snubber circuits may be required at low power factors.
[4] For high-noise environments, or high-frequency operation (>60Hz), or for applications with a high inductive load, a minimum LED drive current of 10mA is recommended.

2 Thermal Characteristics

Parameter	Conditions	Symbol	Rating	Units
Thermal Impedance (Junction to Case)	-	θ_{JC}	0.35	°C/W
Thermal Impedance (Junction to Ambient)	Free Air	θ_{JA}	33	°C/W
Junction Temperature (Operating)	-	T_J	-40 to +125	°C

2.1 Thermal Management

Device high current characterization was performed using Kunze heat sink KU 1-159, phase change thermal interface material KU-ALC 5, and transistor clip KU 4-499/1. This combination provided an approximate junction-to-ambient thermal impedance of 12.5°C/W.

2.2 Heat Sink Calculation

Higher load currents are possible by using lower thermal impedance heat sink combinations.

Heat Sink Rating

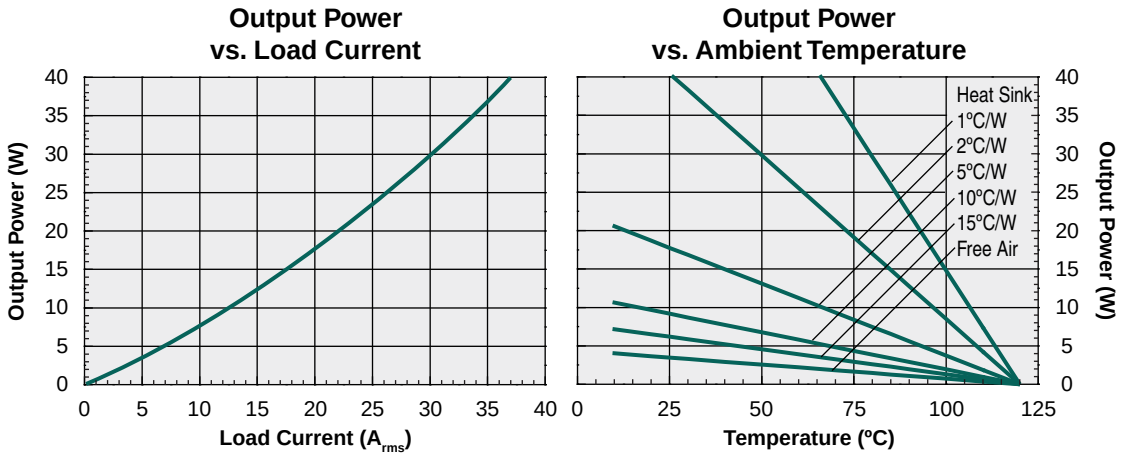
$$\theta_{CA} = \frac{(T_J - T_A)}{P_D} - \theta_{JC}$$

T_J = Junction Temperature (°C), $T_J \leq 125°C$ *
T_A = Ambient Temperature (°C)
θ_{JC} = Thermal Impedance, Junction to Case (°C/W) = 0.35°C/W
θ_{CA} = Thermal Impedance of Heat Sink & Thermal Interface Material , Case to Ambient (°C/W)
P_D = On-State Voltage (V_{rms}) • Load Current (A_{rms})

* Elevated junction temperature reduces semiconductor lifetime.

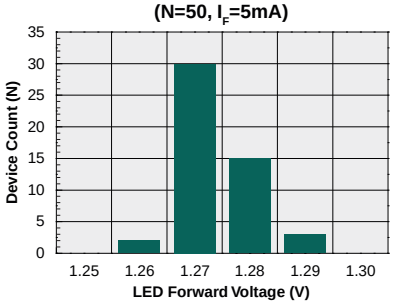
NOTE: The exposed surface of the DCB substrate is not to be soldered.

2.3 Thermal Performance Data

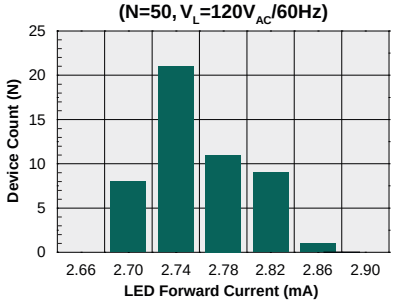


3 Performance Data*

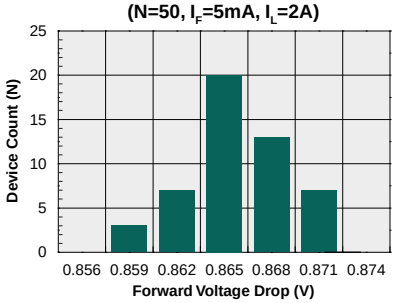
Typical LED Forward Voltage Drop
(N=50, I_F=5mA)



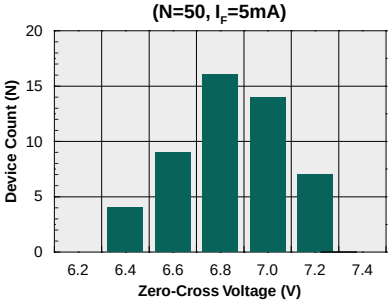
Typical I_F for Switch Operation
with 1A Resistive Load
(N=50, V_L=120V_{AC}/60Hz)



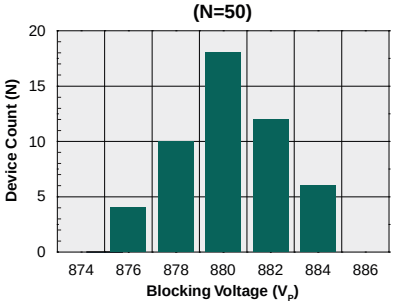
Forward Voltage Drop Distribution
(N=50, I_F=5mA, I_L=2A)



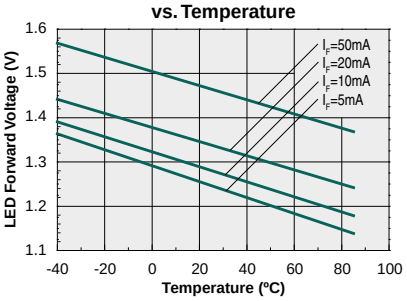
Zero-Cross Voltage
(N=50, I_F=5mA)



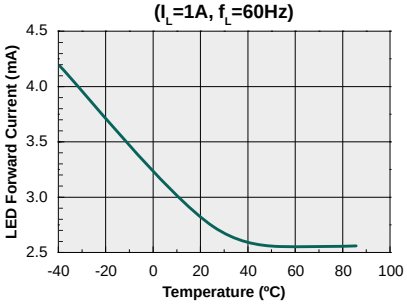
Typical Blocking Voltage Distribution
(N=50)



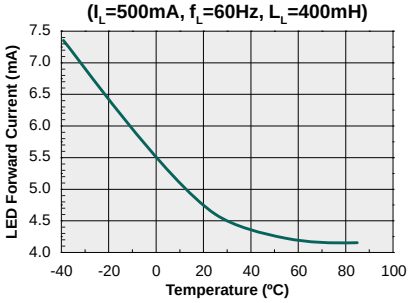
Typical LED Forward Voltage Drop
vs. Temperature



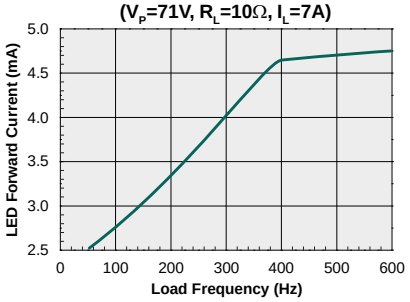
LED Forward Current to Operate
vs. Temperature - Resistive Load
(I_L=1A, f_L=60Hz)



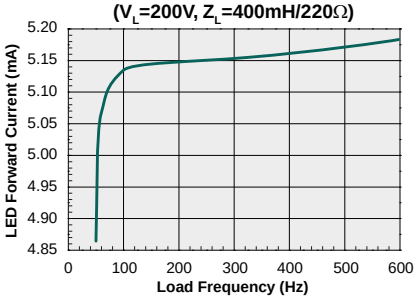
LED Forward Current to Operate
vs. Temperature - Inductive Load
(I_L=500mA, f_L=60Hz, L_L=400mH)



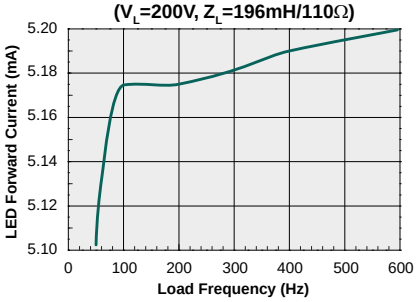
LED Current to Operate
vs. Load Frequency - Resistive Load
(V_P=71V, R_L=10Ω, I_L=7A)



LED Current to Operate
vs. Load Frequency - Inductive Load
(V_L=200V, Z_L=400mH/220Ω)

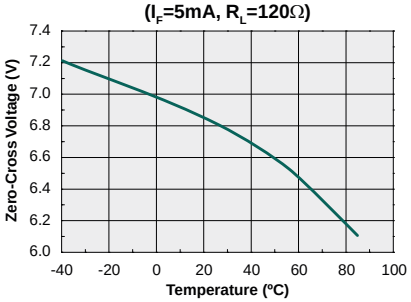


LED Current to Operate
vs. Load Frequency- Inductive Load
(V_L=200V, Z_L=196mH/110Ω)

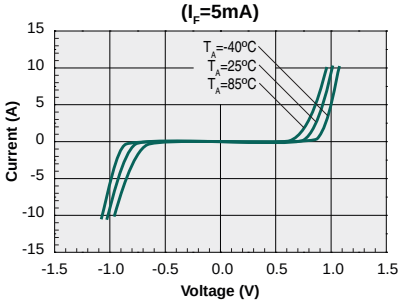


*Unless otherwise noted, data presented in these graphs is typical of device operation at 25ºC.

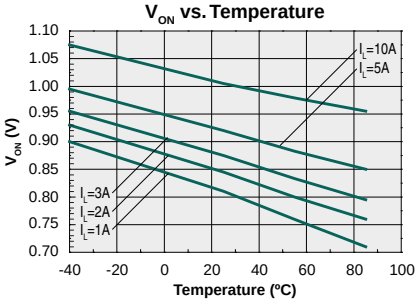
Zero-Cross Voltage vs. Temperature (I_F=5mA, R_L=120Ω)



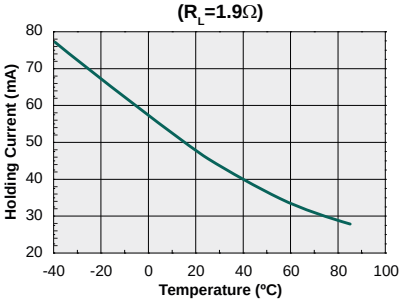
Output Voltage vs. Output Current (I_F=5mA)



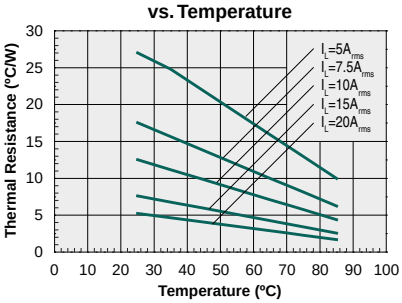
V_{ON} vs. Temperature



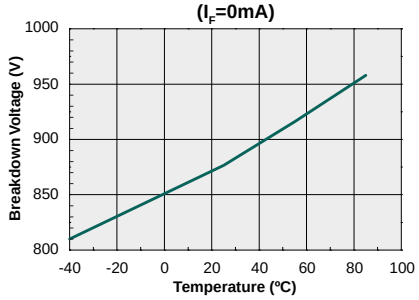
Holding Current vs. Temperature (R_L=1.9Ω)



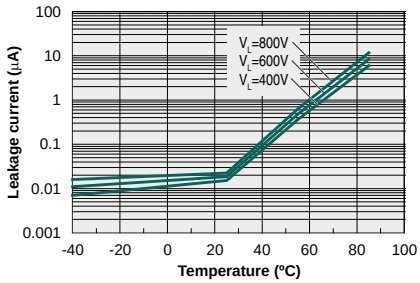
Total Heat Sinking Required vs. Temperature



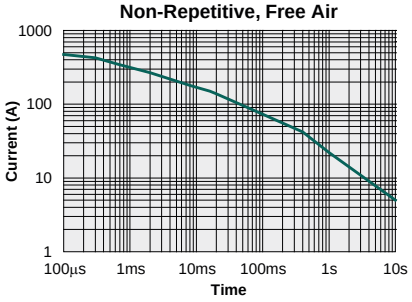
Breakdown Voltage vs. Temperature (I_F=0mA)



Leakage Current vs. Temperature Measured Across Pins 1&2



Maximum Surge Current Non-Repetitive, Free Air



*Unless otherwise noted, data presented in these graphs is typical of device operation at 25ºC.

4 Manufacturing Information

4.1 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.2 Soldering Profile

For through-hole devices, the maximum and minimum peak solder temperature limits (T_p) and the device maximum total dwell time through all solder waves is provided in the table below. Dwell time is the interval the device pins are at or above the minimum peak solder temperature. Body temperature of the device must not exceed the limit given in the table below at any time during the soldering process.

Device	Solder Temperature (T_p)		Body Temperature	Dwell Time	Wave Cycles
	Minimum	Maximum			
CPC1998J	235°C	260°C	245°C	10 seconds*	1

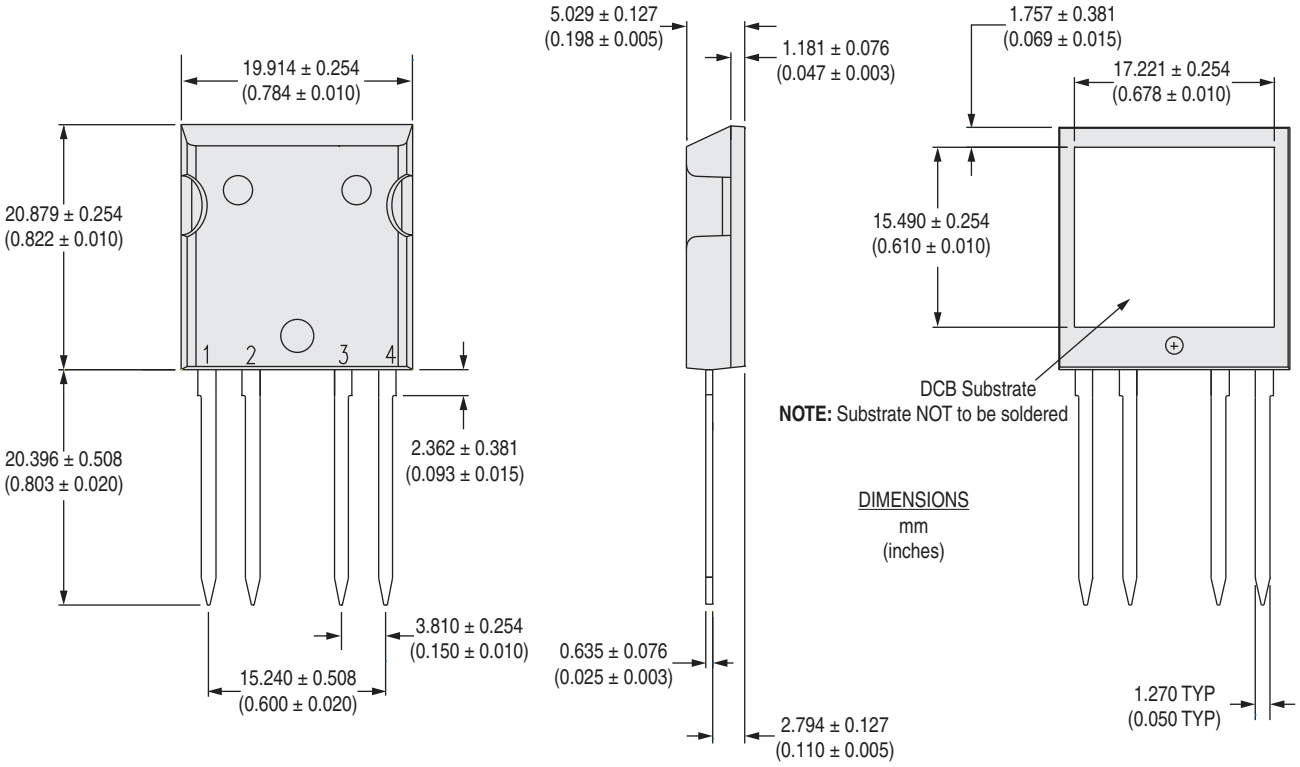
*Total cumulative duration of all waves.

NOTE: The exposed surface of the DCB substrate must not be soldered.

4.3 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

4.4 Mechanical Dimensions



NOTES:
1. Controlling dimension: Inches.
2. Metallized external surface of DCB substrate maintains 2500V_{rms} isolation to device internal structure and all external pins.

For additional information please visit our website at: https://www.ixysic.com

IXYS A Littelfuse Technology

Specification: DS-CPC1998J-R07

11/12/2020