

TLP2601

Isolated Line Receiver
 Simplex / Multiplex Data Transmission
 Computer-Peripheral Interface
 Microprocessor System Interface
 Digital Isolation for A/D, D/A Conversion
 Direct Replacement for HCPL-2601

The TOSHIBA TLP2601 a photocoupler which combines an IRED as the emitter and an integrated high gain, high speed photodetector. The output of the detector circuit is an open collector, Schottky clamped transistor.

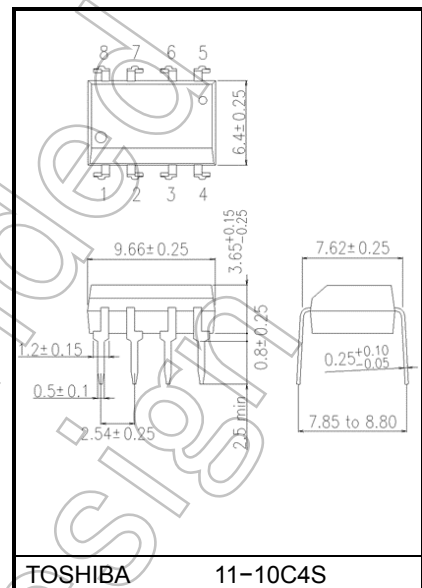
A Faraday shield integrated on the photodetector chip reduces the effects of capacitive coupling between the input LED emitter and the high gain stages of the detector. This provides an effective common mode transient immunity of 1000V/μs.

- Input current thresholds: $I_F = 5\text{mA}$ (max)
- Isolation voltage: 2500Vrms (min)
- Switching speed: 10MBd
- Common mode transient immunity: 1000V/μs (min)
- Guaranteed performance over temp.: 0°C to 70°C
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

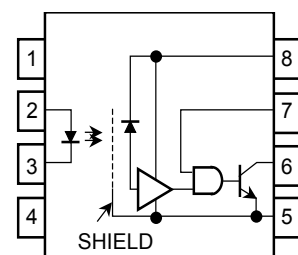
Truth Table (positive logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

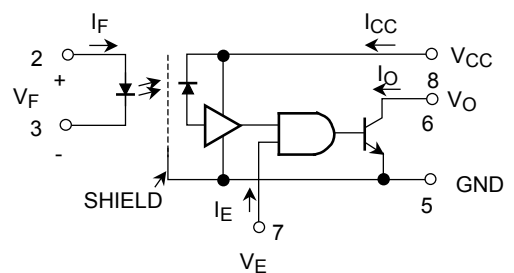
Unit: mm



Pin Configuration (top view)



Schematic



A 0.01 to 0.1μF bypass capacitor must be connected between pins 8 and 5 (see Note 1)

Start of commercial production
 1985-01

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, low level	I _{FL}	0	—	250	μA
Input current, high level	I _{FH}	6.3 (*)	—	20	mA
Supply voltage**, output	V _{CC}	4.5	—	5.5	V
High level enable voltage	V _{EH}	2.0	—	V _{CC}	V
Low level enable voltage	V _{EL}	0	—	0.8	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T _{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

(*) 6.3mA is a guard banded value which allows for at least 20% CTR degradation.

Initial input current threshold value is 5.0 mA or less.

**This item denotes operating ranges, not meaning of recommended operating conditions.

Absolute Maximum Ratings (no derating required)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Reverse voltage	V _R	5	V
	Diode power dissipation	P _D	100	mW
	Diode power dissipation derating (T _a ≥ 70°C)	ΔP _D /°C	-1.8	mW/°C
	Junction Temperature	T _j	125	°C
Detector	Output current	I _O	25	mA
	Output voltage	V _O	-0.5 to 7	V
	Supply voltage (1 minute maximum)	V _{CC}	7	V
	Enable input voltage (not to exceed V _{CC} by more than 500mV)	V _E	5.5	V
	Output power dissipation	P _C	40	mW
	Output Power dissipation derating (T _a ≥ 70°C)	ΔP _C / °C	-0.7	mW / °C
	Junction Temperature	T _j	125	°C
Operating temperature range		T _{opr}	-40 to 85	°C
Storage Temperature range		T _{stg}	-55 to 125	°C
Lead Solder Temperature (10 s)		T _{sol}	260	°C
Isolation voltage (R.H. ≤ 60 %, AC 60 s) (Note 10)		BVS	2500	V _{rms}
			3540	V _{dc}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(**) 1.6 mm below seating plane.

Electrical Characteristics (Ta = 0°C to 70°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
High level output current	I _{OH}	V _{CC} = 5.5 V, V _O = 5.5 V I _F = 250 μA, V _E = 2.0 V	—	1	250	μA
Low level output voltage	V _{OL}	V _{CC} = 5.5 V, I _F = 5 mA V _E = 2.0 V, I _{OL} (sinking) = 13 mA	—	0.4	0.6	V
High level supply current	I _{CCH}	V _{CC} = 5.5 V, I _F = 0 A, V _E = 0.5 V	—	7	15	mA
Low level supply current	I _{CCL}	V _{CC} = 5.5 V, I _F = 10 mA, V _E = 0.5 V	—	12	19	mA
Low level enable current	I _{EL}	V _{CC} = 5.5 V, V _E = 0.5 V	—	-1.6	-2.0	mA
High level enable current	I _{EH}	V _{CC} = 5.5 V, V _E = 2.0 V	—	-1	—	mA
High level enable voltage	V _{EH}	(Note 11)	2.0	—	—	V
Low level enable voltage	V _{EL}	—	—	—	0.8	
Input forward voltage	V _F	I _F = 10 mA, Ta = 25 °C	—	1.65	1.75	V
Input reverse breakdown voltage	BV _R	I _R = 10 μA, Ta = 25 °C	5	—	—	V
Input capacitance	C _{IN}	V _F = 0 V, f = 1 MHz	—	45	—	pF
Input diode temperature coefficient	ΔV _F /ΔT _A	I _F = 10 mA	—	-2.0	—	mV / °C
Input-output insulation leakage current	I _{I-O}	Relative humidity = 45 % Ta=25 °C, t = 5 s V _{I-O} = 3000 Vdc, (Note 10)	—	—	1	μA
Resistance (input-output)	R _{I-O}	V _{I-O} = 500 V, R.H. ≤ 60 % (Note 10)	5×10 ¹⁰	10 ¹⁴	—	Ω
Capacitance (input-output)	C _{I-O}	f = 1 MHz (Note 10)	—	0.6	—	pF

(**) All typ. values are at V_{CC} = 5 V, Ta = 25 °C.

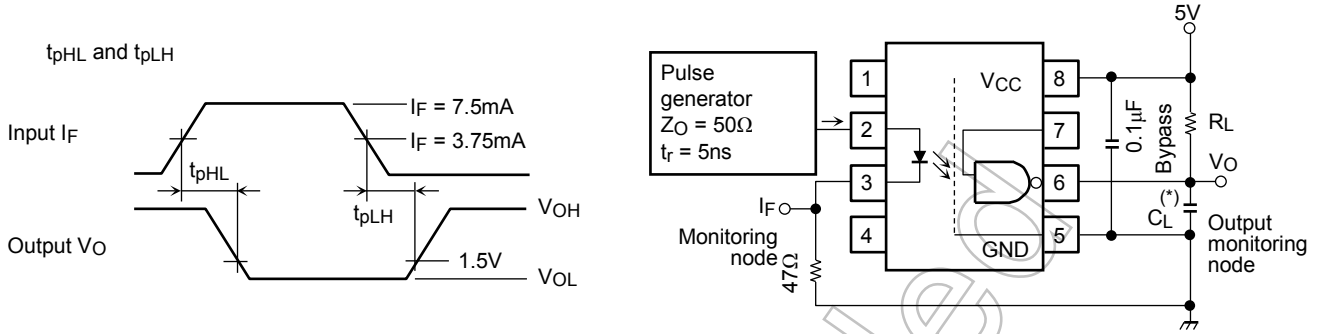
Not for New

Switching Characteristics (Ta = 25°C, Vcc = 5 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to high output level	t _{pLH}	1	R _L = 350 Ω, C _L = 15 pF I _F = 7.5 mA (Note 2), (Note 3), (Note 4)&(Note 5)	—	60	75	ns
Propagation delay time to low output level	t _{pHL}			—	60	75	ns
Output rise time (10–90%)	t _r			—	30	—	ns
Output fall time (90–10%)	t _f			—	30	—	ns
Propagation delay time of enable from V _{EH} to V _{EL}	t _{ELH}	2	R _L = 350 Ω, C _L = 15 pF I _F = 7.5 mA V _{EH} = 3.0 V V _{EL} = 0.5 V (Note 6) & (Note 7)	—	25	—	ns
Propagation delay time of enable from V _{EL} to V _{EH}	t _{EHL}			—	25	—	ns
Common mode transient immunity at high output level	CMH	3	V _{CM} = 400 V R _L = 350 Ω V _{O(min)} = 2 V I _F = 0 mA, (Note 9)	1000	10000	—	V/μs
Common mode transient immunity at low output level	CML			–1000	–10000	—	V/μs

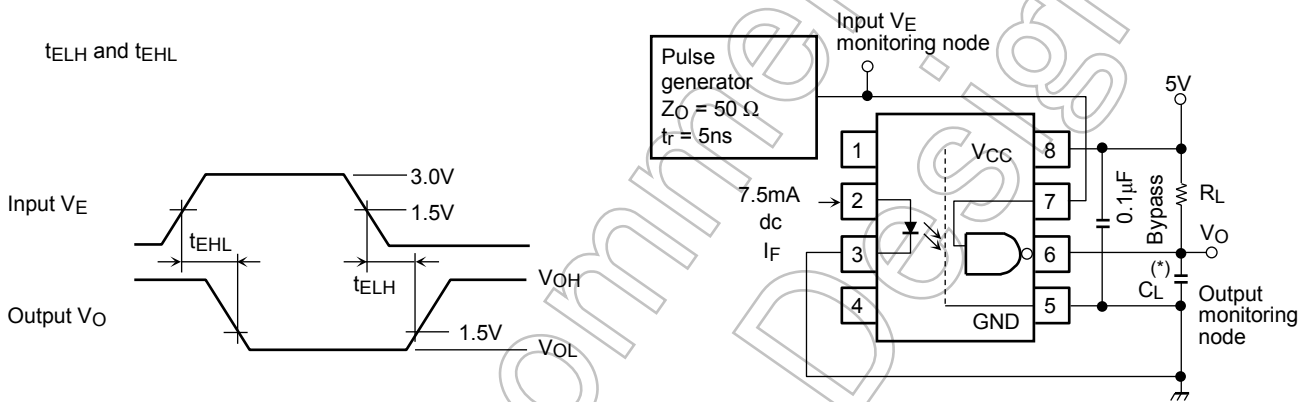
Not Recommended for New Design

Test Circuit 1.



(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

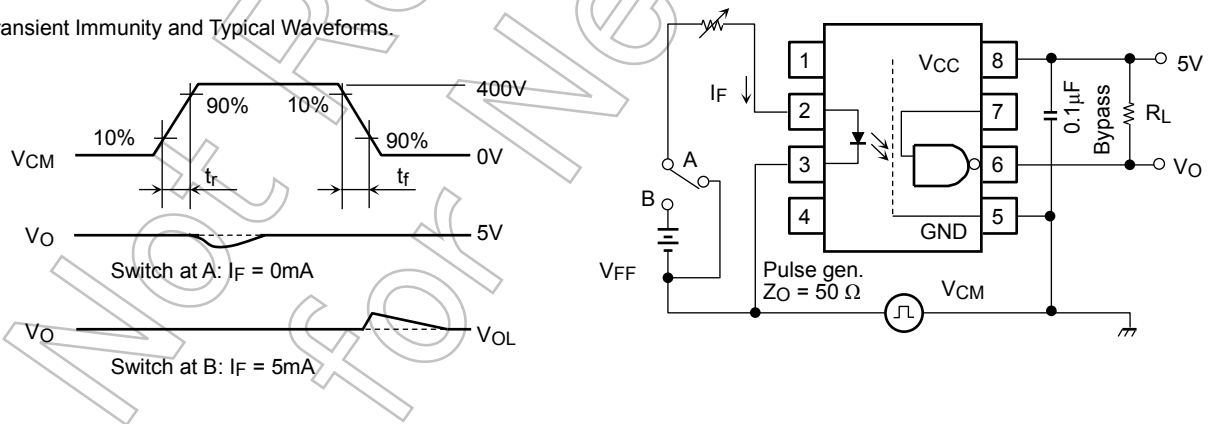
Test Circuit 2.

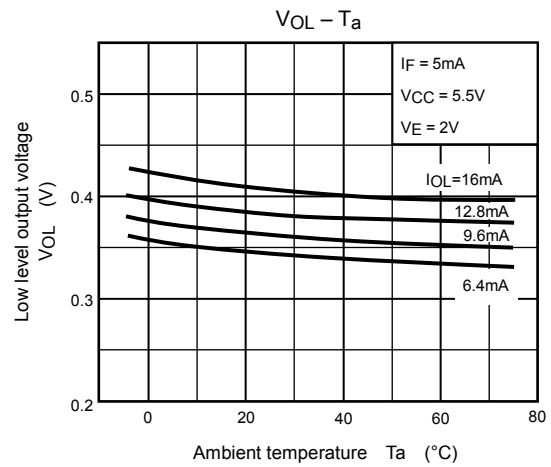
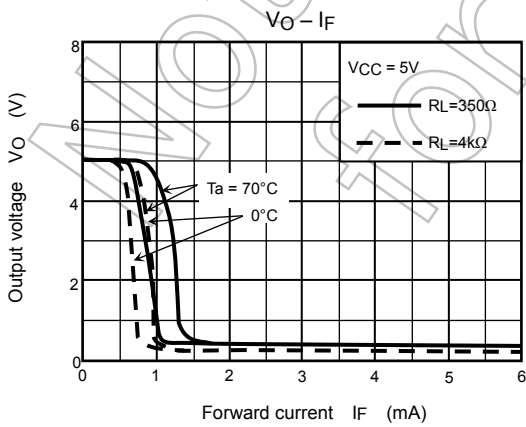
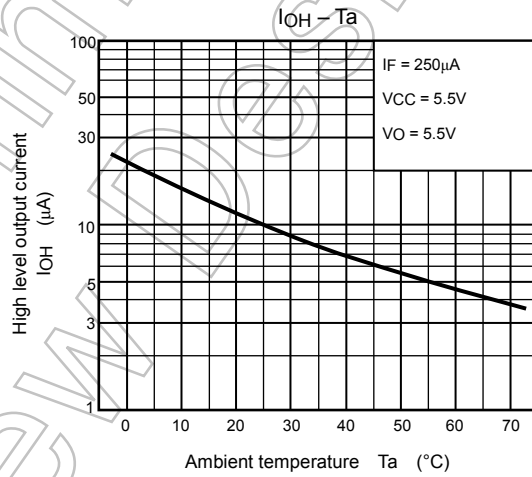
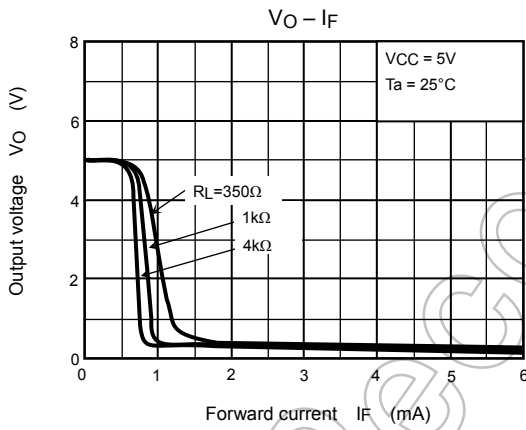
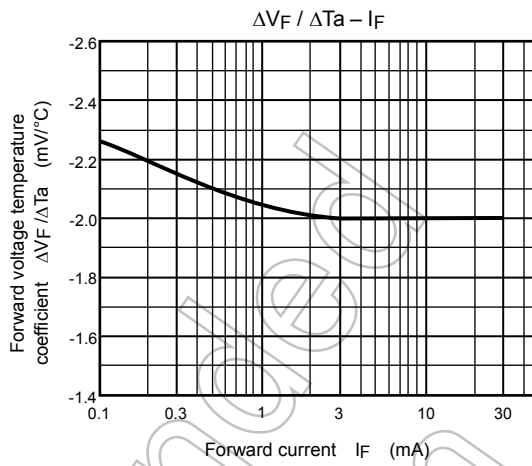
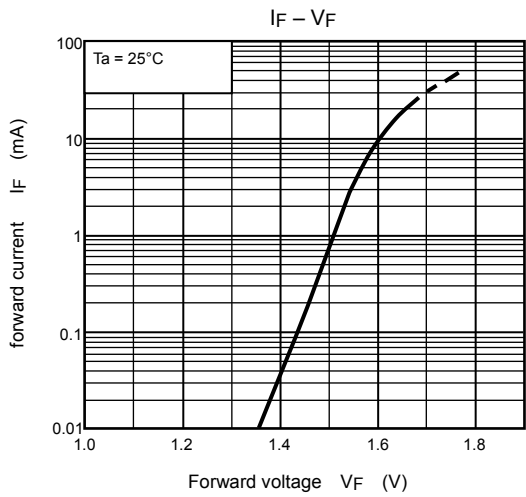


(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

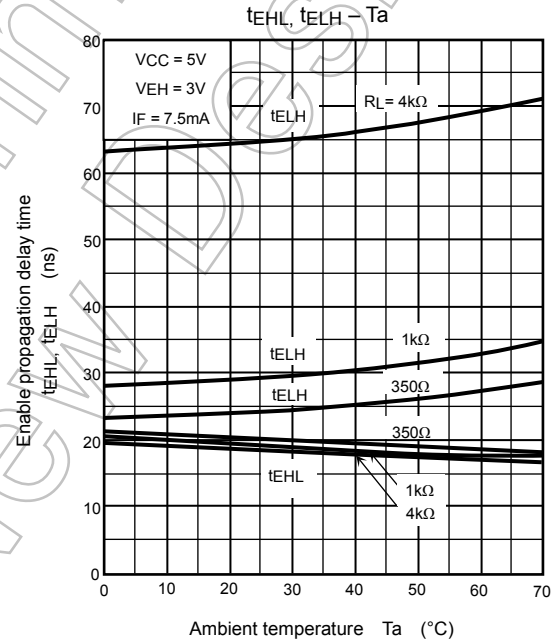
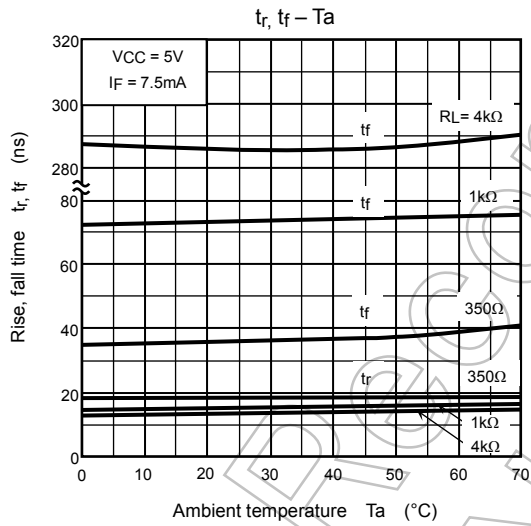
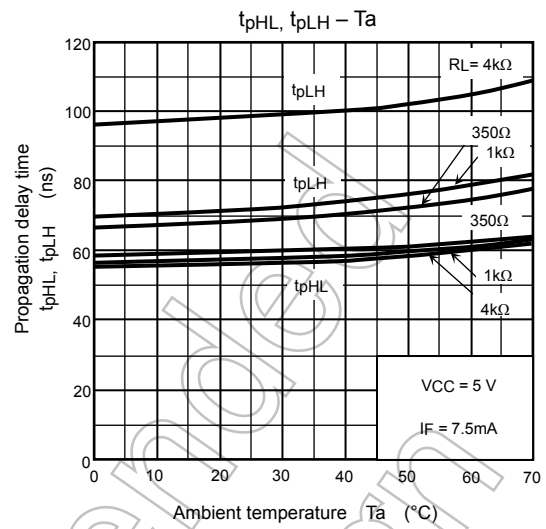
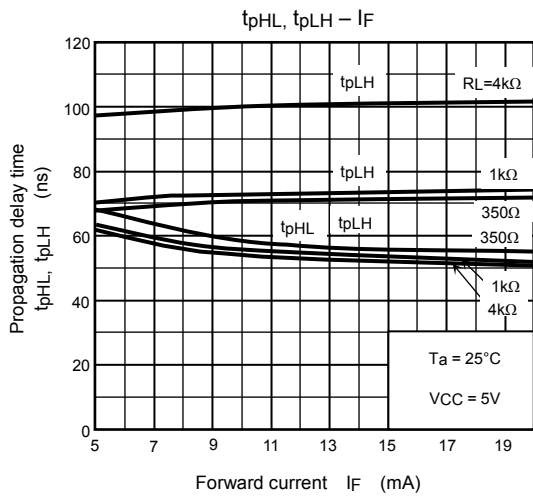
Test Circuit 3.

Transient Immunity and Typical Waveforms.





NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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Notes

1. The VCC supply voltage to each TLP2601 isolator must be bypassed by a 0.1 μF capacitor of larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins of each device.
2. t_{pHL} · Propagation delay is measured from the 3.75 mA level on the low to high transition of the input current pulse to the 1.5 V level on the high to low transition of the output voltage pulse.
3. t_{pLH} · Propagation delay is measured from the 3.75 mA level on the high to low transition of the input current pulse to the 1.5 V level on the low to high transition of the output voltage pulse.
4. t_f · Fall time is measured from the 10 % to 90 % levels of the high to low transition on the output pulse.
5. t_r · Rise time is measured from the 90 % to 10 % levels of the low to high transition on the output pulse.
6. t_{EHL} · Enable input propagation delay is measured from the 1.5 V level on the low to high transition of the input voltage pulse to the 1.5 V level on the high to low transition of the output voltage pulse.
7. t_{ELH} · Enable input propagation delay is measured from the 1.5 V level on the high to low transition of the input voltage pulse to the 1.5 V level on the low to high transition of the output voltage pulse.
8. C_{ML} · The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e. $V_{OUT} < 0.8 \text{ V}$). Measured in volts per microsecond ($\text{V} / \mu\text{s}$).
9. C_{MH} · The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e. $V_{OUT} > 2.0 \text{ V}$). Measured in volts per microsecond ($\text{V} / \mu\text{s}$).
Volts/microsecond can be translated to sinusoidal voltages:

$$\text{V} / \mu\text{s} = \frac{(dV_{CM})}{dt} \text{ Max.} = f_{CM} V_{CM} (\text{p.p.})$$

Example:
 $V_{CM} = 318 \text{ V}_{pp}$ when $f_{CM} = 1 \text{ MHz}$ using C_{ML} and $C_{MH} = 1000 \text{ V} / \mu\text{s}$ data sheet specified minimum.
10. · Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.
11. Enable input · No pull up resistor required as the device has an internal pull up resistor.

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