3.8V TO 60V INPUT AUTOMOTIVE GRADE, 3A LOW IQ SYNCHRONOUS BUCK CONVERTER

Description

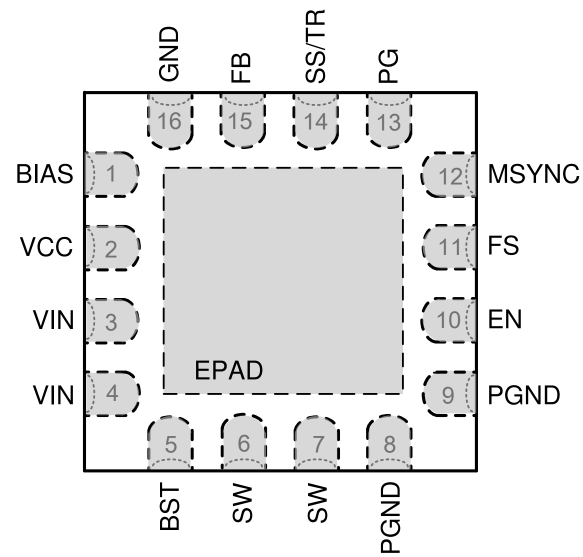
The DIODES™ AP66300Q is an adjustable switching frequency internal compensated synchronous DC-DC buck converter with a default internal frequency of 500kHz. The device fully integrates a 120mΩ high-side power MOSFET and a 55mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The device enables a continuous load current of up to 3A with efficiency as high as 95% in enhanced biased. It features current mode control operation, which enables easy loop stabilization supporting a wide range of output capacitive loads.

The AP66300Q simplifies board layout and reduces space requirements with its high level of integration and minimal need for external components, making it ideal for distributed power architectures.

The AP66300Q is available in the standard Green U-QFN4040-16/SWP (Type UXB) package.

Pin Assignments



Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C3B
- V_{IN} 3.8 to 60V
- 3A Continuous Output Current
- V_{OUT} Adjustable from 0.8V to 50V
- Enhanced Efficiency Mode with Bias
- Adjustable Switching Frequency; 500kHz Default Frequency
- Start-up with Pre-biased Output
- External Soft-Start with Tracking – Sequential, Ratiometric, or Absolute; Default Internal Soft-Start of 1.7ms
- Enable Pin with 5% tolerance
- Soft Discharge
- ±5% Power Good Detection with Internal Pull-up Resistor
- Overcurrent Protection (OCP) with Hiccup
- Thermal Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP66300Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- General-purpose point-of-load DC/DC power conversion
- Automotive infotainments
- Telecommunication systems
- Distributed power systems
- Home audio devices
- Consumer electronics
- Network systems
- FPGA, DSP, and ASIC supplies
- Green electronics

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

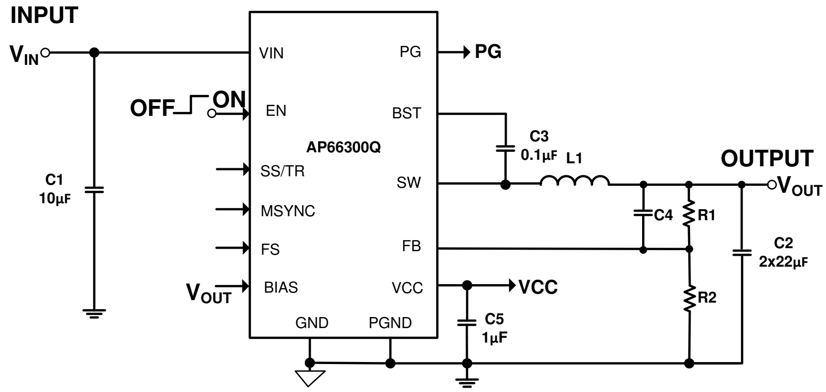


Figure 1. Typical Application Circuit

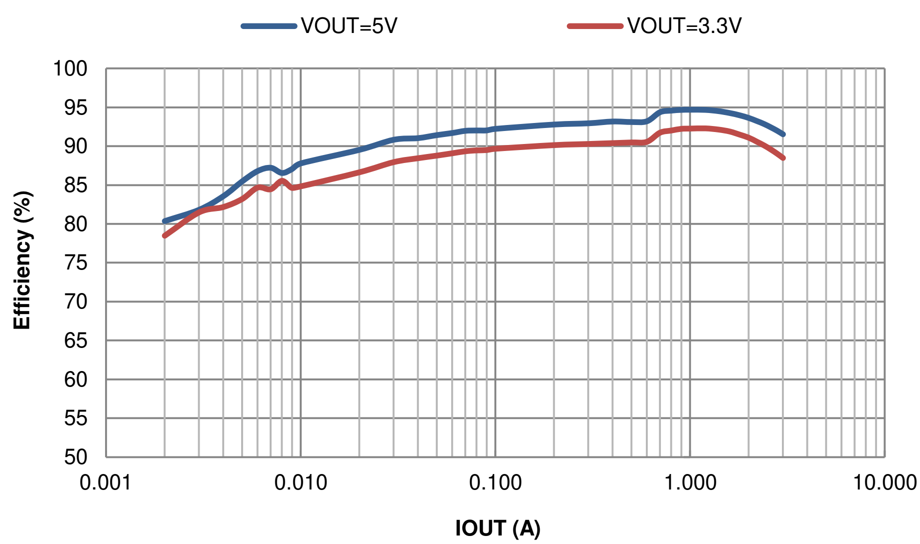


Figure 2. PFM Efficiency vs. Output Current, VIN = 12V, f_{SW} = 500kHz

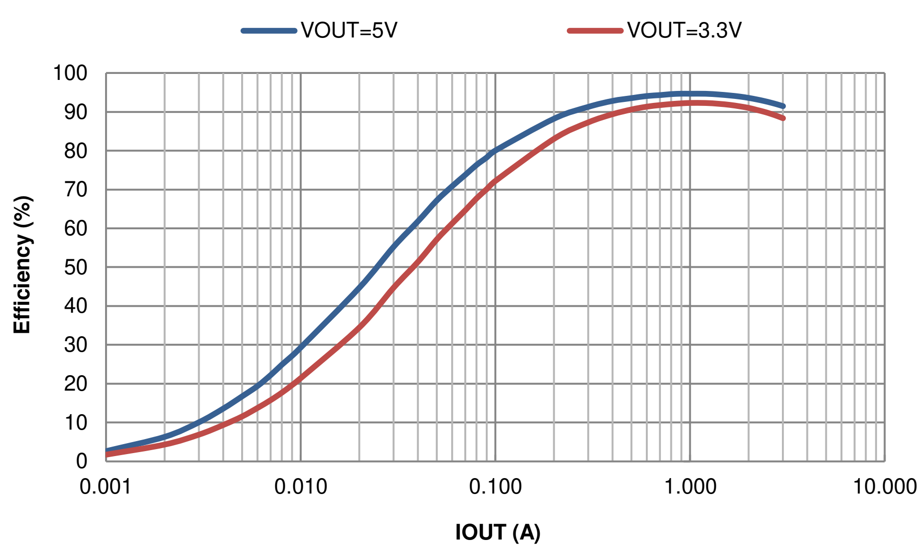


Figure 3. PWM Efficiency vs. Output Current, VIN = 12V, f_{SW} = 500kHz

Pin Descriptions

Pin Name	Pin Number	Function
BIAS	1	The internal regulator will draw current from BIAS instead of VIN when BIAS is tied to a voltage higher than 4.4V. For output voltages of 5V to 15V this pin can be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin. If no supply is available, this pin should tie to PGND.
VCC	2	Internal power supply output pin to connect an additional capacitor. Connect a 1µF (typical) capacitor as close as possible to the VCC and PGND. This pin is not active when EN is low.
VIN	3, 4	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 3.8V to 60V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
BST	5	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET with a 0.1µF or greater capacitor from SW to BST to power the high side switch.
SW	6, 7	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
PGND	8, 9	Power Ground. Connect PGND plane and EXPOSED PAD with as many via for thermal and efficiency performance.
EN	10	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect directly to VIN for automatic startup.
FS	11	This pin sets the oscillator switching frequency using a resistor, R_{FS}, from FS pin to GND. The frequency of operation can be program from 300kHz to 2.5MHz. Connect FS to VCC or HIGH for a default frequency of 500kHz.
MSYNC	12	Connect MSYNC to VCC or HIGH for forced PWM. Connect MSYNC to GND for PFM operation. Apply an external clock source for synchronization with positive edge trigger and PWM.
PG	13	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start interval. There is an internal 5MΩ pull-up resistor.
SS/TR	14	Soft-start pin for the regulator. The SS/TR pin controls the soft-start and sequence of the output. A single capacitor from SS/TR to GND determines the output ramp rate. See the “Output Tracking and Sequencing” section for more application detail about soft-start, output tracking, and sequencing. If SS is tied to VCC, then an internal soft-start of 1.7ms will be used.
FB	15	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive divider connected to it from the output voltage to this pin. The feedback regulation voltage is 0.8V. See “Setting the Output Voltage”.
GND	16	Analog ground that is used for the controller. Single point connection to the EPAD.

Functional Block Diagram

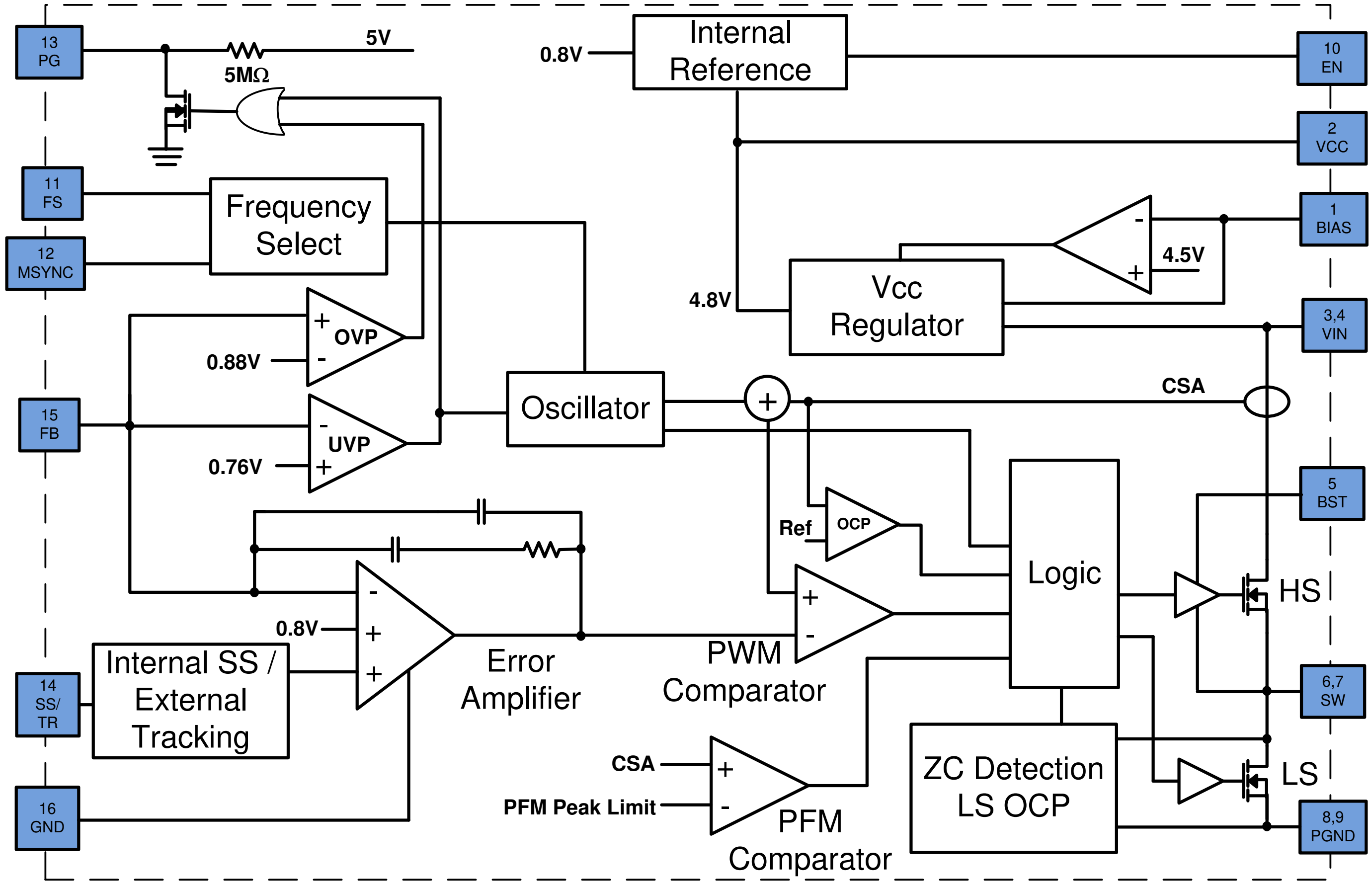


Figure 4. Functional Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +72	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3 (DC)	V
V_{SW}	Switch Node Voltage	-2.5 to V_{IN} +2 (ns)	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +72	V
V_{BST}	Bootstrap Voltage	V_{SW} -0.3 to V_{SW} +6.0	V
V_{BIAS}	Bias Voltage	-0.3 to +18	V
V_{CC}	VCC Voltage	-0.3V to +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{FS}	Frequency Adjust	-0.3V to +6.0	V
V_{PG}	Power Good Voltage	-0.3V to +6.0	V
$V_{SS/TR}$	Soft-start / Tracking	-0.3V to +6.0	V
V_{MSYNC}	Synchronization and MODE	-0.3V to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+300	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2500	V
CDM	Charged Device Model	±1500	V

Notes:
4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance

Symbol	Parameter	**JEDEC** (Note 6)	**EVM** (Note 7)	Unit
θ_{JA}	Junction to Ambient	46	30	°C/W
θ_{JC}	Junction to Case	5	5	°C/W

Note:
6. Device mounted on FR-4 substrate, 1" sq. PC board, 2oz copper, with minimum recommended pad layout.
7. Device mounted on Diodes evaluation board. See user guide for more detail.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 8)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3.8	60	V
V_{BIAS}	Supply Voltage	3.8	15	V
T_A	Operating Ambient Temperature Range	-40	+125	°C
T_J	Operating Junction Temperature Range	-40	+150	°C

Note:
8. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics

T_A = +25°C, V_{IN} = 48V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
UVLO	VCC Undervoltage Lockout Threshold	—	—	3.5	3.75	V
	Hysteresis	—	—	50	—	mV
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, VIN=60V	—	2.2	8	µA
I_Q	Supply Current (Quiescent)	V_{EN} = 2.0V, V_{FB} = 0.85V	—	43	75	µA
VCC	Internal 5V supply	V_{IN}=6V to 60V	4.4	4.8	5.3	V
I_{VCC}	VCC Output Current Limit	—	—	40	80	mA
V_{BIAS}	Rising Edge Bias Switchover Voltage	—	—	4.5	4.7	V
	Falling Edge Bias Switchover Voltage	—	4.05	4.25	—	V
$R_{DS(ON)1}$	High-Side Switch On-Resistance	—	—	120	210	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance	—	—	55	95	mΩ
$R_{DISCHARGE}$	SW Soft Discharge On-Resistance	—	—	10	—	kΩ
I_{LIMIT}	HS Peak Current Limit	VIN > 4.5V	4.3	4.8	5.3	A
		VIN < 4.5V	—	3.2	—	A
I_{PFMPK}	PFM Peak Current Limit	—	1.1	1.35	1.6	A
I_{ZC}	Zero Cross Current Threshold	—	—	0	—	A
I_{LIMIT_NEG}	LS Valley Current Limit	—	-3.3	-2.5	-1.7	A
Hiccup Time	Time delay cycle before next soft-start	—	—	8	—	T_{SS}
I_{SW_LKG}	Switch Leakage Current	V_{EN} = 0V, V_{SW} =0V, V_{IN}=60V	—	—	1	µA
F_{SW}	Oscillator Frequency	FS = VCC	440	500	560	kHz
		R_{FS} =845kΩ	240	300	360	kHz
		R_{FS} =57.6kΩ	2200	2500	2800	kHz
MSYNC	Synchronization Range	—	300	—	2500	kHz
V_{MSYNC_RISING}	MSYNC Rising Threshold	—	1.4	—	—	V
$V_{MSYNC\_FALLING}$	MSYNC Falling Threshold	—	—	—	0.8	V
MSYNC PW	MSYNC Pulse Width	—	—	250	—	ns
T_{ON}	Minimum On-Time	—	—	115	—	ns
T_{OFF}	Minimum OFF-Time	VFB=760mV	—	125	—	ns
V_{FB}	Feedback Voltage	V_{IN}=3.8V to 60V	788	800	808	mV
		SS/TR=0.1V	0.09	0.11	0.13	V
		SS/TR=0.7V	0.68	0.7	0.71	V
T_{SS}	Soft-Start Period	SS/TR=VCC	—	1.7	—	ms
I_{SS}	Soft-Start Charging Current	SS/TR=0V	0.75	1.00	1.25	µA
PG_{UV_FALL}	Undervoltage Falling Threshold	Percent of Output Regulation, Fault	87	90	93	%
PG_{UV_RISE}	Undervoltage Rising Threshold	Percent of Output Regulation, Good	92	95	99	%
PG_{OV_RISE}	Overvoltage Rising Threshold	Percent of Output Regulation, Fault	107	110	114	%
PG_{OV_FALL}	Overvoltage Falling Threshold	Percent of Output Regulation, Good	102	105	108	%
PG Pull-up	PG Pull-up resistor	—	—	5	—	MΩ
PG Low	PG Low Voltage	I_{PG}=-3mA	—	0.1	0.3	V
PG Delay	PG Rising Edge Delay	—	—	1.5	—	ms
	PG Falling Edge Delay	—	—	2	—	µs
V_{EN_TH}	EN Rising Threshold	—	1.38	1.45	1.52	V
	Hysteresis	—	—	100	—	mV
R_{EN}	EN Input Resistance	—	—	40	—	MΩ
T_{SHDN}	Thermal Shutdown (Note 9)	—	—	165	—	°C
T_{HYS}	Thermal Hysteresis (Note 9)	—	—	20	—	°C

Note: 9. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP66300Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz, BOM = Table 1, unless otherwise specified.)

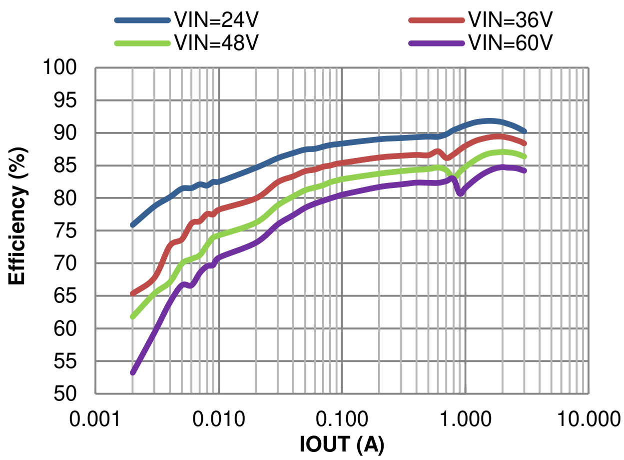


Figure 5. PFM Efficiency vs. Output Current, VOUT=5V, L=6.5µH

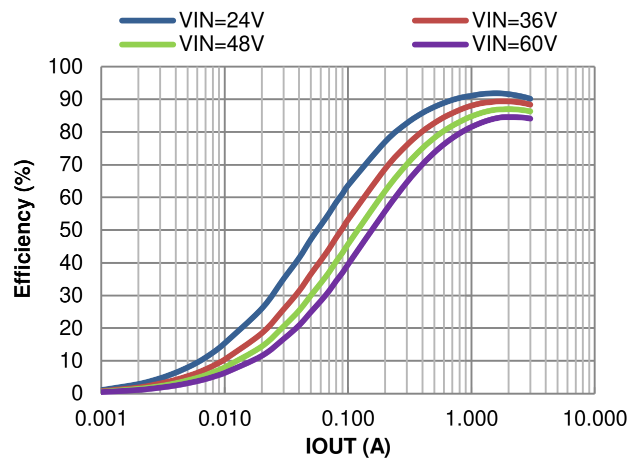


Figure 6. PWM Efficiency vs. Output Current, VOUT=5V, L=6.5µH

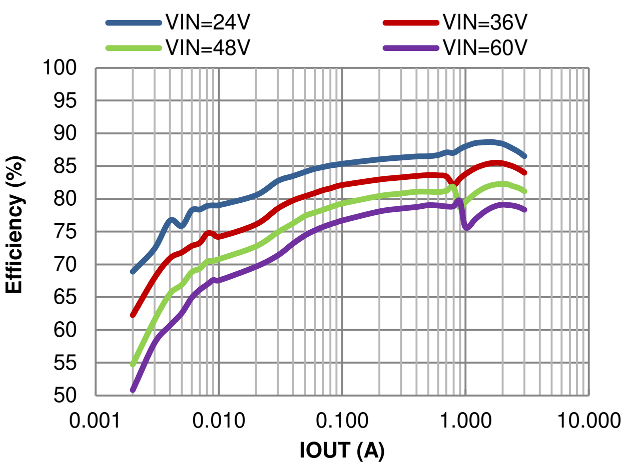


Figure 7. PFM Efficiency vs. Output Current, VOUT=3.3V, L=5.5µH

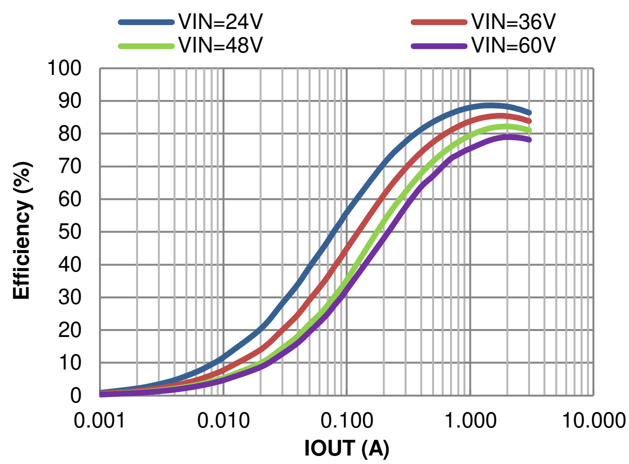


Figure 8. PWM Efficiency vs. Output Current, VOUT=3.3V, L=5.5µH

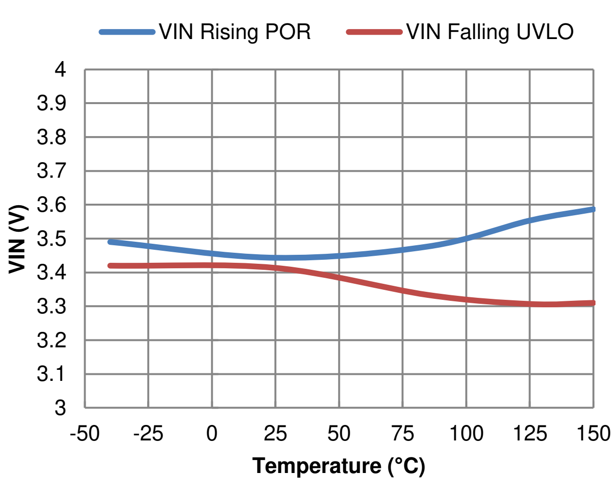


Figure 9. VIN POR and UVLO vs. Temperature

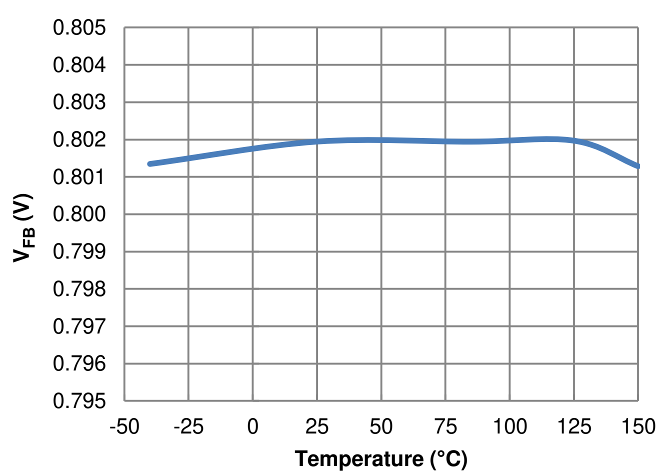


Figure 10. Feedback Voltage vs. Temperature

Typical Performance Characteristics (AP66300Q at T_A = +25°C, VIN = 12V, VOUT = 5V, f_{sw} = 500kHz, BOM = Table 1 unless otherwise specified.)

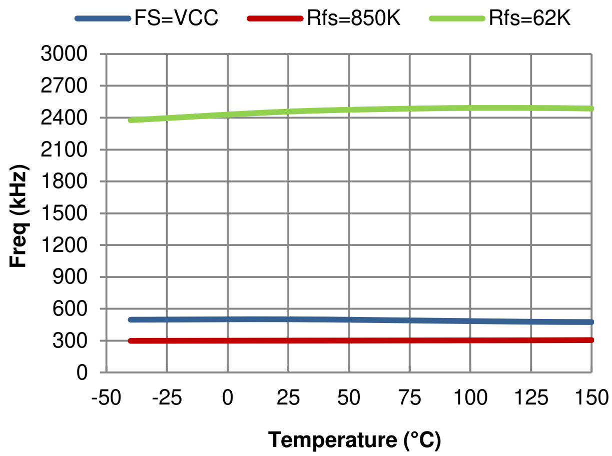


Figure 11. Frequency vs. Temperature

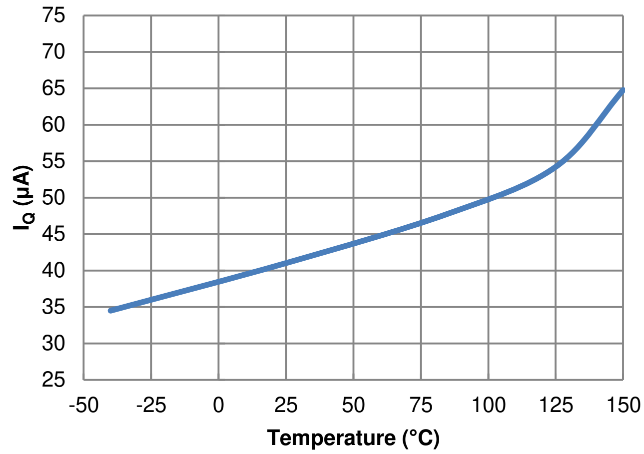


Figure 12. I_Q vs. Temperature, IOUT = 0A

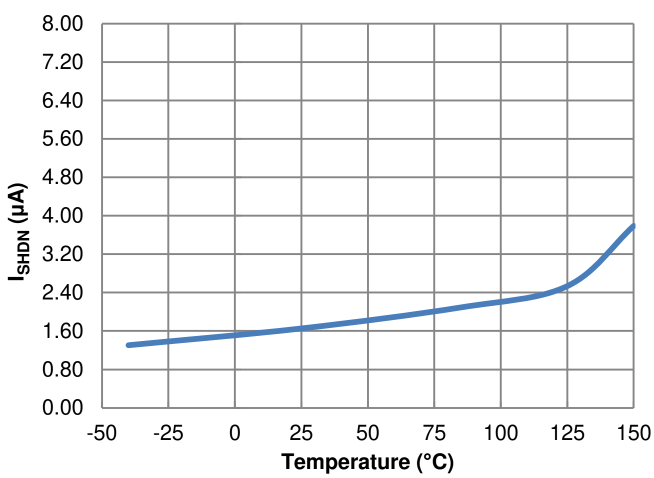


Figure 13. I_{SHDN} vs. Temperature

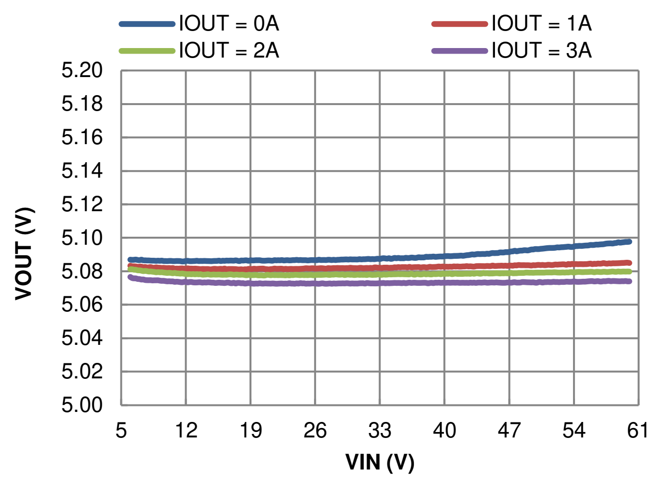


Figure 14. Line Regulation

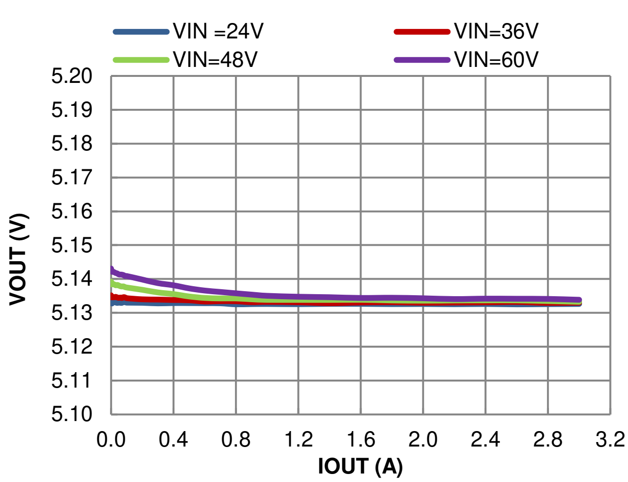


Figure 15. Load Regulation

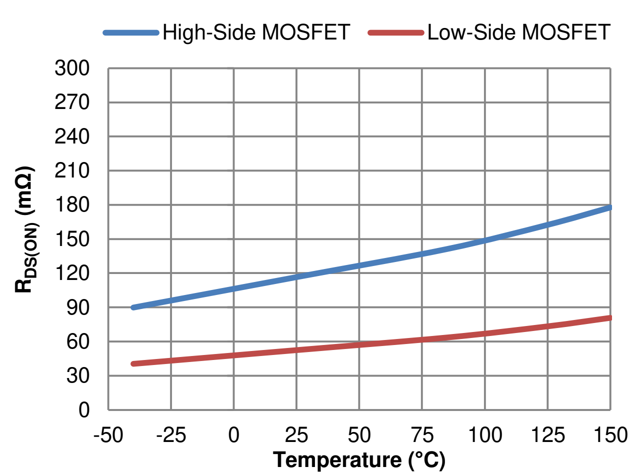


Figure 16. Power MOSFET $R_{DS(ON)}$ vs. Temperature

Typical Performance Characteristics (AP66300Q at T_A = +25°C, VIN = 12V, VOUT = 5V, f_{sw} = 500kHz, BOM = Table 1 unless otherwise specified.)

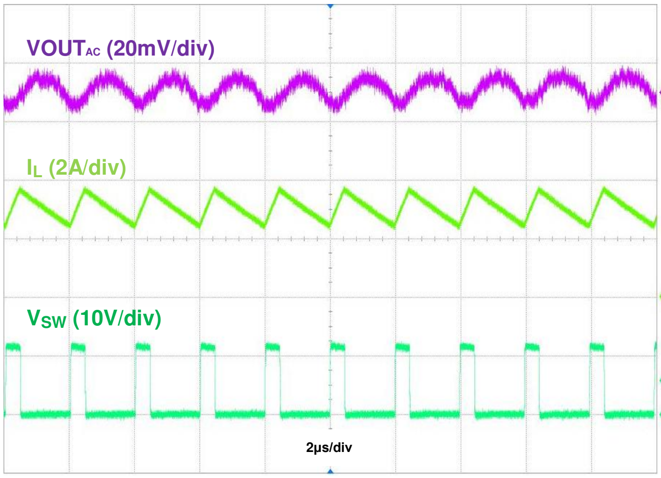


Figure 17. Output Ripple, VIN=12V, VOUT = 5V @3A, PFM

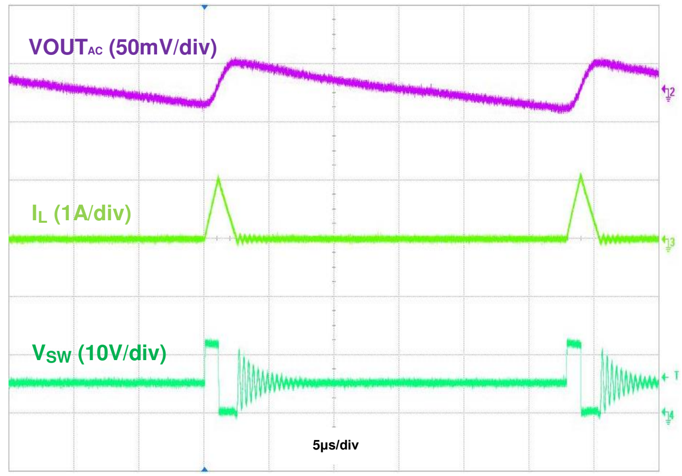


Figure 18. Output Ripple VIN = 12V, VOUT = 5V @50mA, PFM

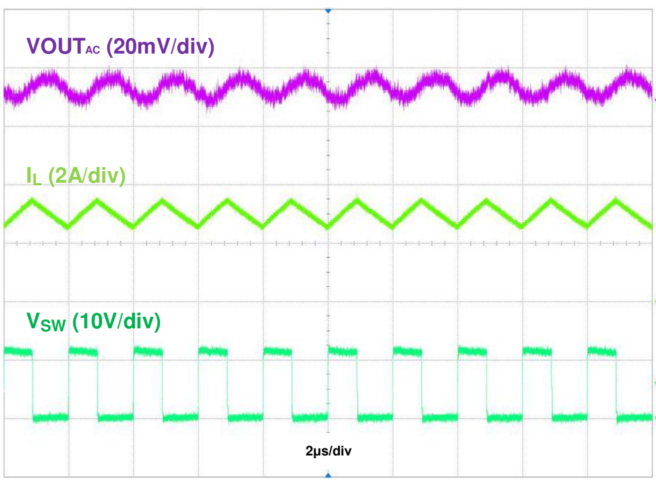


Figure 19. Output Ripple, VIN=12V, VOUT = 5V @3A, PWM

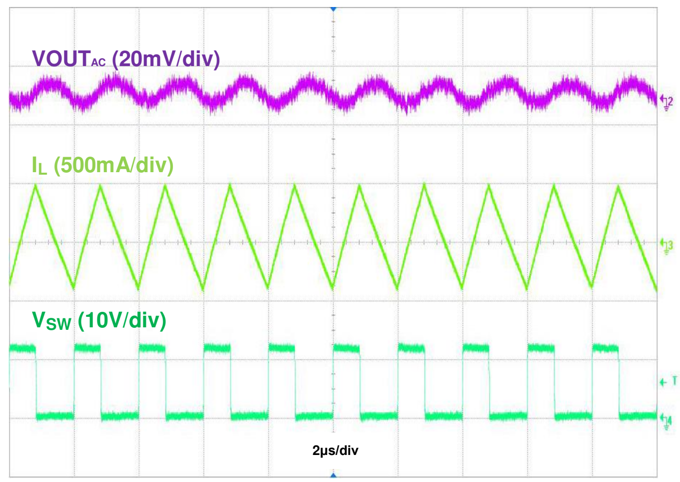


Figure 20. Output Ripple VIN = 12V, VOUT = 5V @50mA, PWM

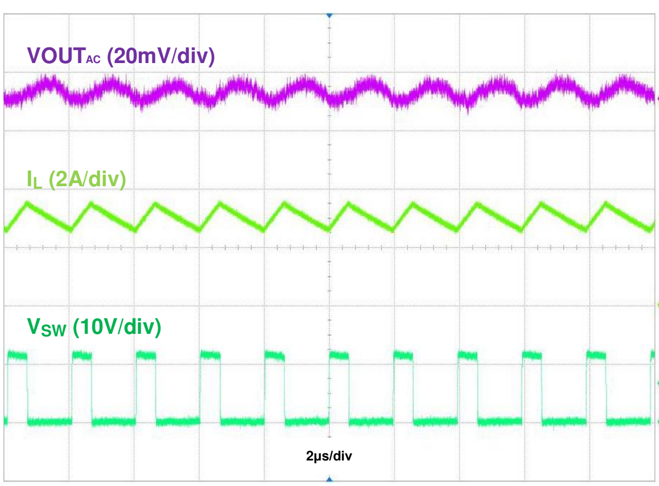


Figure 21. Output Ripple, VIN=12V, VOUT = 3.3V @3A, PFM

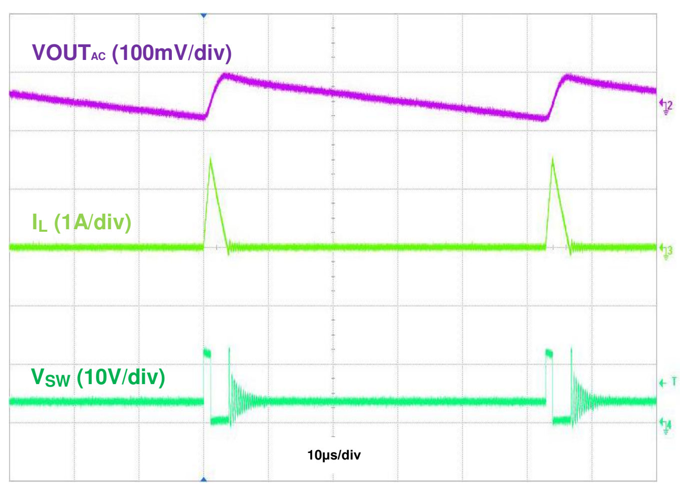


Figure 22. Output Ripple, VIN=12V, VOUT = 3.3V @50mA, PFM

Typical Performance Characteristics (AP66300Q at T_A = +25°C, VIN = 12V, VOUT = 5V, f_{sw} = 500kHz, BOM = Table 1, unless otherwise specified.)

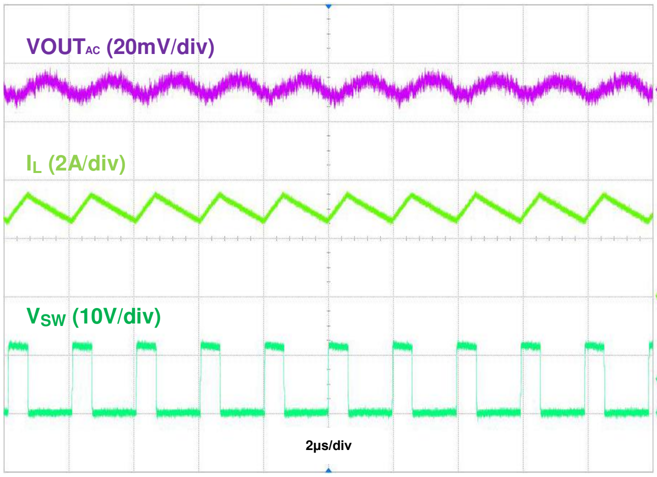


Figure 23. Output Ripple, VIN=12V, VOUT = 3.3V @3A, PFM

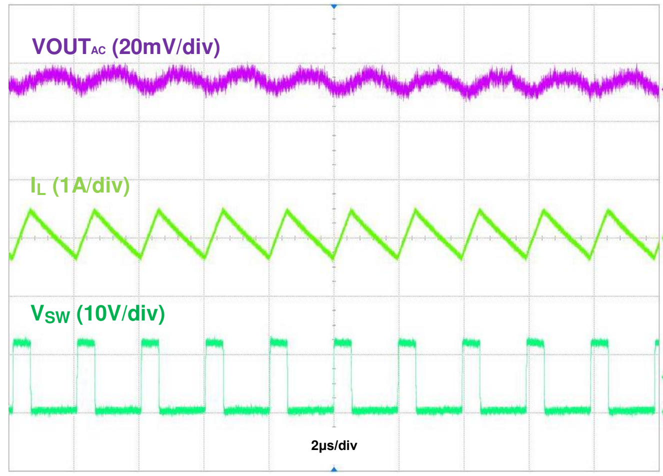


Figure 24. Output Ripple, VIN=12V, VOUT = 3.3V @50mA, PFM

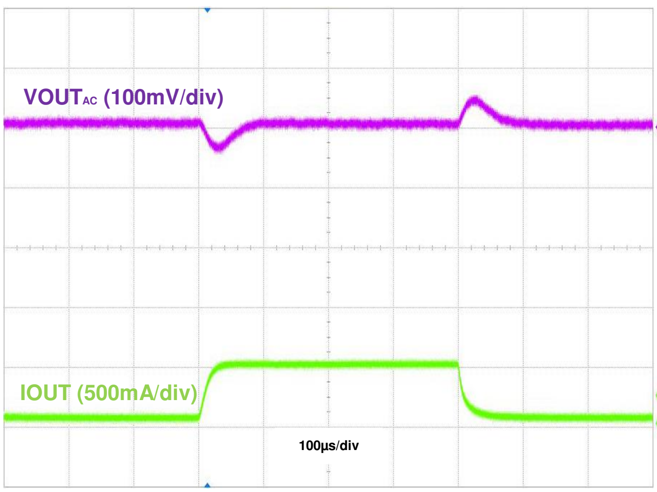


Figure 25. Load Transient, IOUT = 50mA to 500mA to 50mA, PWM

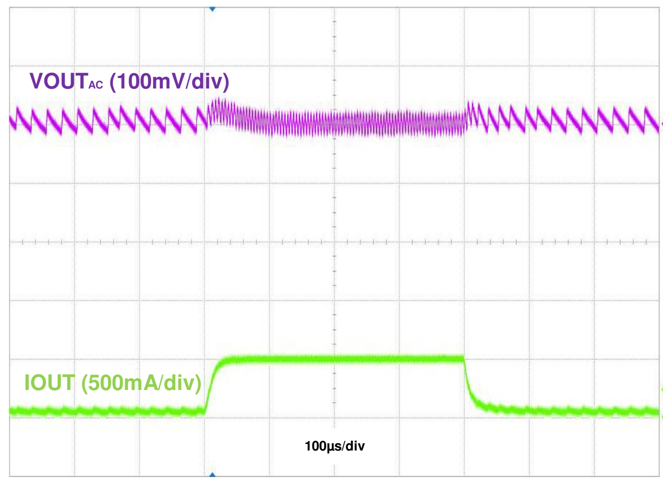


Figure 26. Load Transient, IOUT = 50mA to 500mA to 50mA, PFM

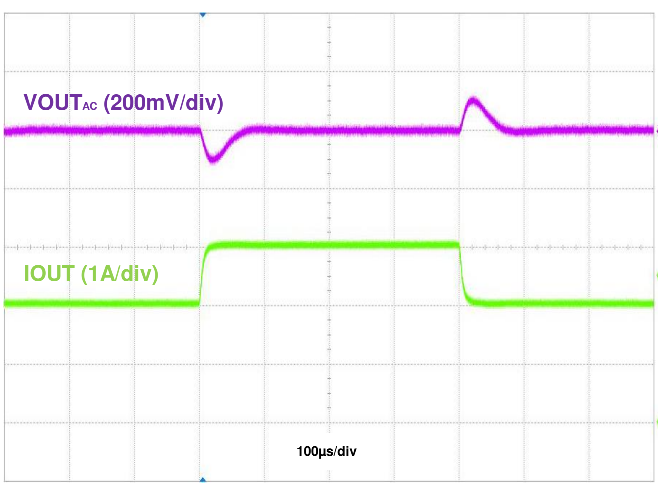


Figure 27. Load Transient, IOUT = 2A to 3A to 2A, PWM

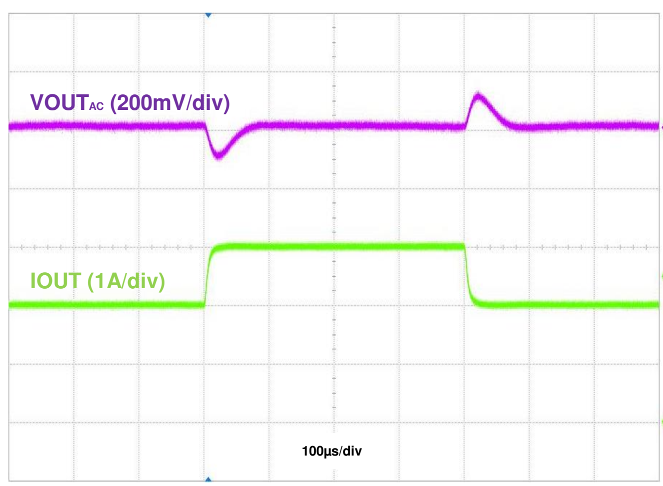


Figure 28. Load Transient, IOUT = 2A to 3A to 2A, PFM

Typical Performance Characteristics (AP66300Q at T_A = +25°C, VIN = 12V, VOUT = 5V, f_{SW} = 500kHz, BOM = Table 1, unless otherwise specified.)

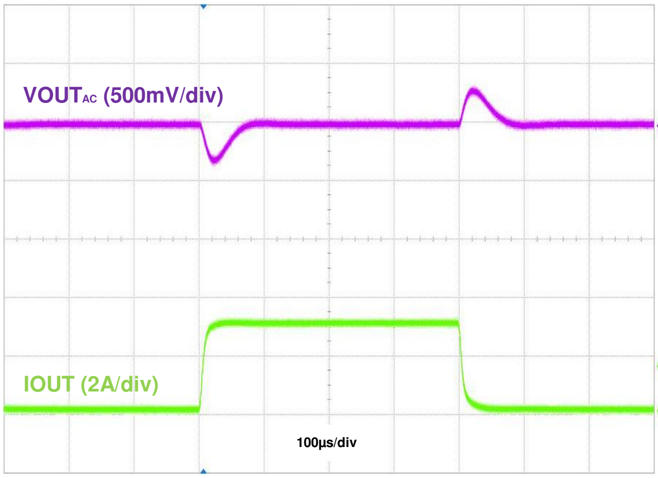


Figure 29. Load Transient, IOUT = 50mA to 3A to 50mA, PWM

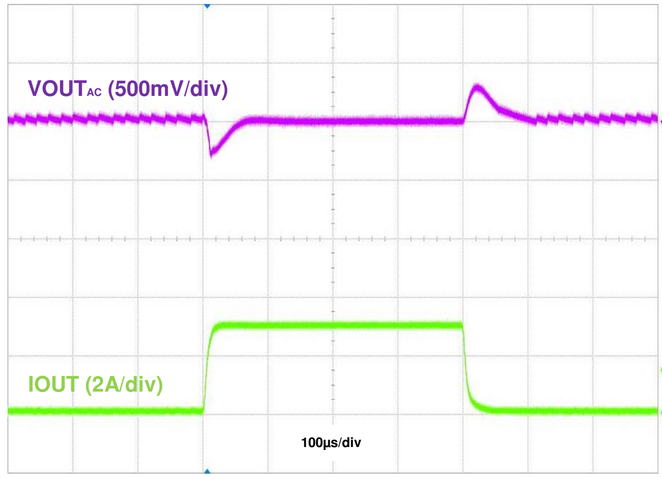


Figure 30. Load Transient, IOUT = 50mA to 3A to 50mA, PFM

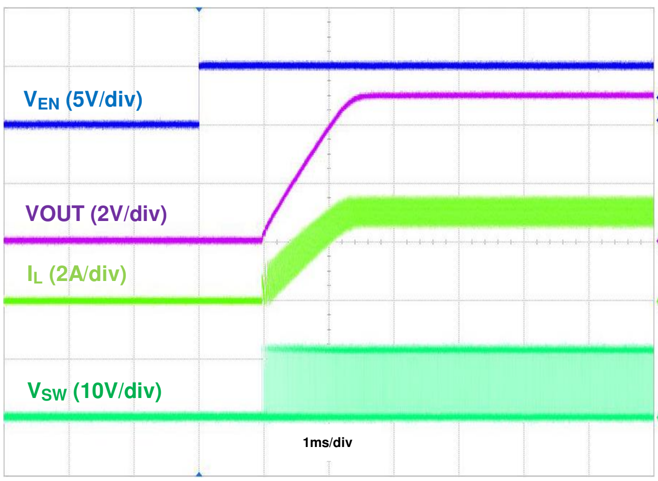


Figure 31. Startup using EN, IOUT = 3A

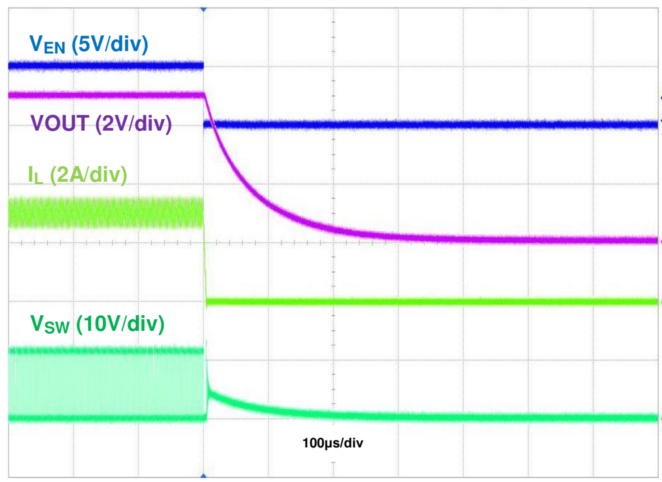


Figure 32. Shutdown using EN, IOUT = 3A

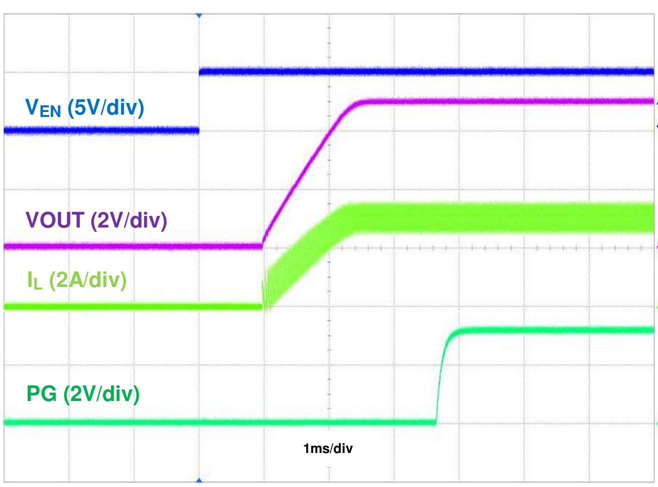


Figure 33. Startup using EN with PG, IOUT = 3A

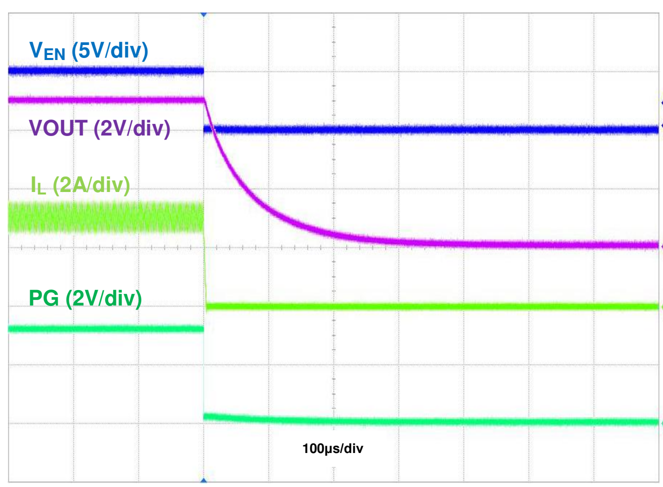


Figure 34. Shutdown using EN with PG, IOUT = 3A

Typical Performance Characteristics (AP66300Q at T_A = +25°C, VIN = 12V, VOUT = 5V, f_{sw} = 500kHz, BOM = Table 1, unless otherwise specified.)

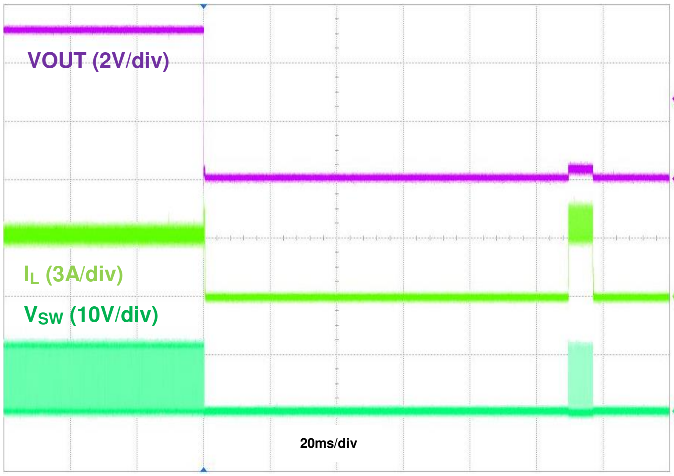


Figure 35. Output Short Protection, IOUT = 3A

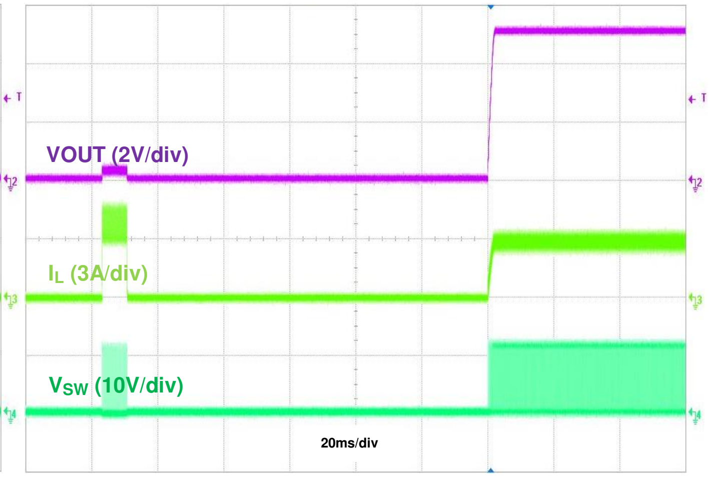


Figure 36. Output Short Recovery, IOUT = 3A

Application Information

Theory of Operation

The AP66300Q is a 3A current mode control, synchronous buck regulator with integrated power MOSFETs. Current mode control assures excellent line regulation, load regulation, and a wide loop bandwidth for fast response to load transients. Figure 1 and figure 4 depicts the typical application schematic and functional block diagram of AP66300Q. The buck controller drives the internal N-FETs. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from 3.8V to 60V. The converter output can be regulated as low as 0.8V to as high as 50V.

The feedback loop is compensated internally. See “Loop Compensation Design” for more details.

Internal VCC Regulator

An internal low dropout regulator produces the 4.8V supply from V_{IN} that powers the drivers and the internal bias circuity. The VCC can supply enough current for the AP66300Q’s circuitry and must be bypassed to PGND with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency, the internal 5V regulator can also draw current from the BIAS pin when its voltage is at 4.5V or higher. If BIAS is connected to an external supply far away, be sure to bypass with a local ceramic capacitor. If the BIAS pin voltage is below 4.25V, the internal 5V regulator will source current from V_{IN}. Application with high input voltage or high switching frequency where the internal 4.8V regulator pulls current from V_{IN} will increase the die temperature.

Enable, Soft-Start, Tracking, Sequencing, and Disable

The enable (EN) input allows the user to control turning on or off the regulator. Once the voltage on the EN pin is above its threshold, the buck controller powers up and soft-start begins.

The regulator does not allow the regulator to sink current during the soft-start period. The default time is 1.7ms if SS/TR pin is tied to VCC. The soft-start time can be extended by connecting an external capacitor between SS/TR and GND. The capacitor along with an internal I_{SS} of 1µA, sets the soft-start interval of the converter, T_{SS}, according to equation below:

C_{SS} (nF) = 1.25*T_{SS} (ms)

Ratiometric tracking is achieved in Figure 37 by using the same value for the soft-start capacitor on each power rail.

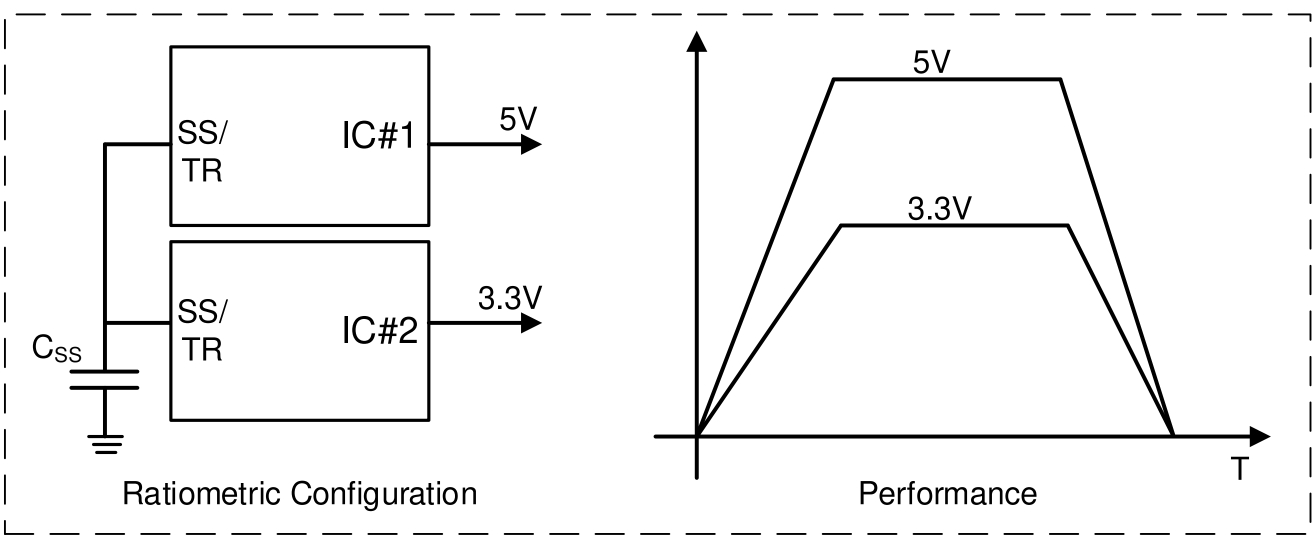


Figure 37. Ratiometic Configuration

By connecting a feedback network from the higher output voltage as shown in the Figure 38 below, coincidental track is implemented. The ratio of R3 and R4 should match with the ratio of feedback resistor divider of IC#2.

Application Information (continued)

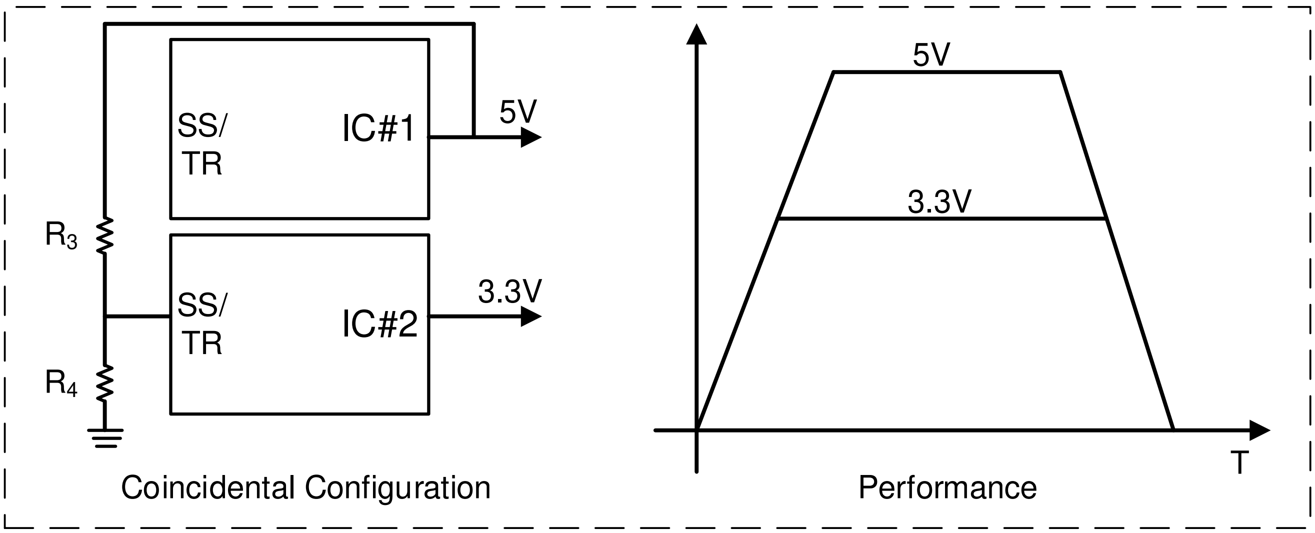


Figure 38. Coincidental Configuration

Figure 39 illustrates output sequencing.

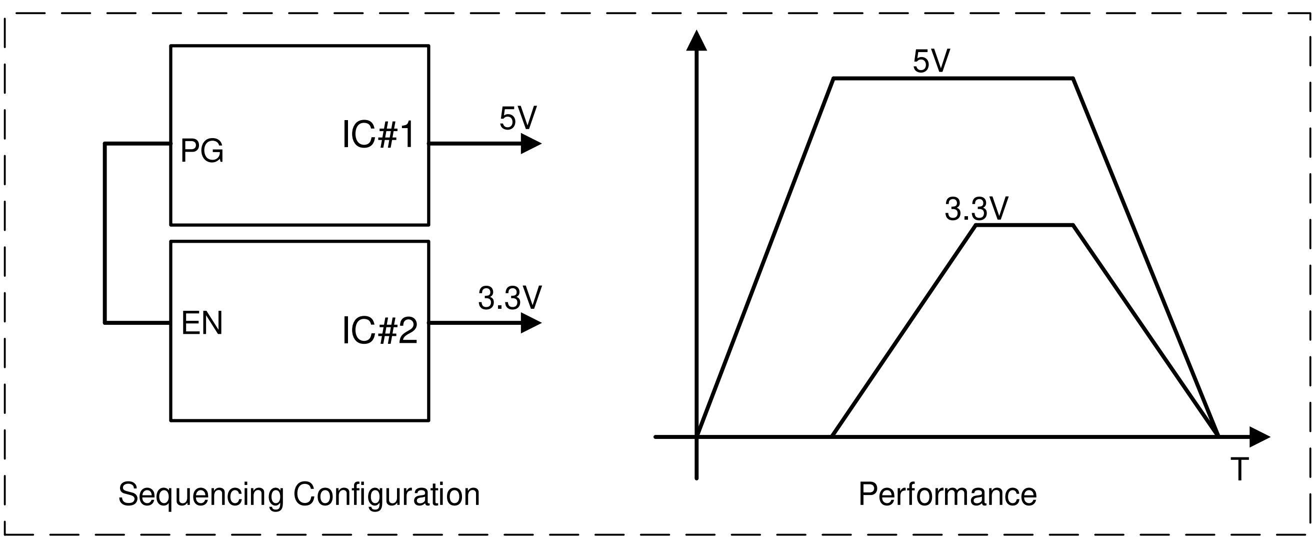


Figure 39. Sequencing Configuration

Application Information (continued)

Output Active Discharge

AP66300Q provides an internal 10kΩ resistor for output active discharge function. The internal resistor discharges the energy stored in the output capacitor to PGND whenever the regulator is disabled. When the regulator remains enabled, the internal resistor is disconnected from the output.

Current Limit Protection

In order to reduce the total power dissipation and to protect the application, AP66300Q has cycle-by-cycle current limiting implementation. The voltage drop across the internal high-side MOSFET is sense and compared with the internally set current limit threshold. This voltage drop is sensed at about 50ns after the HS turns on. When the peak inductor current exceeds the set current limit threshold, current limit protection is activated. When the current limit happens for 17 clock cycles within a 32-cycle time frame, the device enters Hiccup mode in which the controller periodically restarts the part. This protection mode greatly reduces the power dissipated on chip and reduces the thermal stress to help protect the device. AP66300Q will exit Hiccup mode when the overcurrent situation is resolved.

Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP66300Q has a UVLO comparator that monitors the VCC voltage and the internal bandgap reference. If the VCC voltage falls below 3.45V, the AP66300Q is disabled. Both HS and LS MOSFETs are off. Alternatively, the UVLO level can be adjusted adjust by using EN pin with a resistive divider connected from VIN to GND. Connect the center node of the divider to EN. Choose R3 to be approximately 500kΩ, and the R4 is calculated using the equation below with a desired V_{UVLO} threshold.

$$R_4 = \frac{R_3 \cdot 1.45}{V_{UVLO} - 1.45}$$

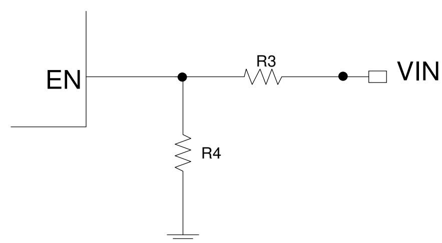


Figure 40. Setting the Input UVLO

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 165°C, the AP66300Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (145°C typical), the device initiates a normal power-up cycle with soft-start.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 4}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

Application Information (continued)

For the U-QFN4040-16/SWP (Type UXB) package, the $θ_{JA}$ is 30°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of 150°C when considering the thermal design. Figure 41 shows a typical derating curve versus ambient temperature.

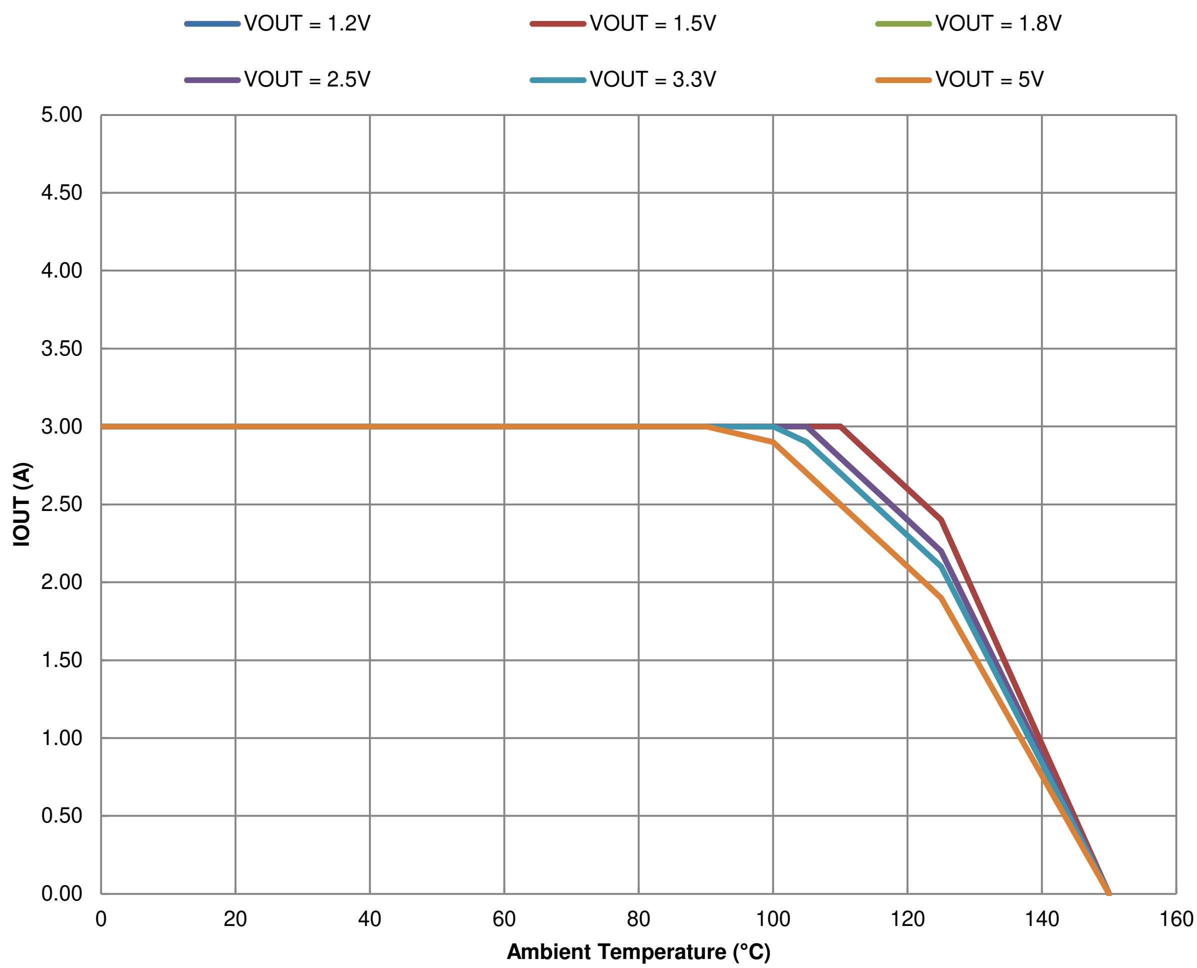


Figure 41. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

Power Good

PG is the open-drain output of a window comparator that continuously monitors the buck regulator's output voltage via the FB pin. PG is actively held low when EN is low and during the soft-start period. After the soft-start period terminates, PG becomes high impedance as long as the output voltage is within ±5% of its regulation. Any fault condition forces PG low. There is an internal 5MΩ pull-up resistor.

Application Information (continued)

Setting the Output Voltage

The output voltage can be adjusted from 0.8V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. An optional C4 of 10pF to 470pF can be used to boost the phase margin and improve stability as well as the transient performance. R2 in figure 42 can be determined by the following equation:

$$R_2 = \frac{R_1 \cdot 0.8}{Vout - 0.8}$$

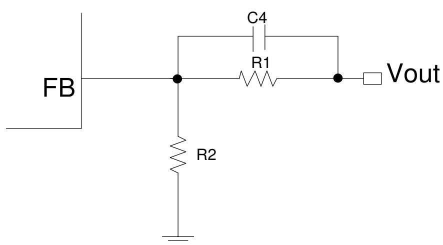


Figure 42. Feedback Divider Network

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (µH)	C2 (µF)	Fsw(kHz)
1.2	100	200	47	3.3	2x22	500
2.5	100	47.06	47	3.3	2x22	500
3.3	100	31.60	47	5.5	2x22	500
5	100	19.10	47	6.5	2x22	500
12	100	7.14	47	15	2x22	500
24	100	3.45	47	20	2x22	500

Table 1 Recommended Component Selection

Operating Frequency

The AP66300Q operates at a default switching frequency st 500kHz when FS is connected to VCC. Using a resistor from FS to GND programs the frequency from 300kHz to 2.5MHz. A minimum on-time of 115ns typical in conjunction with the input and output voltage should be considered when selecting the maximum operating frequency. Use the equation below to set the desired switching frequency:

$$R_{FS}[k\Omega] = \frac{267}{FS[MHz]} - 50$$

Alternatively, the frequency of operation can be synchronized from 300kHz to 2.5MHz with an external signal applied to the MSYNC pin.
It is recommended to use an MSYNC pulse width of at least 250ns.

CCM Control Scheme

The regulator employs a current-mode pulse-width modulation control scheme for fast transient response and pulse-by-pulse current limiting. The current loop consists of the oscillator, the PWM comparator, current sensing circuit, and a slope compensation circuit. The gain of the current sensing circuit is typically 300mV/A and the slope compensation is 500mV/T. The reference for the current loop is provided by the output of an Error Amplifier (EA), which compares the feedback signal at the FB pin to the integrated 0.8V reference. Thus, the output voltage is regulated by using the error amplifier to control the reference for the current loop. The error amplifier is an operational amplifier that converts the voltage error signal to a voltage output. The voltage loop is internally compensated with the 50pF and 320kΩ RC network that can support most applications.

PWM operation is initialized by the clock from the oscillator. The HS MOSFET is turned on at the beginning of a cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier, CSA, signal and the slope compensation, SE, reaches the control reference of the current loop, the PWM comparator sends a signal to the logic to turn off the HS MOSFET and turn on the LS MOSFET. The LS MOSFET stays on until the end of the cycle. Figure 43 shows the typical operating waveforms during Continuous Conduction Mode (CCM) operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier's output.

Application Information (continued)

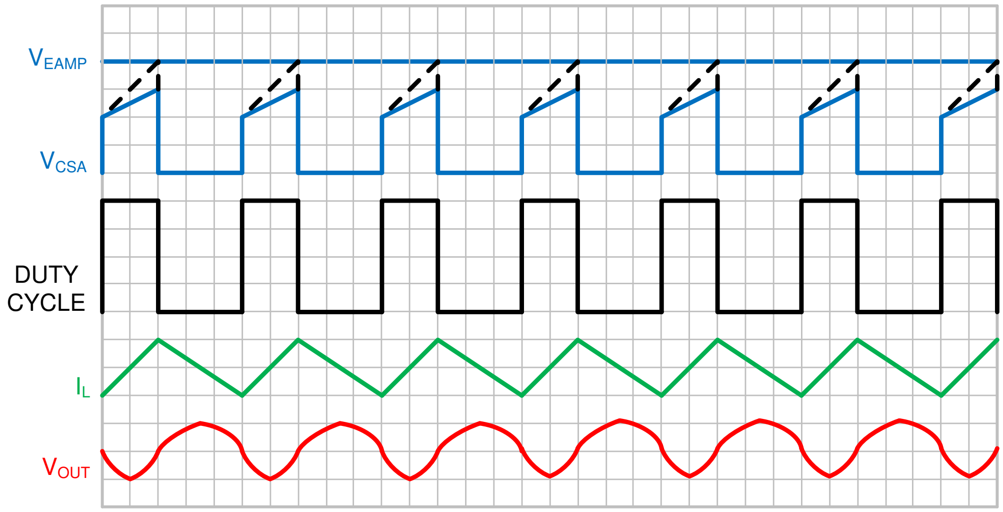


Figure 43. CCM Operation Waveforms

PFM Control Scheme

The AP66300Q enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 35 illustrates the PFM operation. A zero-cross sensing circuit shown in Figure 4 monitors the LS MOSFET current for zero crossing. When 8 consecutive cycles are detected, the regulator enters the PFM mode. The counter is reset to zero when the current in any cycle does not cross zero. Once the PFM mode is entered, the pulse modulation starts being controlled by the PFM comparator shown in Figure 44. The HS MOSFET is turned on at the clock's rising edge and turned off when its current reaches the peak PFM current limit value. Then, the inductor current is discharged to 0A, stays at zero, and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the HS MOSFET is turned on again as it repeats the previous operations. The regulator resumes normal PWM mode operation when the output voltage drops 2.5% below the nominal voltage.

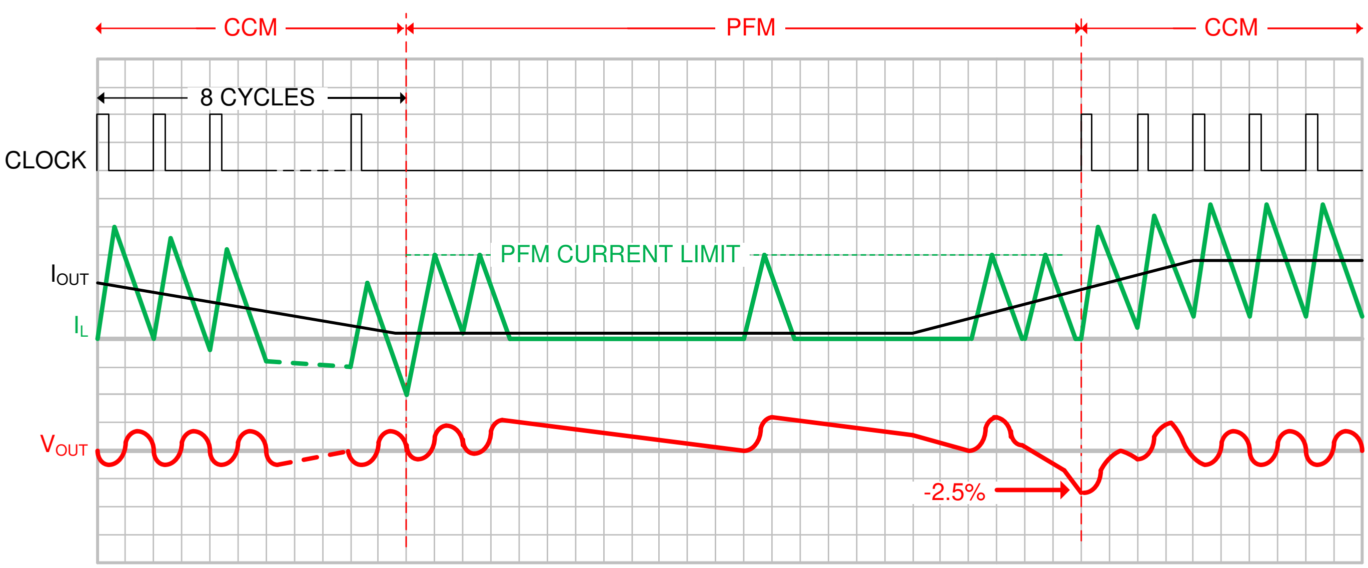


Figure 44. PFM Operation Waveforms

Application Information (continued)

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMS rating that is greater than half of the maximum load current.

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 10µF ceramic capacitor is sufficient and 0.1µF parallel capacitor is also recommended for improving the stability.

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% to 40% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence, choosing an inductor with appropriate saturation current rating is important.

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications.
For highest efficiency, the inductor's DC resistance should be as low as possible. Use a larger inductance for improved efficiency under light load conditions.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

ESR of the output capacitor dominates the output voltage ripple. The amount of ripple is approximated using the equation below:

$$\mathrm{Vout}_{\mathrm{capacitor}} = \Delta \mathrm{I}_{\mathrm{inductor}} * (\mathrm{ESR} + \frac{1}{8 \mathrm{f}_{\mathrm{SW}} C_O})$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF ceramic capacitor will be sufficient.

$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - V_{out}^2}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap

The internal driver of the HS FET is equipped with a BST undervoltage detection (UV) circuit. In the event that the voltage difference between BST and SW falls below 2V, the UV detection circuit allows the LS FET on for 400ns to recharge the bootstrap capacitor.

Self-Bias Mode

For highest possible efficiency operation, it is recommended to connect the BIAS pin directly to Vout or other external supply in the range of 4.5V to 15V. In this condition, the internal LDO will source from the BIAS voltage to minimize the power dissipation. Therefore, the overall efficiency is improved.

Application Information (continued)

Loop Compensation Design

The regulator uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a Type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 45 shows the small signal model of the synchronous buck regulator and figure 46 is the compensation network.

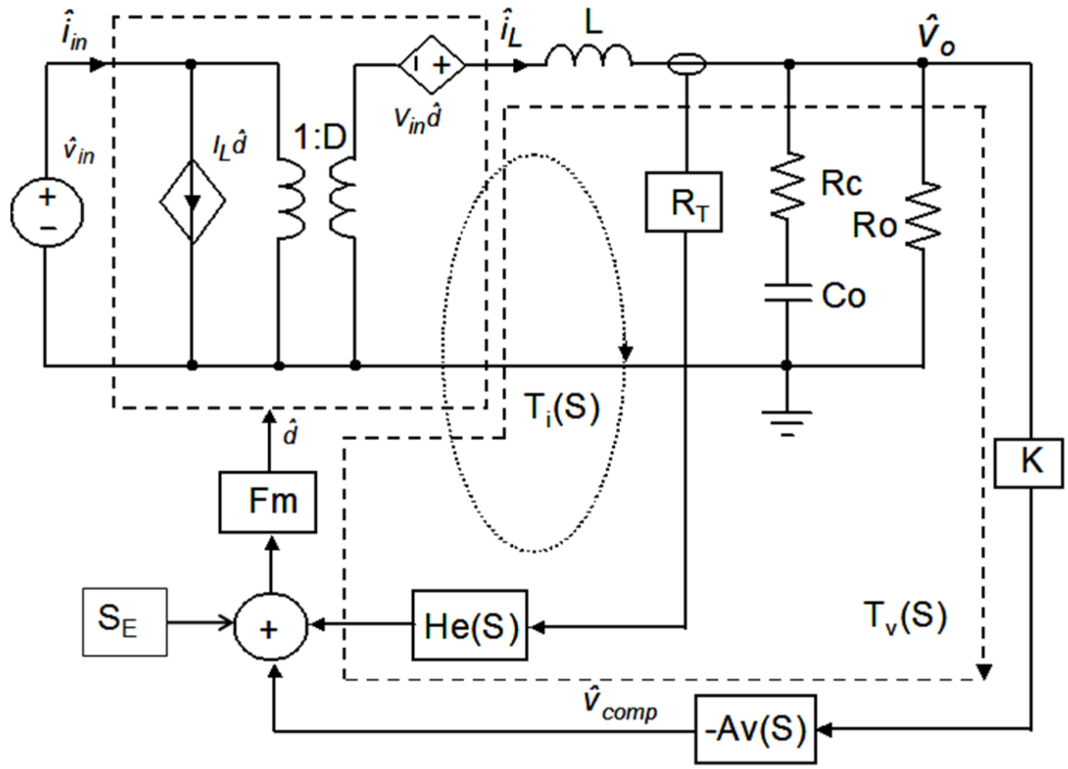


Figure 45. Linearized Small Signal Model

Figure 46 is the type 2 compensator.

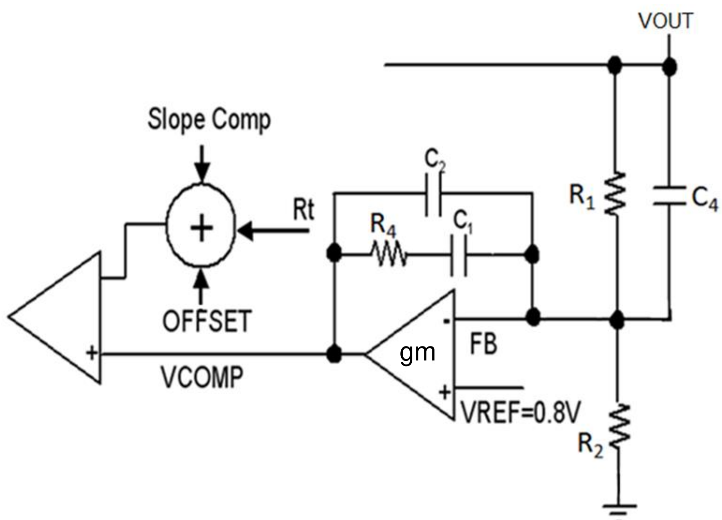


Figure 46. Type 2 Compensator

Application Information (continued)

Compensation design goals are the following:

1. Crossover frequency, f_c, of approximately 1/10th of the switching frequency.
2. Phase margin > 40°.
3. Gain margin > 10dB in magnitude.

The loop gain at the crossover frequency has a unity gain. Therefore, the value of the top feedback resistance is determined by:

$$R_1 = \frac{136k}{C_o f_C V_{OUT}}$$

Where, C_O is the total output capacitance seen by the regulator. This may include ceramic high frequency decoupling and bulk output capacitors. Ceramic will have a derating factor by approximately 40% depending on dielectric, voltage stress, and thermal.

An additional zero contribution due to R_1 and C_4 can boost the phase margin. Put the compensator zero between $1/2f_C$ to f_C frequency.

$$C_4 = \frac{1}{2\pi f c R_1}$$

Layout

PCB Layout

1. The AP66300Q is a high switching frequency converter. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The AP66300Q works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 47 for more details.

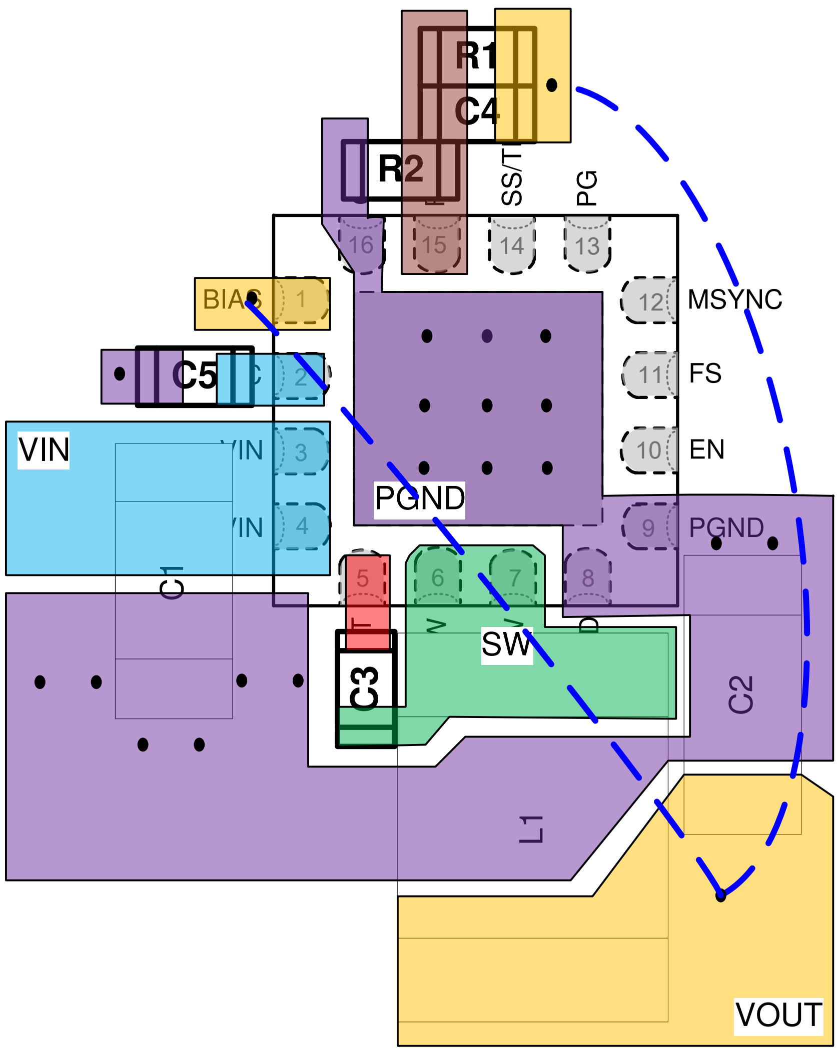


Figure 47. PC Board Layout

Ordering Information (Note 10)

AP66300xx - 13

Package	Packing
xx : xxx	13 : Tape & Reel

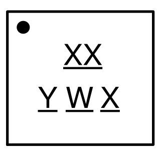
Part Number	Package Code	Package	Identification Code	Tape and Reel	
				Quantity	Part Number Suffix
AP66300QFVBW-13	FVBW	U-QFN4040-16/SWP (Type UXB)	F3Q	3000	-13

Note: 10. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-QFN4040-16/SWP (Type UXB)

(Top View)



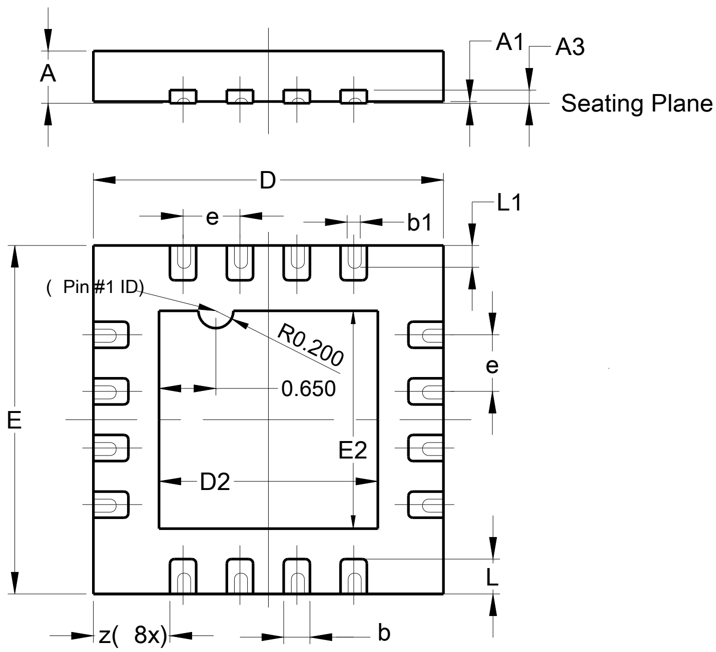
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP66300QFVBW-13	U-QFN4040-16/SWP (Type UXB)	F3Q

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-16/SWP (Type UXB)

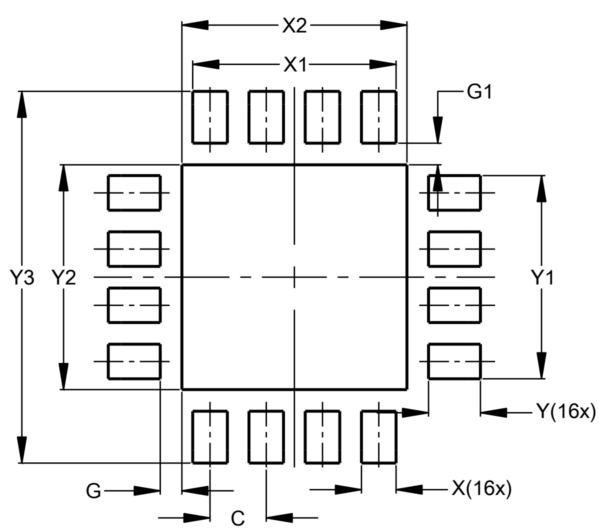


U-QFN4040-16/SWP (Type UXB)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	--	--	0.15
b	0.25	0.35	0.30
b1	--	--	0.15
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	--	--	0.65
L	0.35	0.45	0.40
L1	--	--	0.25
z	0.850	0.900	0.875
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-16/SWP (Type UXB)



Dimensions	Value (in mm)
C	0.650
G	0.250
G1	0.250
X	0.400
X1	2.350
X2	2.600
Y	0.600
Y1	2.350
Y2	2.600
Y3	4.300

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 34.54 grams (Approximate)

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