60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
60V	25mΩ @ V_{GS} = 10V	6.5A
	34mΩ @ V_{GS} = 4.5V	5.2A

Features and Benefits

- 0.6mm Profile—Ideal for Low Profile Applications
- Low On-Resistance
- PCB Footprint of 2.56mm^2
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

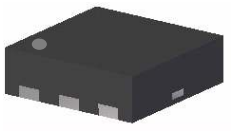
This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Power Management Functions
- Load Switch

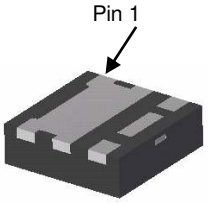
Mechanical Data

- Case: U-DFN1616-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Lead Free Plating (NiPdAu Finish over Copper Leadframe). Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.003 grams (Approximate)

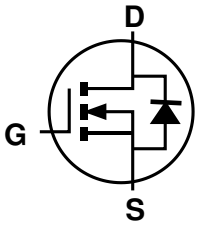
U-DFN1616-6 (Type K)



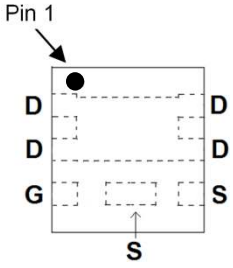
Top View



Bottom View



Device Symbol



Top View
Pin-Out

Ordering Information (Note 4)

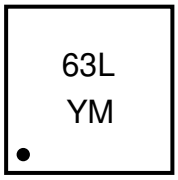
Part Number	Case	Packaging
DMT6030LFCL-7	U-DFN1616-6 (Type K)	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

Site 1:

U-DFN1616-6 (Type K)



63L = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: H = 2020)
M = Month (ex: 9 = September)

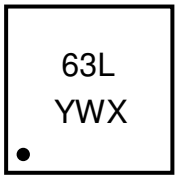
Date Code Key

Year	2017	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	E	…	H	I	J	K	L	M	N	O	P	R

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Site 2:

U-DFN1616-6 (Type K)



63L = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 0 = 2020)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2017	…	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	7	…	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	6.5 5.2	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	30	A
Maximum Body Diode Continuous Current (Note 6)			I_S	1.7	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	30	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.78	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	160	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.58	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	79	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	16.7	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 48V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	19	25	mΩ	V_{GS} = 10V, I_D = 6.5A
		—	25	34		V_{GS} = 4.5V, I_D = 4A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	639	—	pF	V_{DS} = 30V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	166	—		
Reverse Transfer Capacitance	C_{rss}	—	13.1	—		
Gate Resistance	R_g	—	1.4	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 10V)	Q_g	—	9.1	—	nC	V_{DS} = 30V, I_D = 10A
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	4.5	—		
Gate-Source Charge	Q_{gs}	—	1.2	—		
Gate-Drain Charge	Q_{gd}	—	2.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	2.6	—	ns	V_{GS} = 10V, V_{DD} = 30V, R_g = 6Ω, I_D = 10A
Turn-On Rise Time	t_R	—	2.2	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	10.7	—		
Turn-Off Fall Time	t_F	—	3.4	—		
Body Diode Reverse Recovery Time	t_{RR}	—	26.5	—	ns	I_F = 10A, dI/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	12.3	—	nC	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

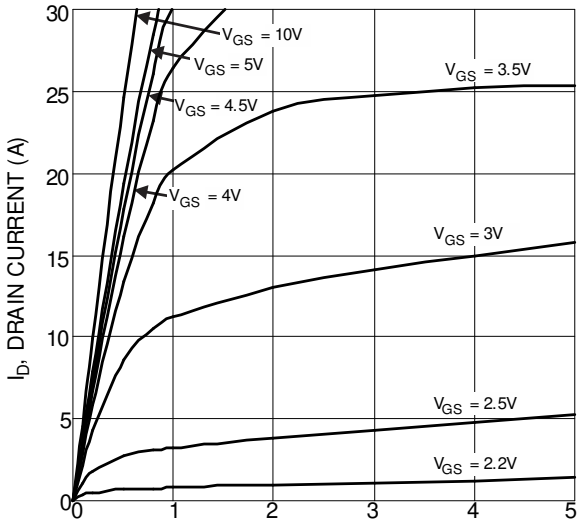


Figure 1 Typical Output Characteristic

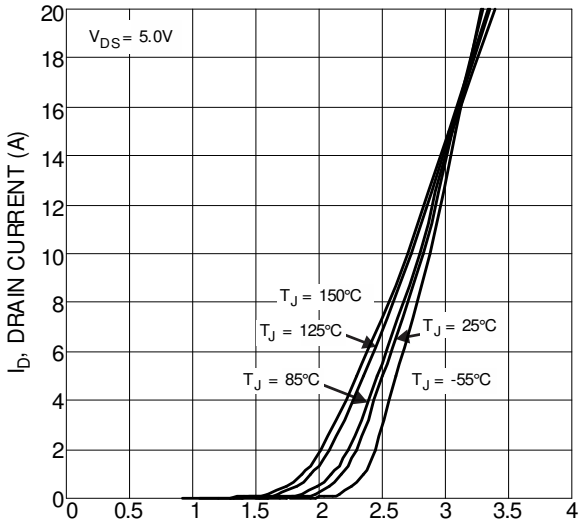


Figure 2 Typical Transfer Characteristics

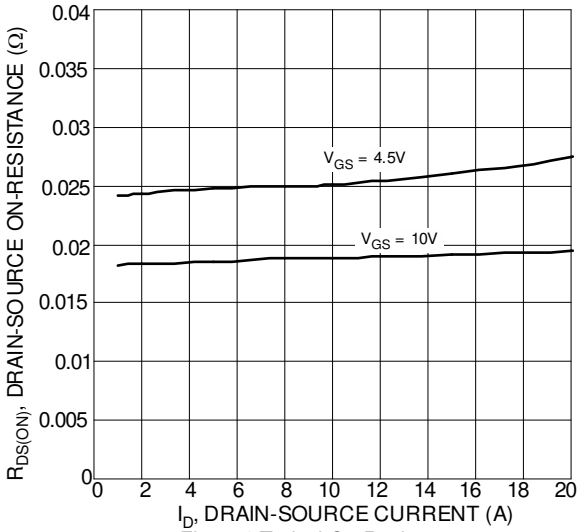


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

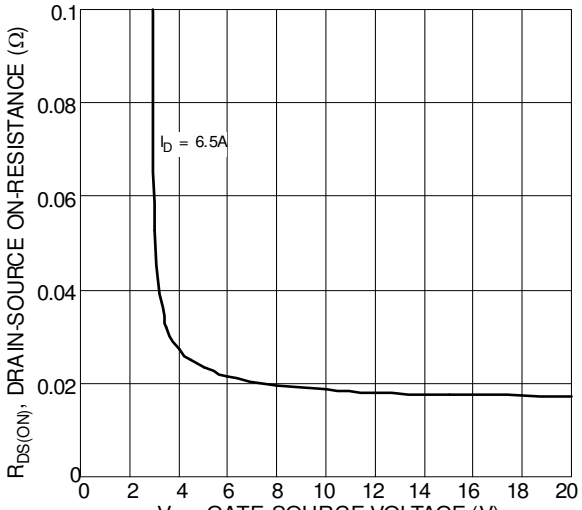


Figure 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

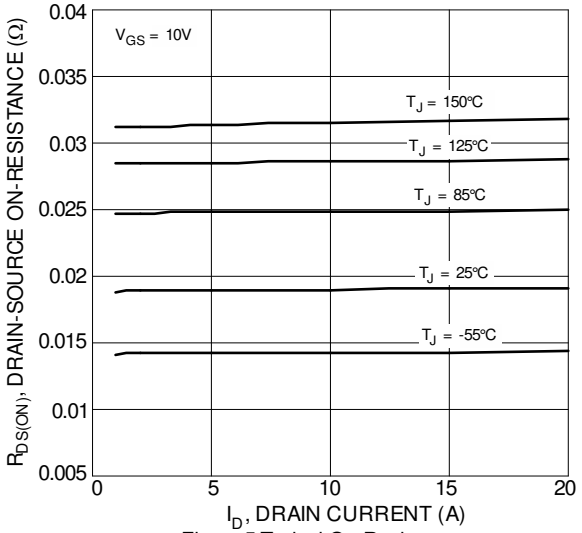


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

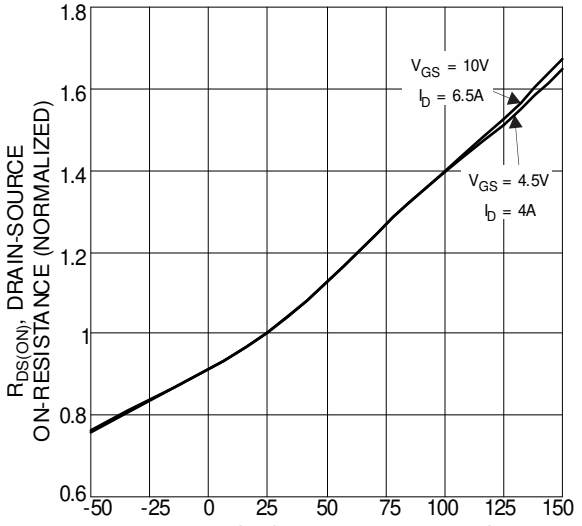


Figure 6 On-Resistance Variation with Temperature

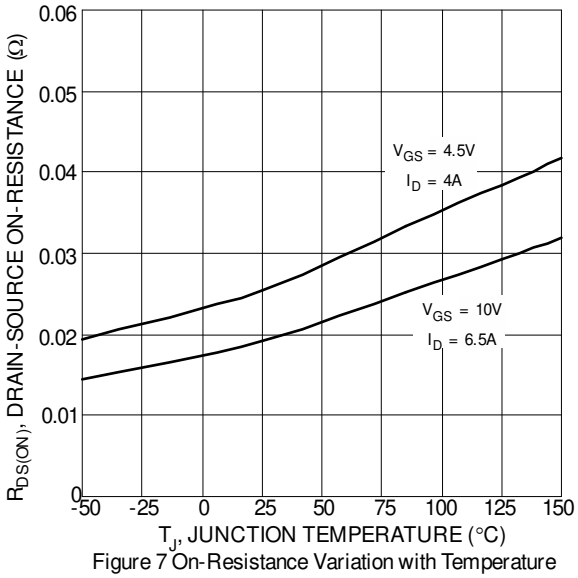


Figure 7 On-Resistance Variation with Temperature

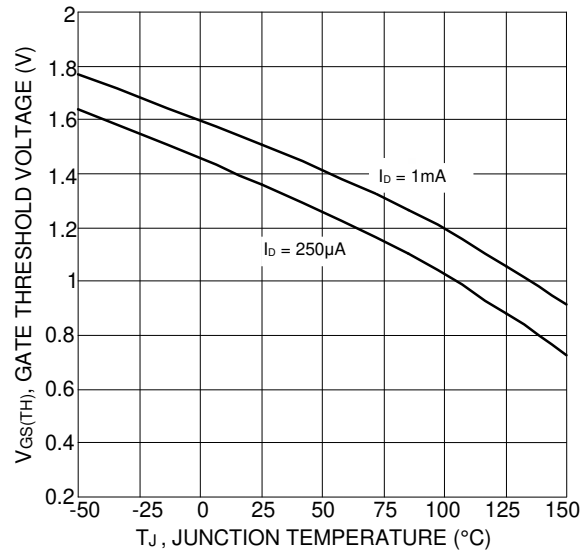


Figure 8 Gate Threshold Variation vs. Junction Temperature

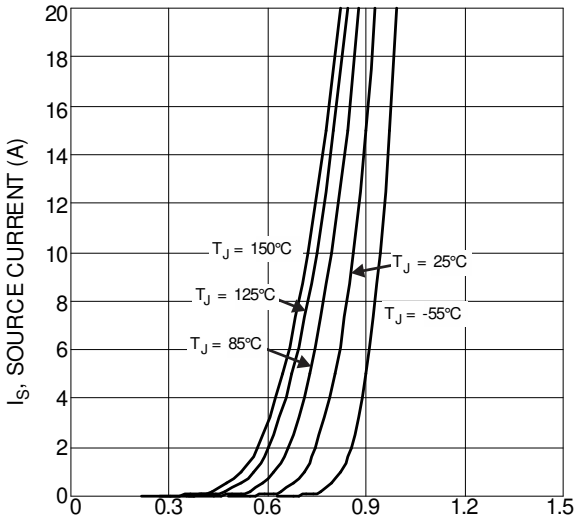


Figure 9 Diode Forward Voltage vs. Current

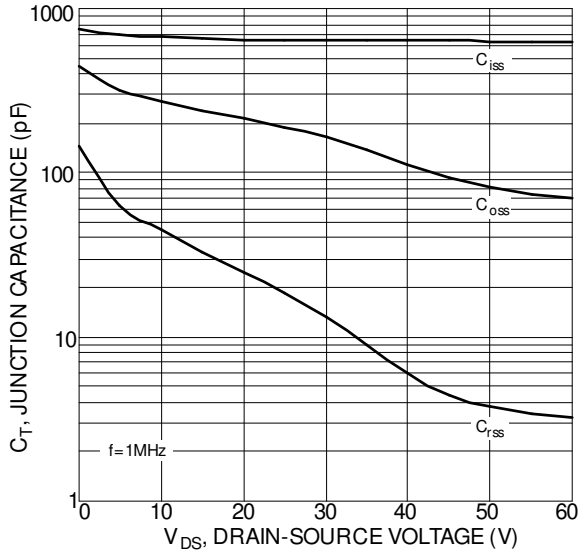


Figure 10 Typical Junction Capacitance

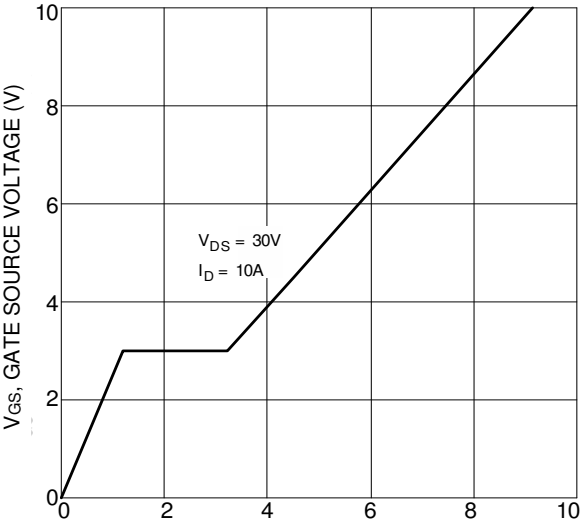


Figure 11 Gate Charge

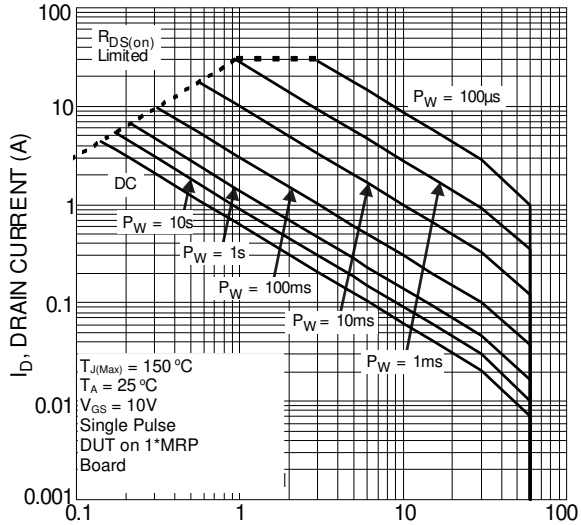


Figure 12 SOA, Safe Operation Area

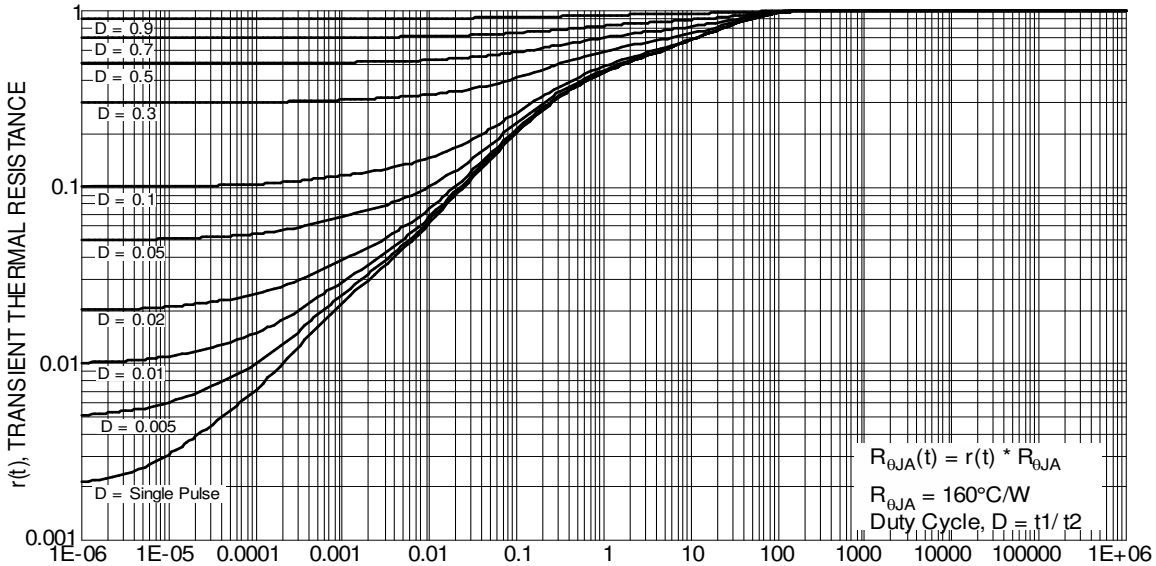
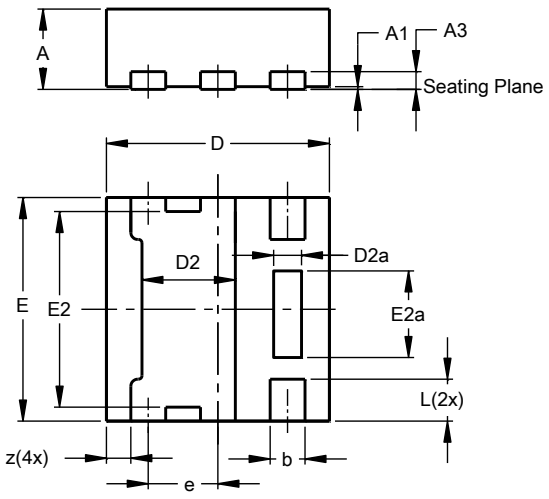


Figure 13 Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1616-6 (Type K)

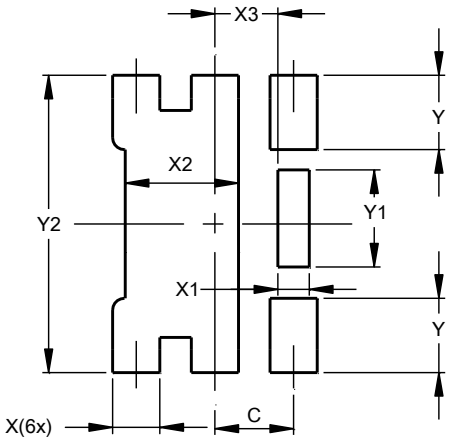


U-DFN1616-6 (Type K)			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.60	0.575
A1	0.00	0.05	0.02
A3	–	–	0.13
b	0.20	0.30	0.25
D	1.55	1.65	1.60
D2	0.57	0.77	0.67
D2a	0.10	0.30	0.20
e	–	–	0.50
E	1.55	1.65	1.60
E2	1.30	1.50	1.40
E2a	0.52	0.72	0.62
L	0.25	0.35	0.30
z	–	–	0.175
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1616-6 (Type K)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.200
X2	0.720
X3	0.400
Y	0.475
Y1	0.620
Y2	1.900

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