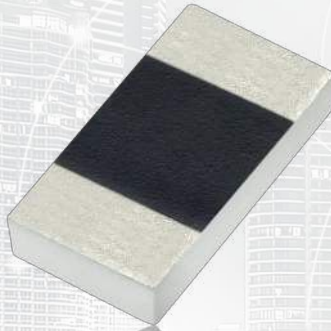




TAOGLAS®



Datasheet

DSRC / C-V2X / V2V / V2X / V2I 5900MHz Ceramic Chip Antenna

Part No:
CA.51

Description:

5.9GHz C-V2X Ceramic SMD Mount Chip Antenna

Features:

5850MHz to 5925MHz
Peak Gain 2dBi
Stable and Reliable Performance
Linear Polarized & High Efficiency
Low Profile, Compact Size
Manufactured in an IATF16949 Approved Facility
Dimensions: 1.6*0.8*0.3mm
RoHS & REACH Compliant

1. Introduction	3
2. Specifications	4
3. Antenna Characteristics	5
4. Radiation Patterns	7
5. Mechanical Drawing – Antenna	9
6. Antenna Integration Guide	10
7. Mechanical Drawing – Evaluation Board	17
8. Soldering Conditions	18
9. Packaging	19
<hr/>	
Changelog	21

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1. Introduction



The Taoglas CA.51 5.9GHz is a ceramic chip antenna specifically designed for C-V2X (& DSRC) applications and exhibits high-efficiency in a miniature SMD mount ceramic antenna with a small footprint requirement. This ceramic chip antenna uses the main PCB as its ground plane, thereby increasing antenna efficiency and decreasing the assembly cost. It is tuned for different PCB sizes by simply changing the value of the matching circuit. At 1.6mm*0.8mm*0.3mm, it is one of the smallest antennas available worldwide. This antenna is delivered on tape and reel.

C-V2X is the communications medium of choice for active safety V2V/V2X (Vehicle-to-Vehicle and Vehicle-to-Other) systems. Primarily allocated for vehicle safety applications, C-V2X supports high-speed, low-latency, short-range, V2V/V2X wireless communications.

This antenna can be mounted with no performance degradation in either orientation as long as the antenna is soldered correctly via Surface mounting. Please see the integration instructions section for further detail regarding the optimum way to integrate this antenna into your device.

For further optimization to customer-specific device environments and for support to integrate and test this antennas performance in your device, contact your regional Taoglas Customer Services Team.

Applications:

IEEE 802.11p (WAVE- Wireless Access in the Vehicular Environment)

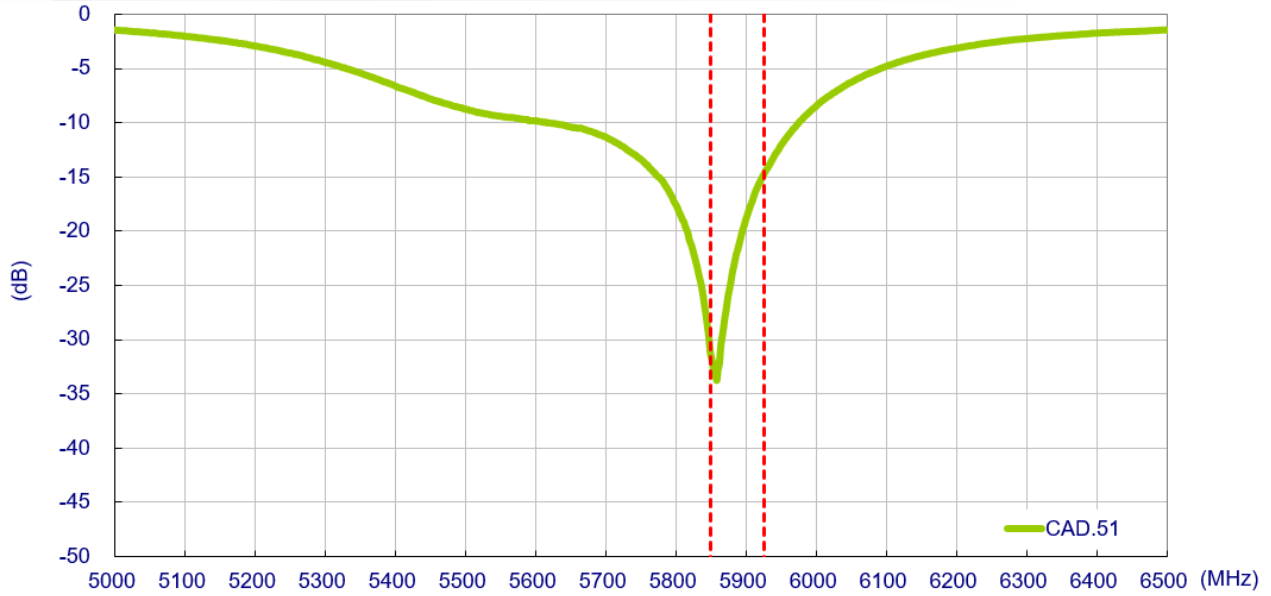
DSRC (Dedicated Short Range Communication) systems for V2V / V2I / V2X

2. Specifications

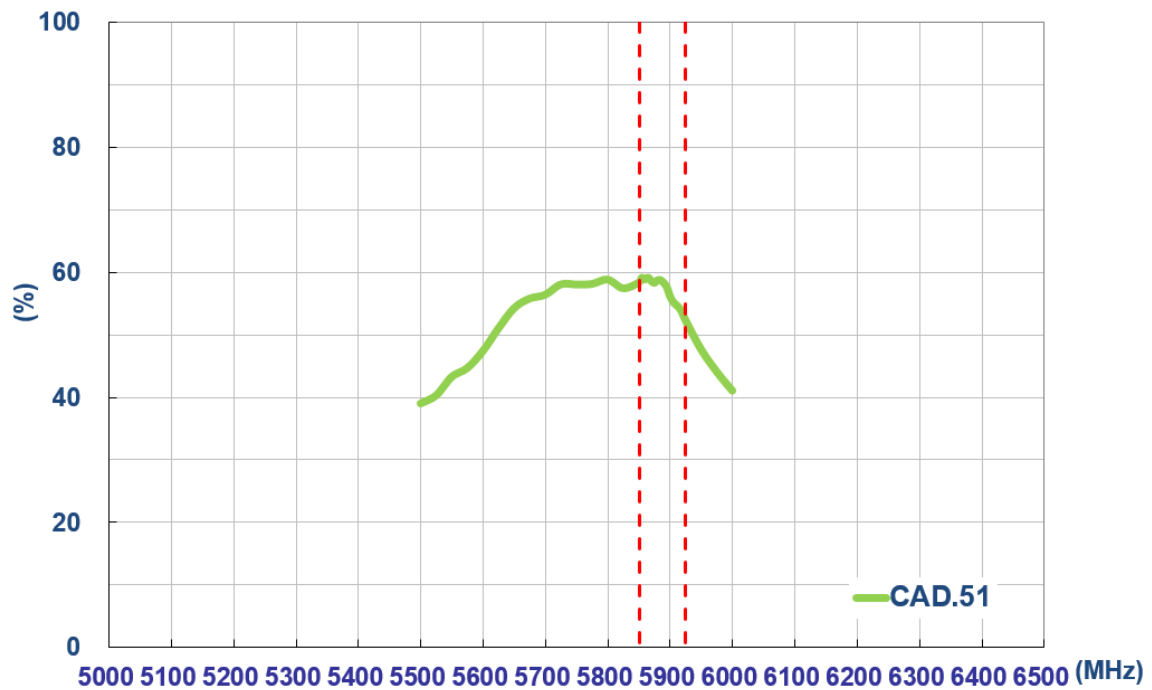
Antenna	
Frequency (MHz)	5850-5925 MHz
Efficiency (%)	
40 x 40 mm Ground Plane	57.08
Average Gain (dB)	
40 x 40 mm Ground Plane	-2.44 dB (typical)
Peak Gain (dBi)	
40 x 40 mm Ground Plane	2.87 dBi (typical)
VSWR	2 max.
Impedance (Ω)	50 Ω
Polarization	Linear
Radiation Pattern	Omni
Input Power(W)	2
Mechanical	
Dimensions (mm)	1.6 x 0.8 x 03
Ground plane (mm)	40 x 40 (Recommended)
Material	Ceramic
Environmental	
Temperature Range	-40°C to 85°C
Temperature Coefficient of Frequency (ppm/°C)	0±20 max. (@-40°C to 85°C)
Humidity	Non-condensing 65°C 95% RH
Moisture Sensitivity Level	3 (168 Hours)

3. Antenna Characteristics

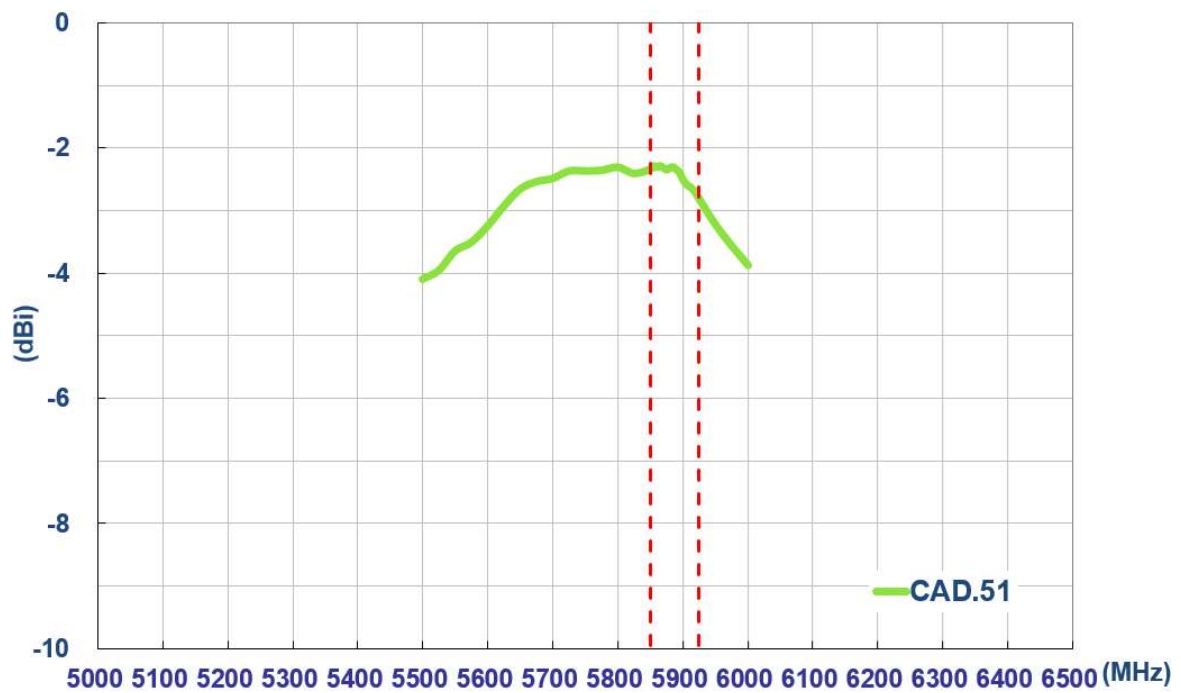
3.1 Return Loss



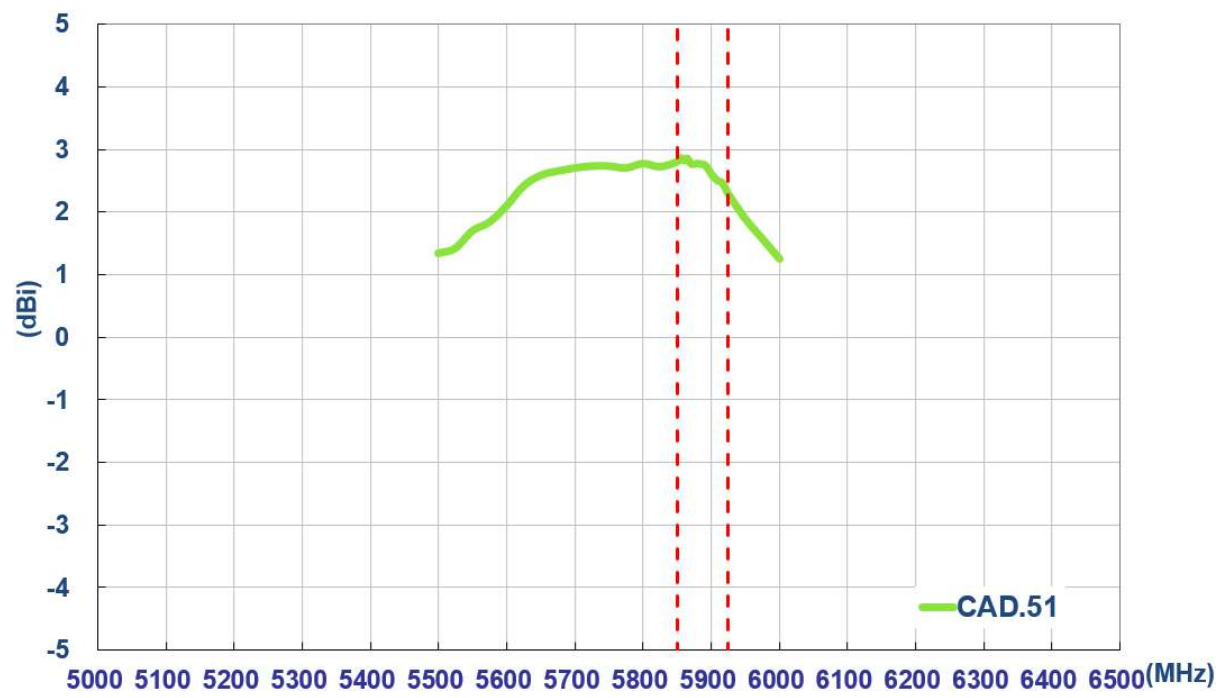
3.2 Efficiency



3.3 Average Gain



3.4 Peak Gain



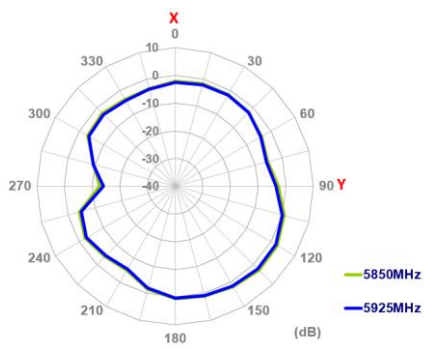
4. Radiation Patterns

4.1 Test Setup – Antenna on Evaluation Board

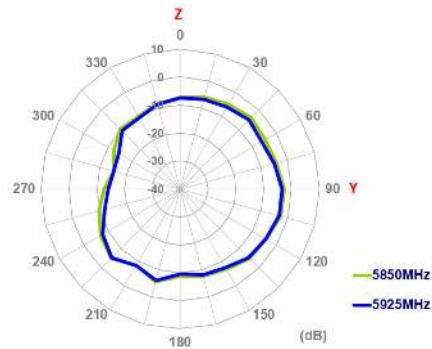


4.2 5850 - 5925MHz Radiation Patterns

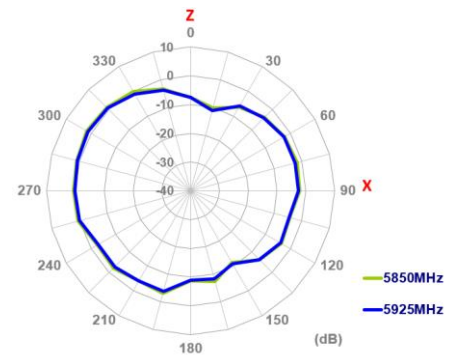
XY Plane



XY Plane Flipped

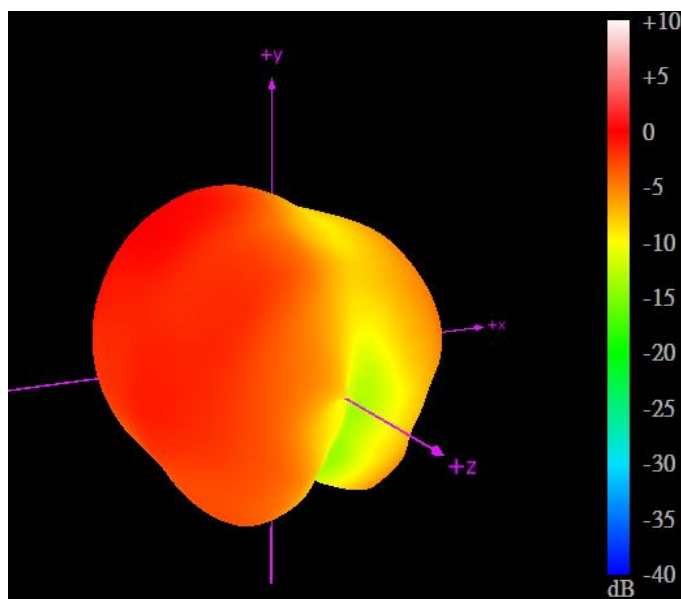


XZ Plane

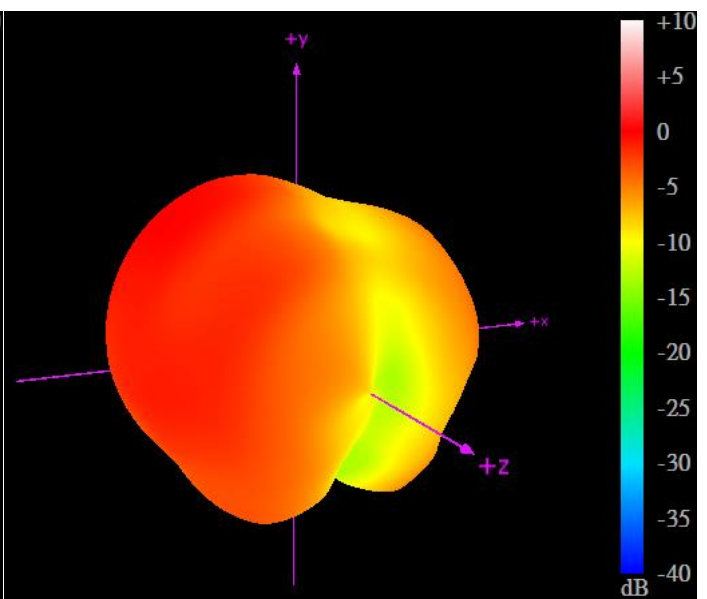


4.3 3D Radiation Pattern

5850MHz



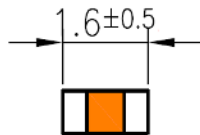
5925MHz



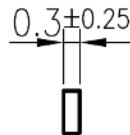
5. Mechanical Drawing – Antenna

5.1 Antenna Dimension and Drawing

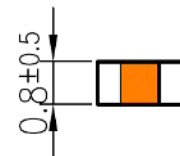
Front View



Side View



Back View



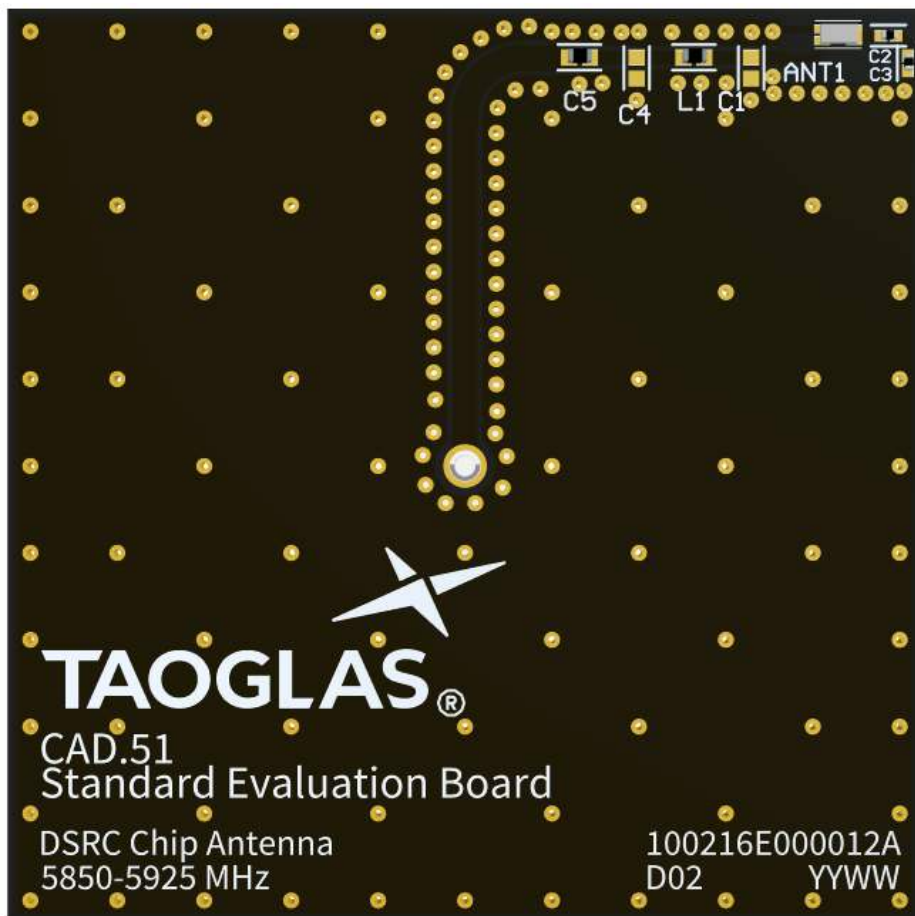
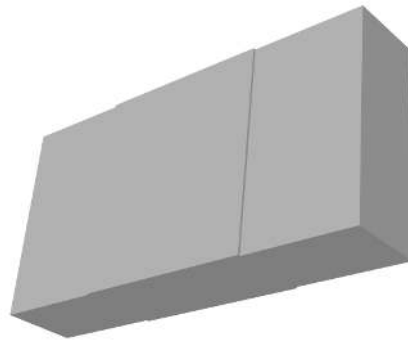
Unit: mm

5.2 Antenna Footprint

Foot Print																
<p>Top Copper</p> <p>Pad 1 and 6 should be connected to Ground. Pad 1 should be connected to a 50 ohm transmission line.</p> <p>↑ : Connected to GND ↓ : Connected to 50 ohm transmission line.</p>	<p>Top Solder Paste</p> <p>Pads 1 and 2 are the same size, Pad 3, 4, 5 and 6 are the same size.</p>															
<p>Top Solder Mask</p> <p>Pads 1 and 2 are the same size, Pad 3, 4, 5 and 6 are the same size. This drawing is a negative of solder mask. Black regions are anti-mask.</p>	<p>Composite Diagram</p>															
<p>NOTE:</p> <table border="0"> <tr> <td>1. Ag Plated area</td> <td></td> <td>6. Ground keepout should extend from top layer through all inner PCB layers to minimize coupling from RF feed to ground.</td> </tr> <tr> <td>2. Solder Mask area</td> <td></td> <td>7. Any vias in pads should be either filled or tented to prevent solder from wicking away from the pad during reflow.</td> </tr> <tr> <td>3. Copper area</td> <td></td> <td>8. The dimension tolerances should follow standard PCB manufacturing guidelines</td> </tr> <tr> <td>4. Paste area</td> <td></td> <td></td> </tr> <tr> <td>5. Copper Keepout Area</td> <td></td> <td></td> </tr> </table>		1. Ag Plated area		6. Ground keepout should extend from top layer through all inner PCB layers to minimize coupling from RF feed to ground.	2. Solder Mask area		7. Any vias in pads should be either filled or tented to prevent solder from wicking away from the pad during reflow.	3. Copper area		8. The dimension tolerances should follow standard PCB manufacturing guidelines	4. Paste area			5. Copper Keepout Area		
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5. Copper Keepout Area																

*Taoglas is able to provide CAD drawing file to customers for evaluation.

6. Antenna Integration Guide

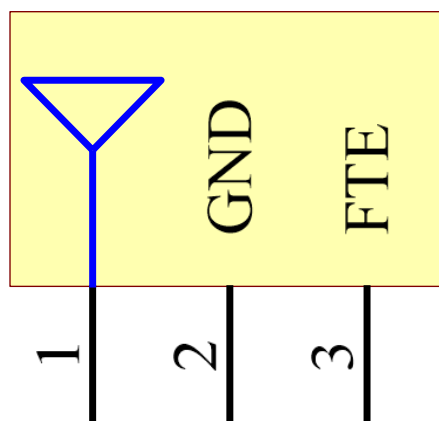


6.1 Schematic Symbol and Pin Definition

The circuit symbol for the antenna is shown below. The antenna has 3 pins with all three pins as functional.

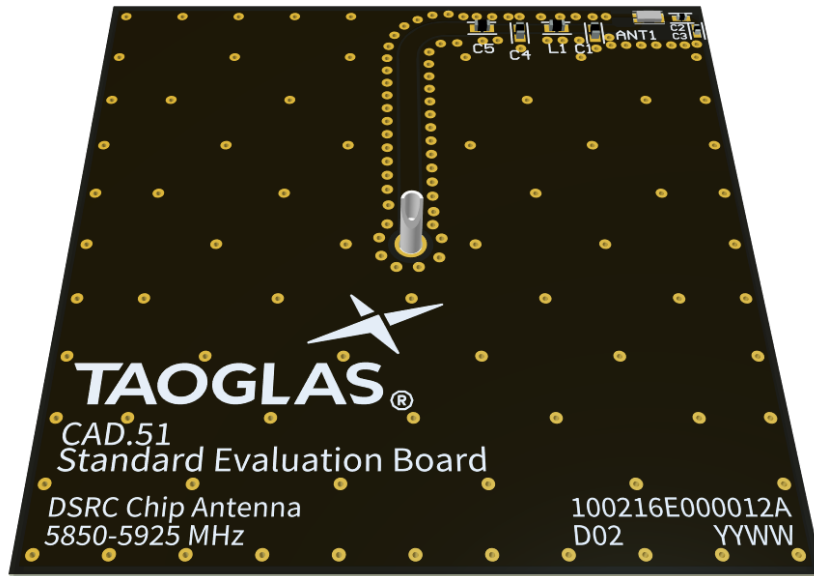
Pin	Description
1	RF Feed
2	Ground
3	FTE

CA.51
ANT1



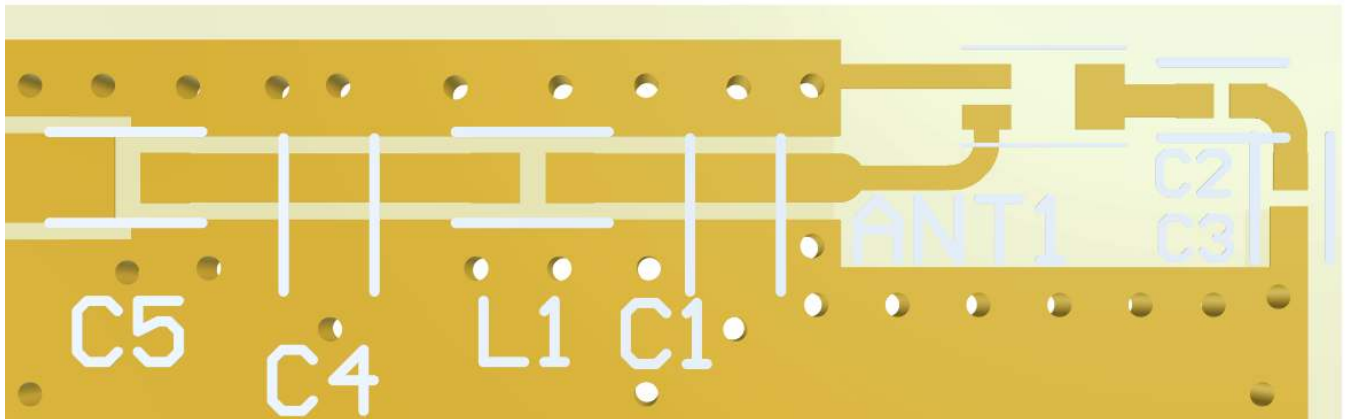
6.2 Antenna Integration

Whatever the size of the PCB, the antenna should ideally be placed on the PCB's longest side, to take advantage of the ground plane. Optimized matching components can be placed as shown.

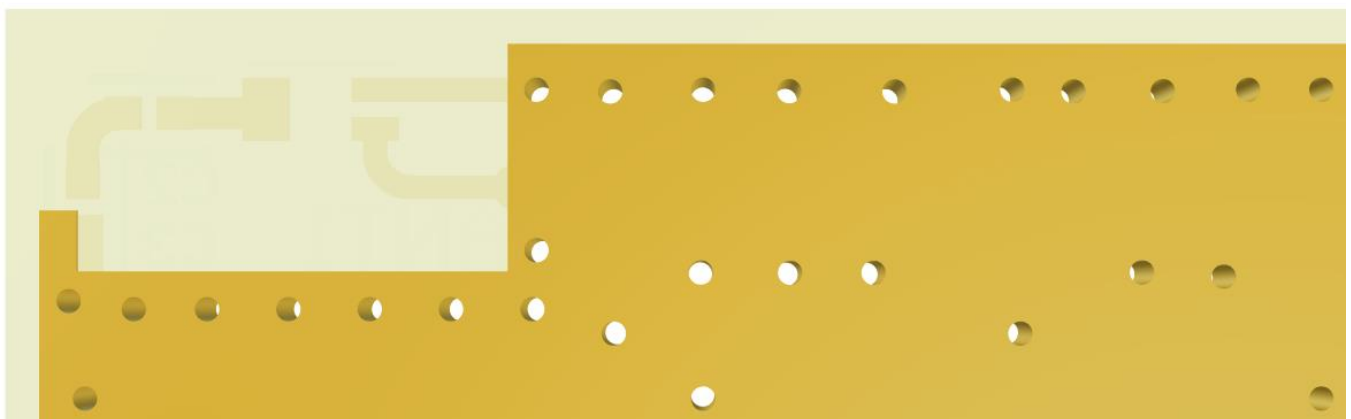


6.3 PCB Layout

The footprint and clearance on the PCB must meet the layout drawing in (Footprint Drawing). Note the placement of the optimized components. L1 is placed as close as possible to the RF feed (pad 1) but still within the transmission line. C5 is then placed tightly in series after that. C2 is placed as close as possible to the Tuning feed (pad 3) followed by C3 connecting to ground. C1 & C4 are optional components but the footprints are recommended in case they are needed.



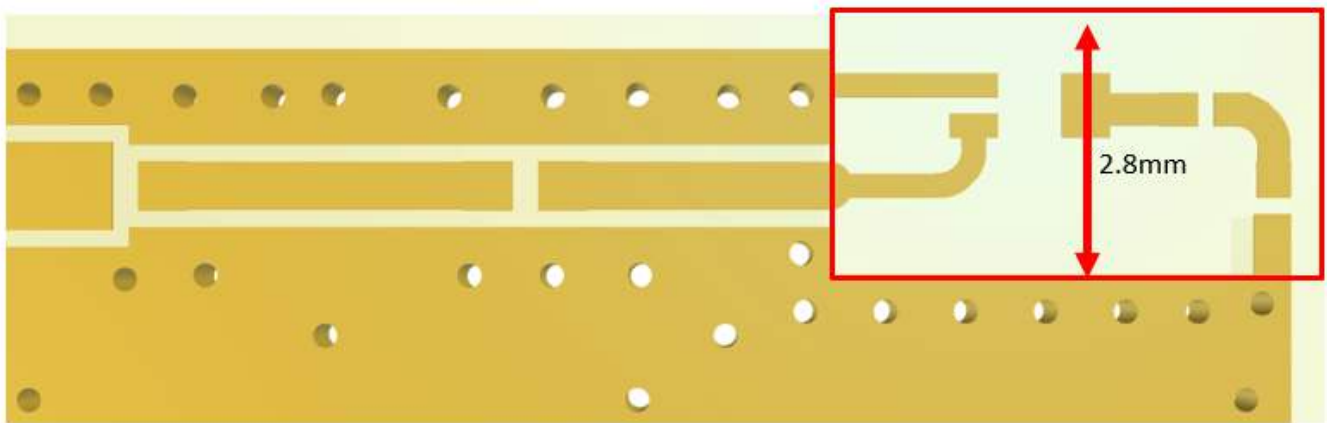
Topside



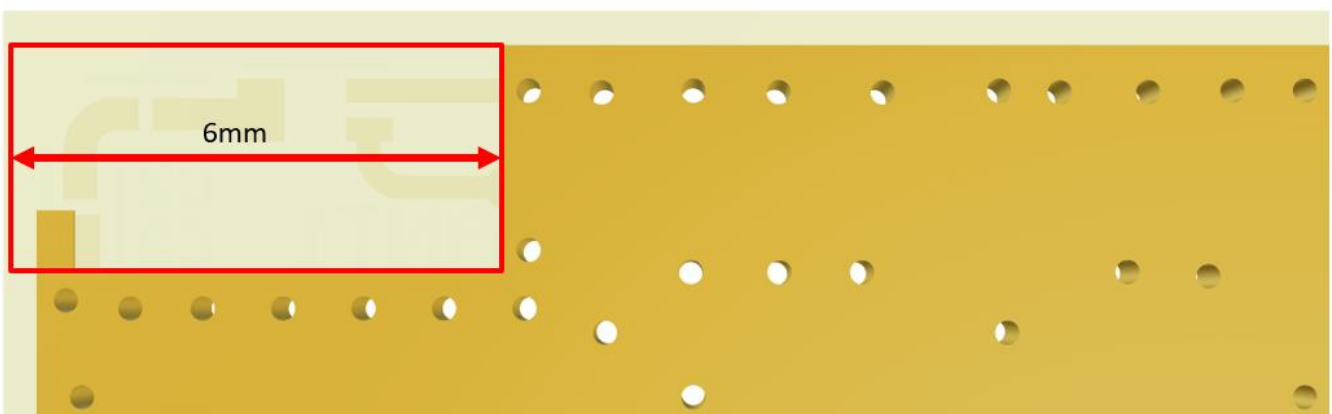
Bottom Side

6.4 PCB Keep Out

Below shows the antenna footprint and clearance through ALL layers on the PCB. Only the antenna pads and connections to feed and GND are present within this clearance area (marked RED). The clearance area extends to 6mm in width and 2.6mm in length from the corner of the PCB. This clearance area includes the bottom side and ALL internal layers on the PCB.

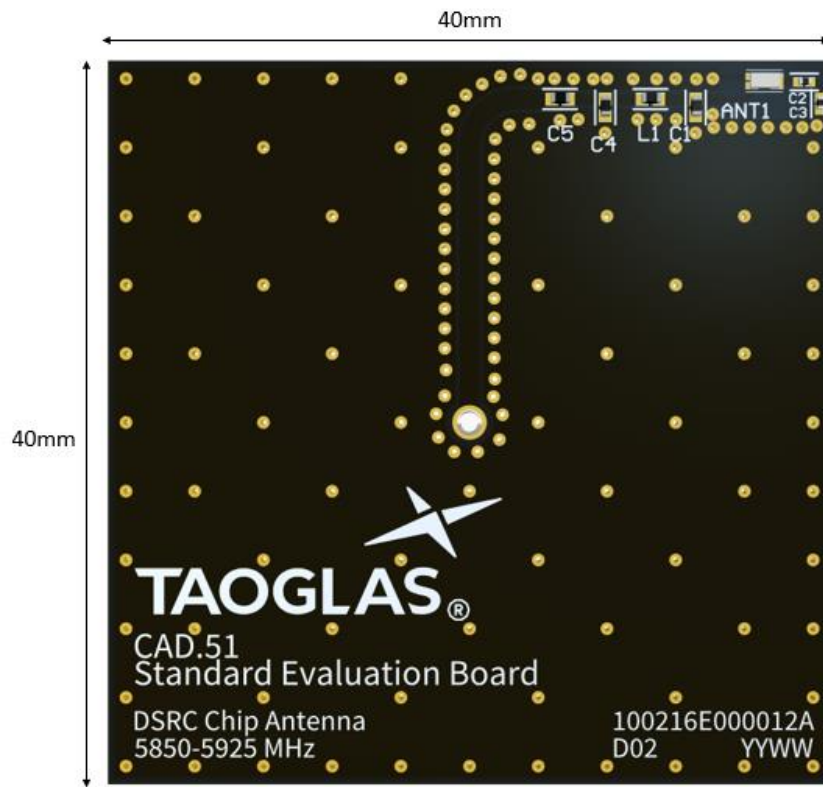


Topside

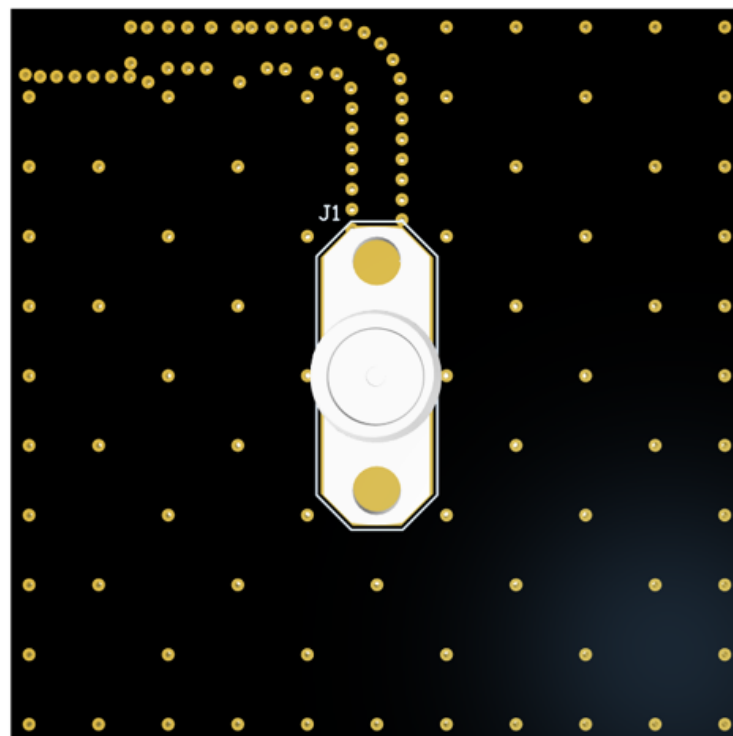


Bottom Side

6.5 Evaluation Board



Topside

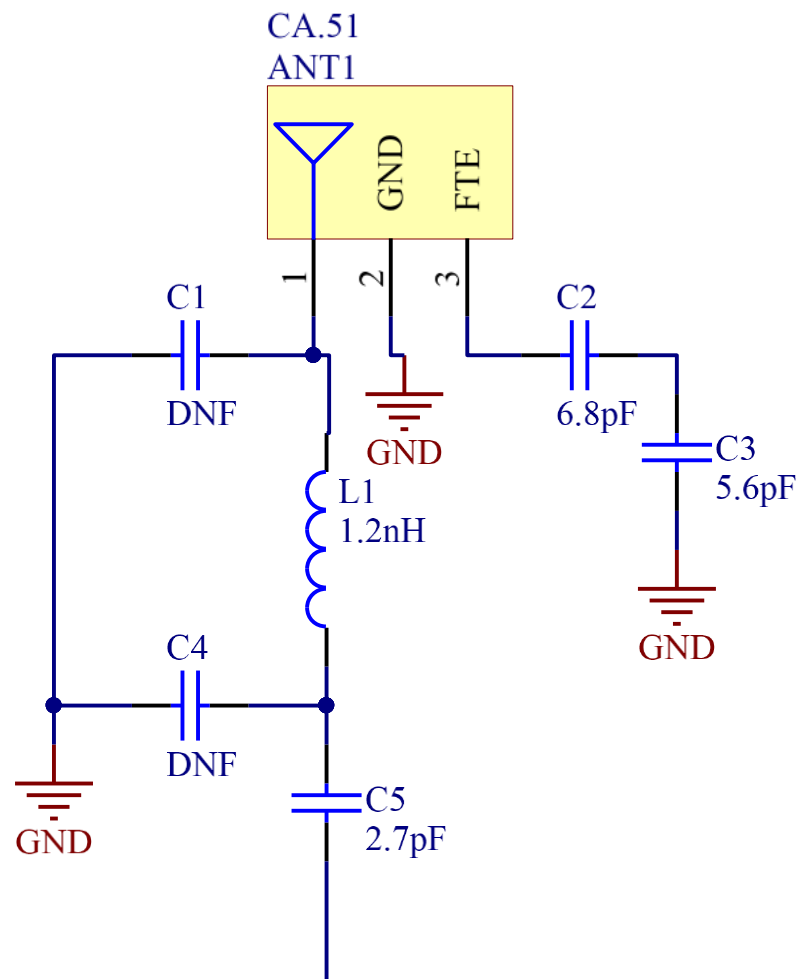


Bottom Side

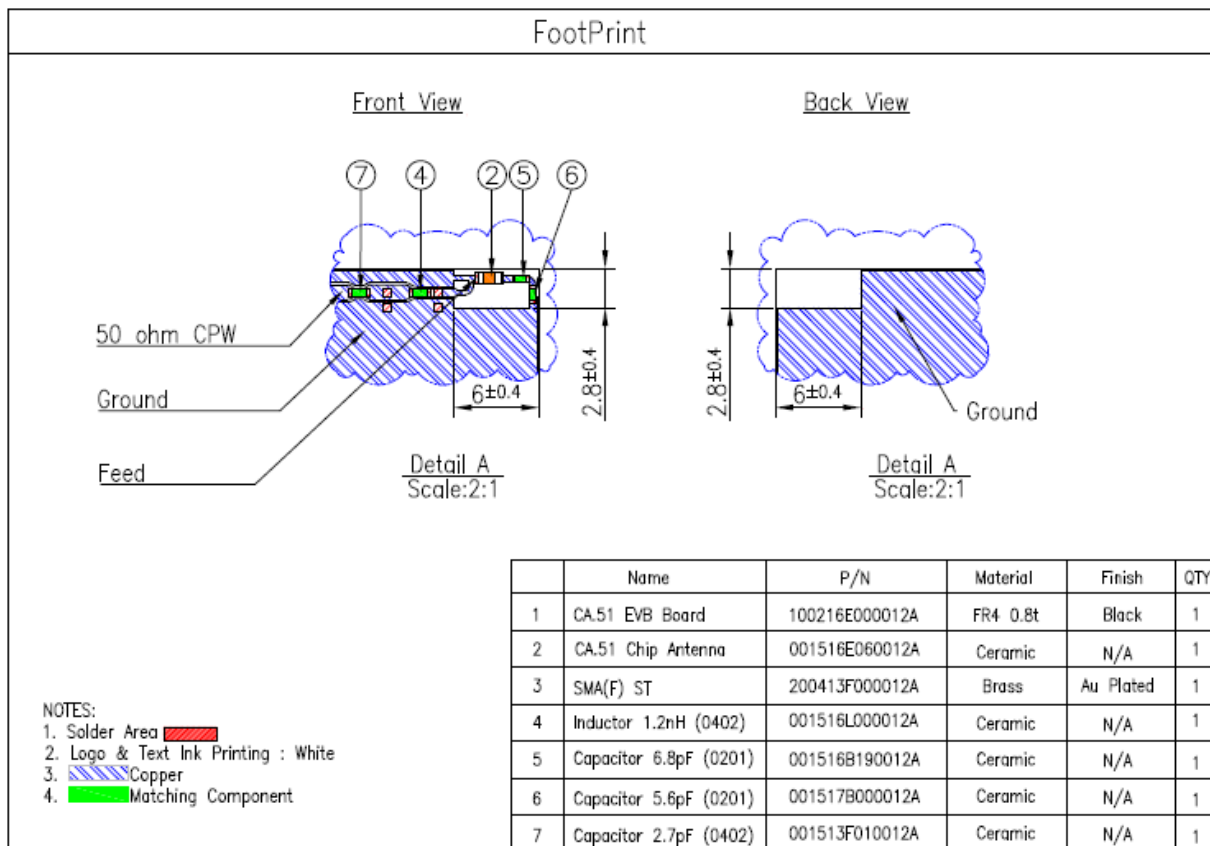
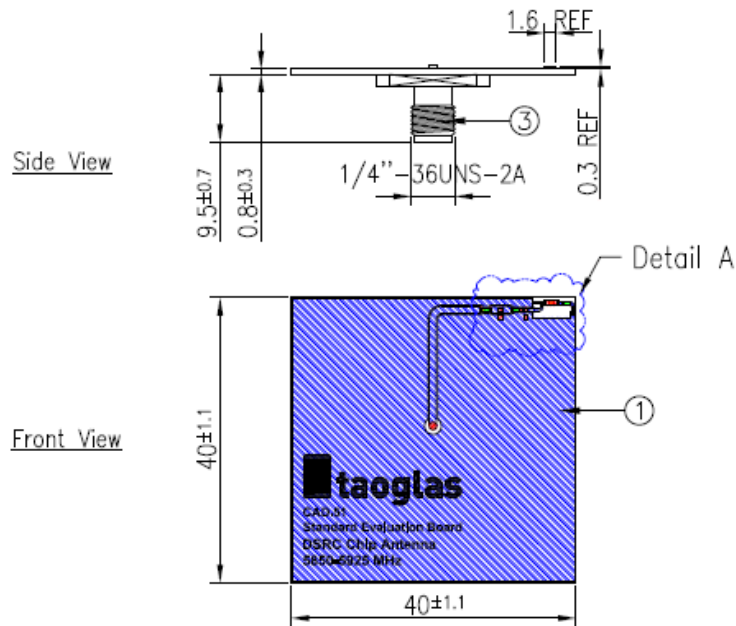
6.6 Evaluation Board Matching Circuit

A matching component (L1) in series with the CA.51 is required for the antenna to have optimal performance on the evaluation board, located outside of the ground plane in the space specified in the above images. Additional matching components may be necessary for your device, so we recommend incorporating extra component footprints, forming a “pi” network, between the cellular module and the edge of the ground plane.

Designator	Type	Value	Manufacturer	Manufacturer Part Number
L1	Inductor	8.7nH	TDK	
C1, C4	Capacitor	DNF	-	-
C2	Capacitor	6.8pF	Murata	GRM0335C1H6R8CA01D
C3	Capacitor	5.6pF	Murata	GRM0335C1H5R6CA01D
C5	Capacitor	2.7pF	Murata	GRM1555C1H2R7CA01D

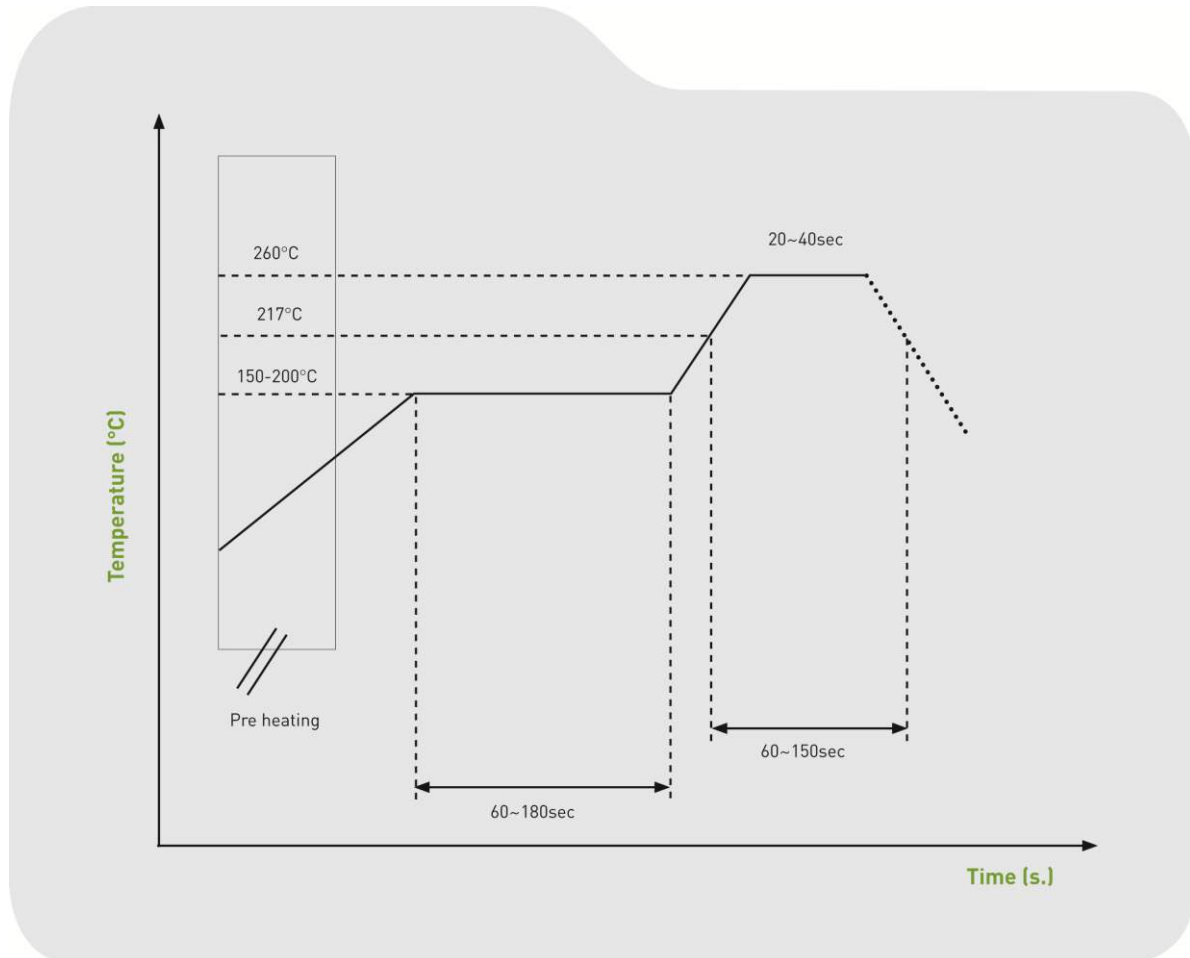


7. Mechanical Drawing – Evaluation Board



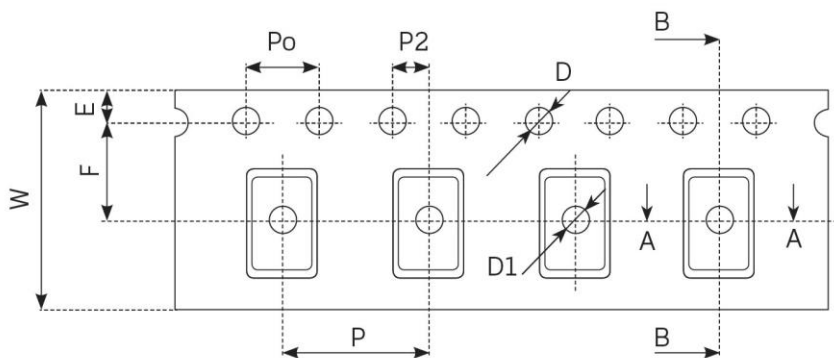
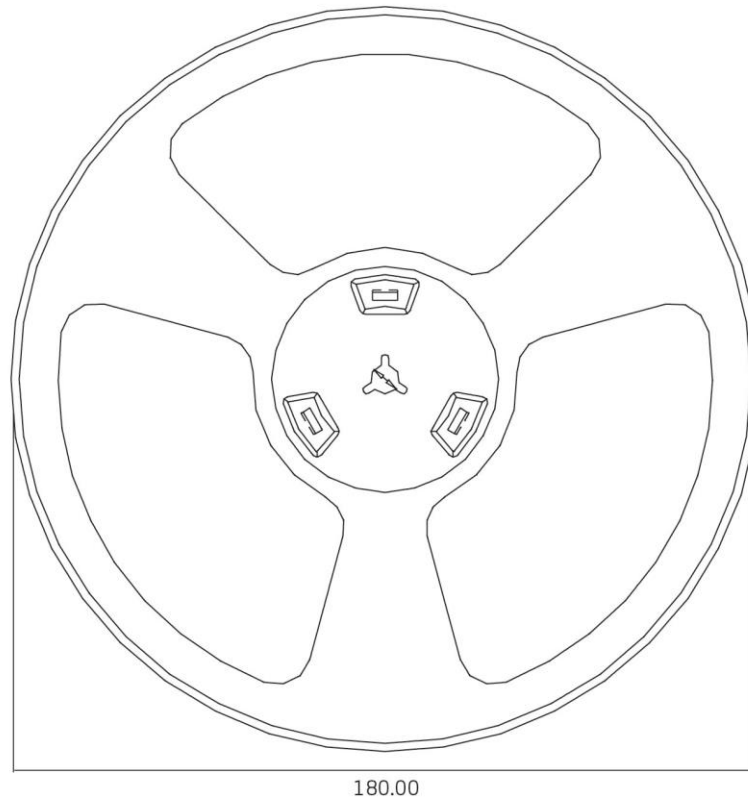
8. Soldering Conditions

Typical Soldering profile for lead-free process:



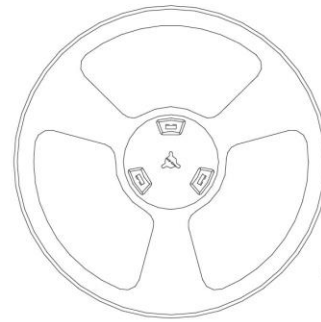
9. Packaging

5000 pc CA.51 per reel
 Dimensions - Ø180*11mm
 Weight - 159.8g

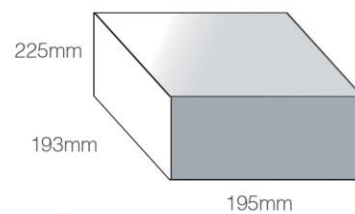


W : 12.00mm
 P : 8.00mm
 E : 1.75mm
 F : 5.50mm
 P2 : 2.00mm
 D : 1.50mm
 D1 :
 Po : 4.00mm

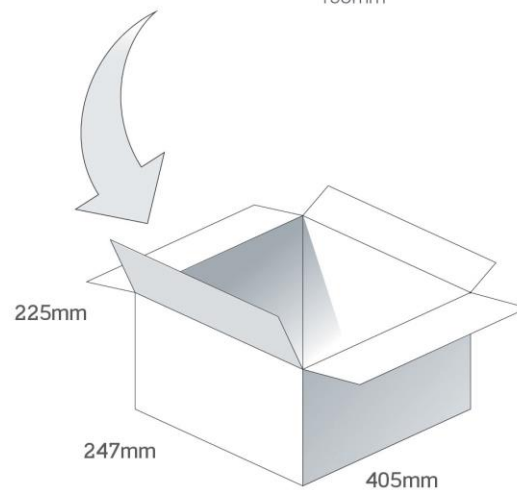
5000 pcs CA.51 reel
 Dimensions - 180*180*11mm
 Weight - 159.8g



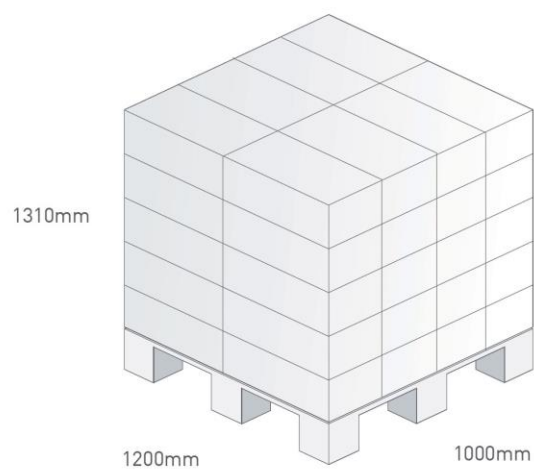
50,000 pcs CA.51 / 10 Reel in small box
 Dimensions - 193*225*195mm
 Weight - 1.6Kg



2 small boxes, 100,000 pcs in one carton
 Carton Dimensions - 247*405*225mm
 Weight - 3.2Kg



Pallet Dimensions 1200*1000*1310mm
 40 Cartons per Pallet
 8 Cartons per layer
 5 Layers



Changelog for the datasheet

SPE-17-8-032 – CA.51

Revision: D (Current Version)

Date:	2021-10-04
Changes:	Integration Guide Added
Changes Made by:	Cesar Sousa

Previous Revisions

Revision: C

Date:	2021-10-04
Changes:	Format Change, MSL
Changes Made by:	Erik Landi

Revision: B

Date:	2019-10-25
Changes:	Updated to C-V2X
Changes Made by:	Jack Conroy

Revision: A (Original First Release)

Date:	2017-05-22
Notes:	Initial Release
Author:	STAFF



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