1:1 AND 1:2 REGISTERED BUFFER WITH 1.8V SSTL I/O

IDT74SSTU32864/ A/C/D/G

FEATURES:

- 1:1 and 1:2 registered buffer
- 1.8V Operation
- SSTL_18 style clock and data inputs
- Differential CLK input
- Control inputs compatible with LVCMOS levels
- Flow-through architecture for optimum PCB design
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Maximum operating frequency: 340MHz
- Available in 96-pin LFBGA package

APPLICATIONS:

- Ideally suited for DDR2-400/533 (PC2 - 3200/ 4200) registered DIMM applications
- Along with CSPU877/A/D, zero delay PLL clock buffer, provides complete solution for DDR2-400/533 DIMMs
- SSTU32864 is optimized for DDR2 Raw cards B and C
- SSTU32864A is optimized for DDR2 Raw card A
- SSTU32864C/D/G are optimized for DDR2 Raw cards A, B, and C
- SSTU32864G has control pins for output slew rate control

DESCRIPTION:

The SSTU32864 is a 25-bit 1:1 / 14-bit 1:2 configurable registered buffer designed for 1.7V to 1.9V V_{DD} operation. All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32864 operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high and $\overline{CLK}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from the A configuration (when low) to B configuration (when high). The C1 input controls the configuration from the 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

This device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{RESET}$ and Cx inputs must always be held at a valid logic high or low level.

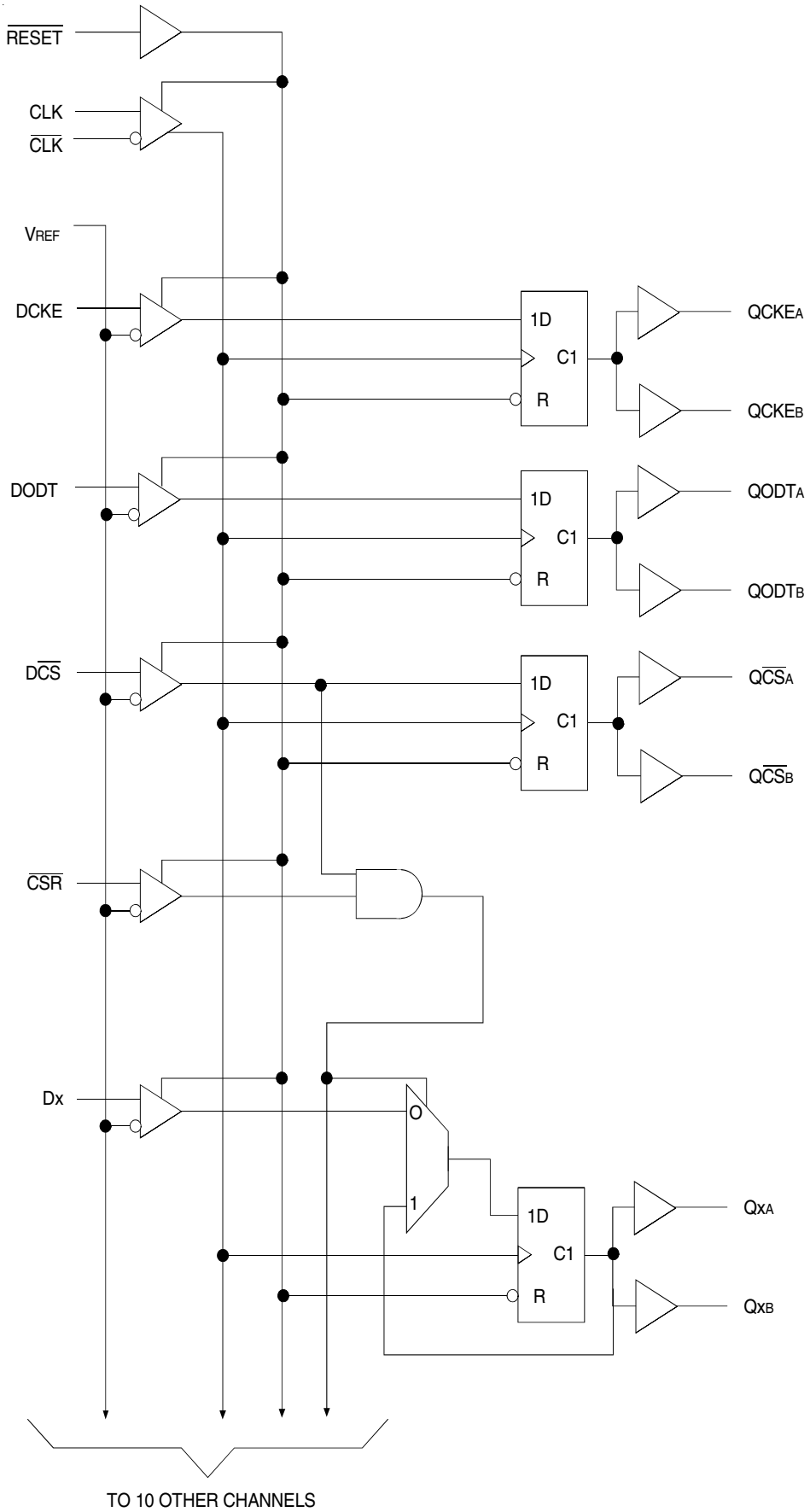
To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CLK and $\overline{CLK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of a reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the SSTU32864 must ensure that the outputs will remain low, thus ensuring no glitches on the outputs.

The device monitors both D$\overline{CS}$ and $\overline{CSR}$ inputs and will gate the outputs from changing states when both D$\overline{CS}$ and $\overline{CSR}$ inputs are high. If either D$\overline{CS}$ or $\overline{CSR}$ input is low, the device will function normally. The $\overline{RESET}$ input has priority over the D$\overline{CS}$ control and will force the inputs low. If the D$\overline{CS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hard-wired to ground, in which case the set-up time requirement for D$\overline{CS}$ would be the same as for the other D data inputs.

The SSTU32864G has two slew control pins (Z_{OH} and Z_{OL}) used to optimize the signal integrity on the DIMM.

FUNCTIONAL BLOCK DIAGRAM (1:2)



PIN CONFIGURATION (TYPE A)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	QCKEB	Q2B	Q3B	QODTB	Q5B	Q6B	C0	$\overline{QCS}$B	ZOL	Q8B	Q9B	Q10B	Q11B	Q12B	Q13B	Q14B
5	QCKEA	Q2A	Q3A	QODTA	Q5A	Q6A	C1	$\overline{QCS}$A	ZOH	Q8A	Q9A	Q10A	Q11A	Q12A	Q13A	Q14A
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	NC	NC	NC	NC	NC	$\overline{RESET}$	D$\overline{CS}$	$\overline{CSR}$	NC	NC	NC	NC	NC	NC	NC
1	DCKE	D2	D3	DODT	D5	D6	NC	CLK	$\overline{CLK}$	D8	D9	D10	D11	D12	D13	D14

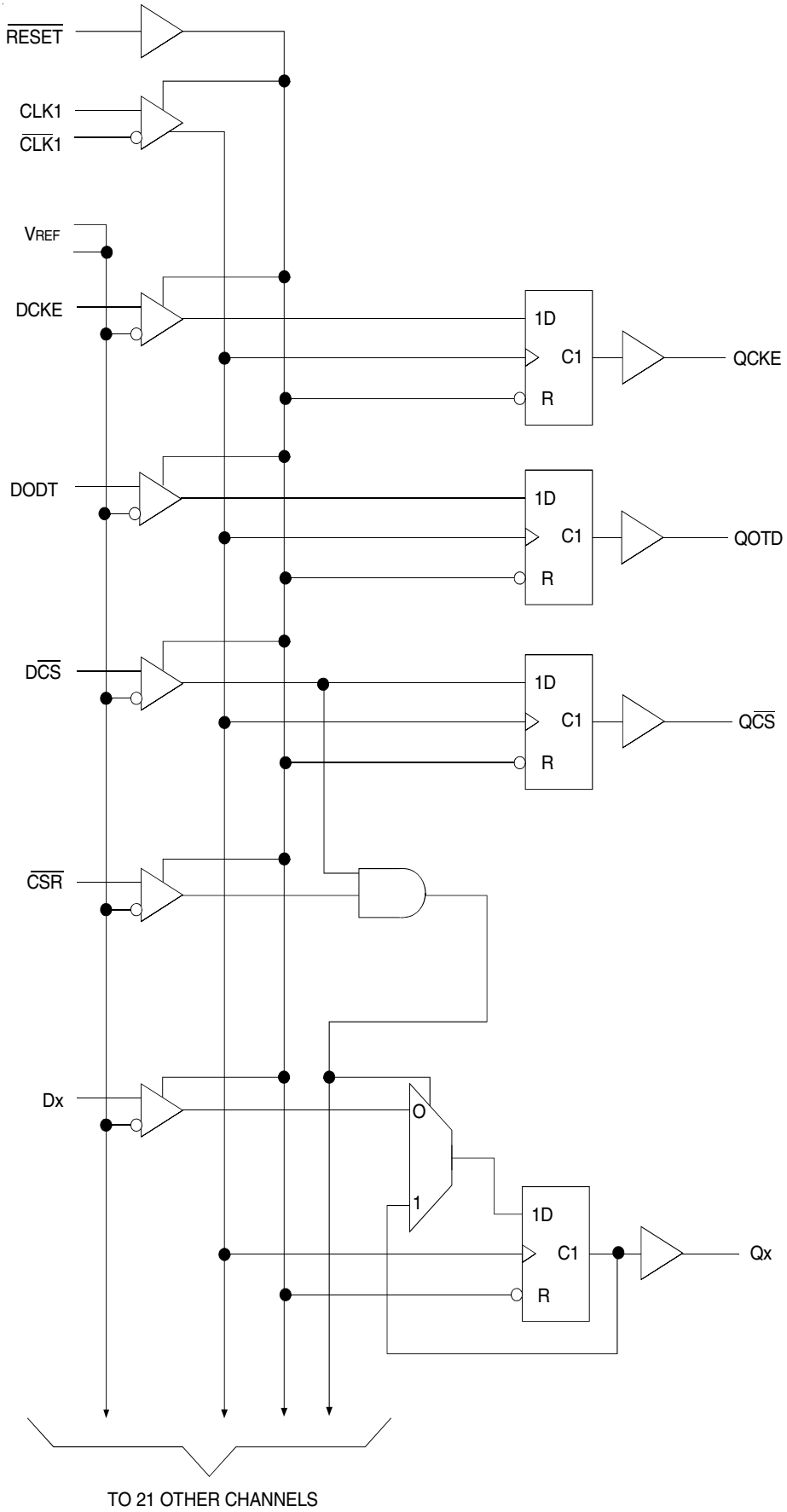
96-PIN LFBGA
1:2 REGISTER (TYPE A, FRONTSIDE)
TOP VIEW

PIN CONFIGURATION (TYPE B)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	Q1B	Q2B	Q3B	Q4B	Q5B	Q6B	C0	$\overline{QCS}$B	ZOL	Q8B	Q9B	Q10B	QODTB	Q12B	Q13B	QCKEB
5	Q1A	Q2A	Q3A	Q4A	Q5A	Q6A	C1	$\overline{QCS}$A	ZOH	Q8A	Q9A	Q10A	QODTA	Q12A	Q13A	QCKEA
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	NC	NC	NC	NC	NC	$\overline{RESET}$	D$\overline{CS}$	$\overline{CSR}$	NC	NC	NC	NC	NC	NC	NC
1	D1	D2	D3	D4	D5	D6	NC	CLK	$\overline{CLK}$	D8	D9	D10	DODT	D12	D13	DCKE

96-PIN LFBGA
1:2 REGISTER (TYPE B, BACKSIDE)
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM (1:1)



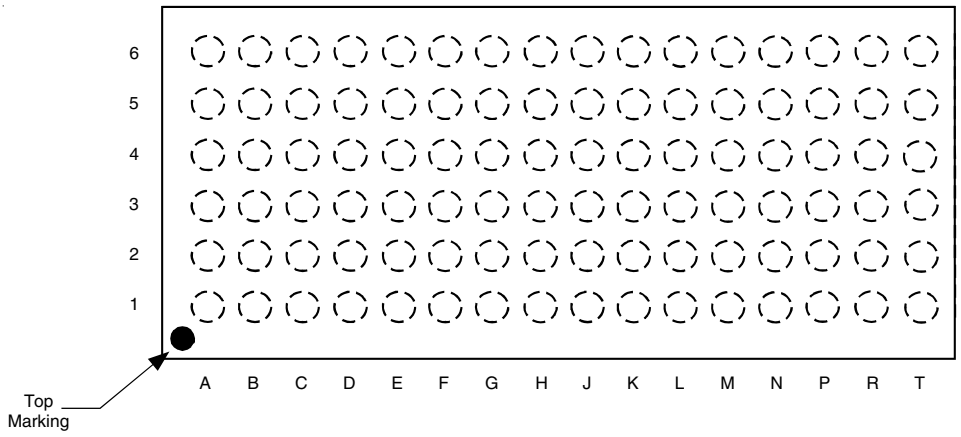
PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	NC	Q15	Q16	NC	Q17	Q18	C0	NC	ZOL	Q19	Q20	Q21	Q22	Q23	Q24	Q25
5	QCKE	Q2	Q3	QODT	Q5	Q6	C1	$\overline{QCS}$	ZOH	Q8	Q9	Q10	Q11	Q12	Q13	Q14
4	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD
3	VREF	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VREF
2	NC	D15	D16	NC	D17	D18	$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	D19	D20	D21	D22	D23	D24	D25
1	DCKE	D2	D3	DODT	D5	D6	NC	CLK	$\overline{CLK}$	D8	D9	D10	D11	D12	D13	D14

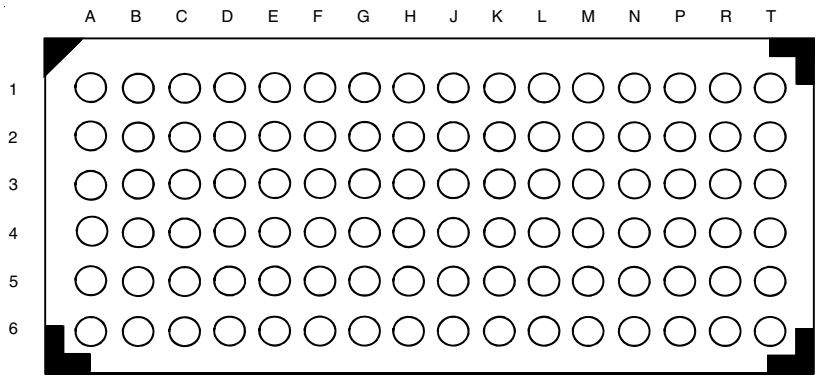
*Rows 3 and 4 are reserved for VDD and GND.

96-PIN LFBGA
1:1 REGISTER
TOP VIEW

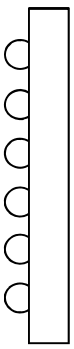
96 BALL LFBGA PACKAGE ATTRIBUTES



TOP VIEW



BOTTOM VIEW



SIDE VIEW

FUNCTION TABLE (EACH FLIP-FLOP) (1)

Inputs						Qx	$Q\overline{CS}x$	QODTx, QCKEx
$\overline{RESET}$	$D\overline{CS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dx, DODT, DCKE	Outputs	Output	Outputs
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
H	H	H	↑	↓	L	Q_0(2)	H	L
H	H	H	↑	↓	H	Q_0(2)	H	H
H	H	H	L or H	L or H	X	Q_0(2)	Q_0(2)	Q_0(2)
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Output level before the indicated steady-state conditions were established.

MODE SELECT

C_0	C_1	Device Mode
0	0	1:1 25-bit to 25-bit
0	1	1:2 14-bit to 28-bit, Front (Type A)
1	0	Reserved
1	1	1:2 14-bit to 28-bit, Back (Type B)

OUTPUT CONTROL (SSTU32864G)

Z_{OH}	Z_{OL}	Output Slew Rate
0	0	Standard
0	1	Highest
1	0	Low
1	1	High

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description		Max.	Unit
V_{DD}	Supply Voltage Range		–0.5 to 2.5	V
V_I(2,3)	Input Voltage Range		–0.5 to 2.5	V
V_O(2,3)	Output Voltage Range		–0.5 to V_{DD} +0.5	V
I_{IK}	Input Clamp Current	V_I < 0	±50	mA
		V_I > V_{DD}		
I_{OK}	Output Clamp Current	V_O < 0	±50	mA
		V_O > V_{DD}		
I_O	Continuous Output Current, V_O = 0 to V_{DD}		±50	mA
V_{DD}	Continuous Current through each V_{DD} or GND		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. This value is limited to 2.5V maximum.

TERMINAL FUNCTIONS (ALL PINS)

Terminal Name	Electrical Characteristics	Description
GND	Ground Input	Ground
V_{DD}	1.8V nominal	Power Supply Voltage
V_{REF}	0.9V nominal	Input Reference Voltage
Z_{OH}(1)	LVCMOS	Output Slew Rate Control
Z_{OL}(1)	LVCMOS	Output Slew Rate Control
CLK	Differential Input	Positive Master Clock Input
$\overline{CLK}$	Differential Input	Negative Master Clock Input
Cx	LVCMOS Input	Configuration Control Inputs
$\overline{RESET}$	LVCMOS Input	Asynchronous Reset Input. Resets registers and disables V_{REF} data and clock differential-input receivers.
$\overline{CSR}$, D$\overline{CS}$	SSTL_18 Input	Chip Select Inputs. Disables outputs Dx switching when both inputs are HIGH.
Dx	SSTL_18 Input	Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$.
DODT	SSTL_18 Input	The outputs of this register bit will not be suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls
DCKE	SSTL_18 Input	The outputs of this register bit will not be suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls
Qx	1.8V CMOS	Data Outputs that are suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls
Q$\overline{CS}$x	1.8V CMOS	Data Output that will not be suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls
QODTx	1.8V CMOS	Data Output that will not be suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls
QCKEx	1.8V CMOS	Data Output that will not be suspended by the D$\overline{CS}$ and $\overline{CSR}$ controls

NOTE:
1. The signals will be left unconnected for the SSTU32864/A/C/D.

OPERATING CHARACTERISTICS, T_A = 25ºC (1,2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.7	—	1.9	V
V_{REF}	Reference Voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination Voltage		V_{REF}– 40mV	V_{REF}	V_{REF}+ 40mV	V
V_I	Input Voltage		0	—	V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Data Inputs	V_{REF}+ 250mV	—	—	V
V_{IL}	AC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 250mV	V
V_{IH}	DC High-Level Input Voltage	Data Inputs	V_{REF}+ 125mV	—	—	V
V_{IL}	DC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 125mV	V
V_{IH}	High-Level Input Voltage	$\overline{RESET}$, Cx	0.65 * V_{DD}	—	—	V
V_{IL}	Low-Level Input Voltage	$\overline{RESET}$, Cx	—	—	0.35 * V_{DD}	V
V_{ICR}	Common Mode Input Voltage	CLK, $\overline{CLK}$	0.675	—	1.125	V
V_{ID}	Differential Input Voltage	CLK, $\overline{CLK}$	600	—	—	mV
I_{OH}	High-Level Output Current		—	—	–8	mA
I_{OL}	Low-Level Output Current		—	—	8	
T_A	Operating Free-Air Temperature		0	—	70	° C

NOTES:
1. The $\overline{RESET}$ and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0° C to +70° C, V_{DD} = 1.8V ±0.1V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}		V_{DD} = 1.7V to 1.9V, I_{OH} = –6mA		1.2	—	—	V
V_{OL}		V_{DD} = 1.7V to 1.9V, I_{OL} = 6mA		—	—	0.5	V
I_I	All Inputs	V_I = V_{DD} or GND		–5	—	5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = GND		—	—	100	µA
	Static Operating	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$		—	—	40	mA
I_{DDD}	Dynamic Operating (Clock Only)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle.		—	—	—	µA/Clock MHz
	Dynamic Operating (Per Each Data Input)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	1:1 Mode	—	—	—	µA/Clock MHz/Data Input
			1:2 Mode	—	—	—	
C_I	Data Inputs	V_I = V_{REF} ± 250mV		2.5	—	3.5	pF
	CLK and $\overline{CLK}$	V_{ICR} = 0.9V, V_{ID} = 600mV		2	—	3	
	$\overline{RESET}$	V_I = V_{DD} or GND		2	—	4	

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter		V_{DD} = 1.8V ± 0.1V		Unit
			Min.	Max.	
f_{CLOCK}(1)	Clock Frequency		—	340	MHz
t_w	Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW		1	—	ns
t_{ACT}(2)	Differential Inputs Active Time		—	10	ns
t_{INACT}(3)	Differential Inputs Inactive Time		—	15	ns
t_{SU}	Setup Time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ HIGH	0.7	—	ns
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ LOW	0.5	—	
		DODT, $\overline{CSR}$, Data, and DCKE before CLK↑, $\overline{CLK}$↓	0.5	—	
t_H	Hold Time	Data, $\overline{DCS}$, $\overline{CSR}$, DCKE, and DODT after CLK↑, $\overline{CLK}$↓	0.5	—	ns

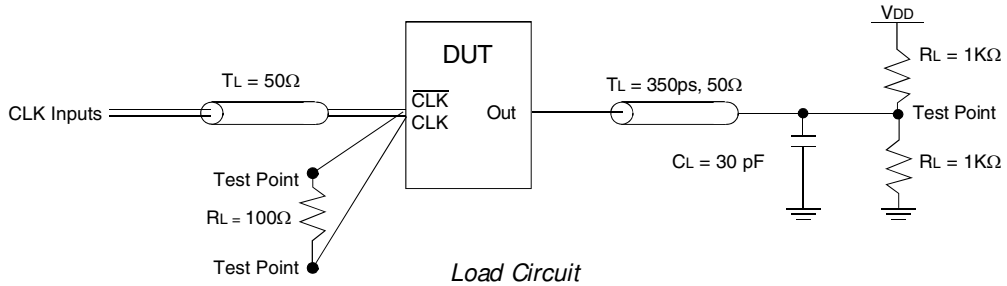
NOTES:
1. 270MHz max clock frequency for parts assembled and tested prior to WW37.
2. Data and V_{REF} inputs must be low a minimum time of t_{ACT} max, after $\overline{RESET}$ is taken HIGH.
3. Data, V_{REF}, and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max, after $\overline{RESET}$ is taken LOW.

SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) (1)

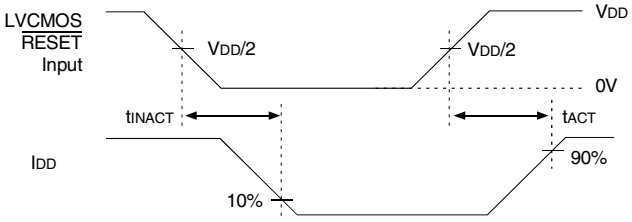
Symbol	Parameter	V_{DD} = 1.8V ± 0.1V		Unit
		Min	Max.	
f_{MAX}		340	—	MHz
t_{PDM}(2)	CLK and $\overline{CLK}$ to Q	1.41	2.15	ns
t_{PDMSS}(2,3)	CLK and $\overline{CLK}$ to Q (simultaneous switching)	—	2.35	ns
t_{RPHL}	$\overline{RESET}$ to Q	—	3	ns
dV/dt_r	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt_f	Output slew rate from 20% to 80%	1	4	V/ns
dV/dt_Δ(4)	Output slew rate from 20% to 80%	—	1	V/ns

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS.
2. Includes 350ps of test load transmission line delay.
3. This parameter is not production tested.
4. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

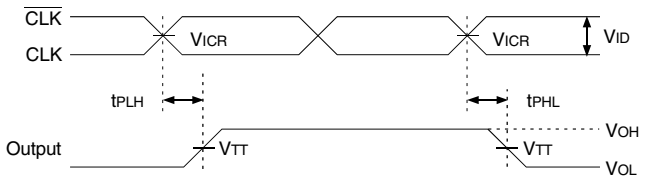
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 1.8V ± 0.1V)



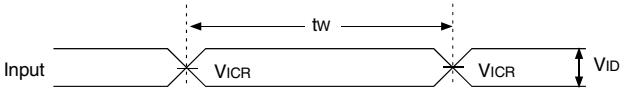
Load Circuit



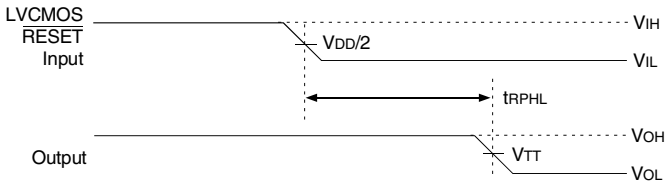
Voltage and Current Waveforms
Inputs Active and Inactive Times



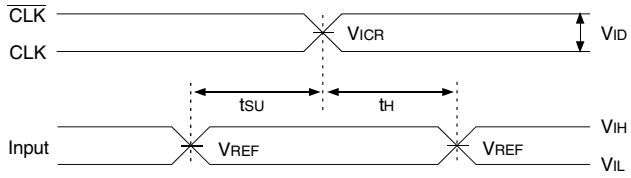
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



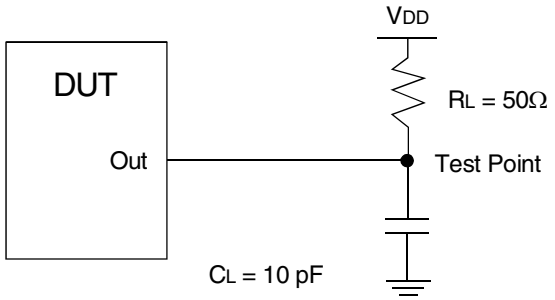
Voltage Waveforms - Propagation Delay Times



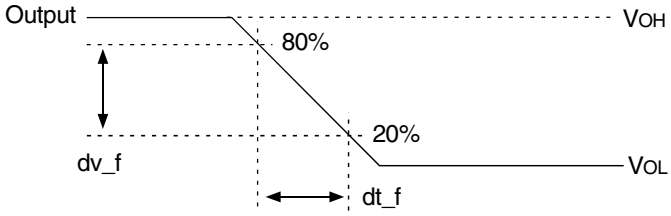
Voltage Waveforms - Setup and Hold Times

NOTES:
1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{TT} = V_{REF} = V_{DD}/2
6. V_{IH} = V_{REF} + 250mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV.
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

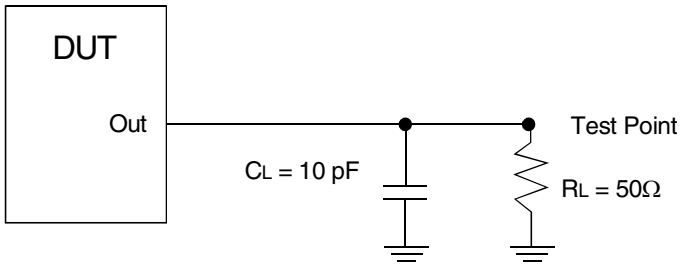
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 1.8V ± 0.1V)



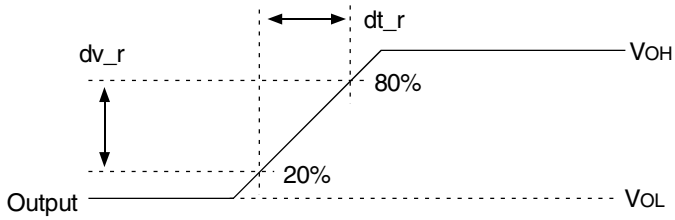
Load Circuit: High-to-Low Slew-Rate Adjustment



Voltage Waveforms: High-to-Low Slew-Rate Adjustment



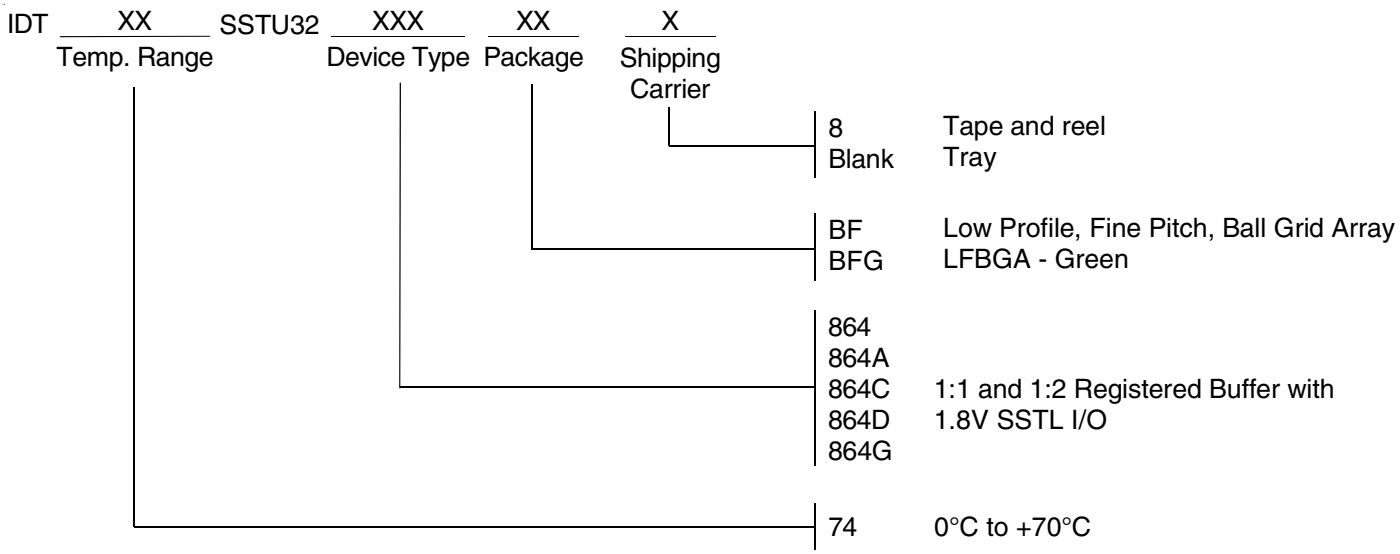
Load Circuit: Low-to-High Slew-Rate Adjustment



Voltage Waveforms: Low-to-High Slew-Rate Adjustment

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

ORDERING INFORMATION



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