Features

- **Fast Read Access Time – 55 ns**
- **Dual Voltage Range Operation**
    - **Low-voltage Power Supply Range, 3.0V to 3.6V or Standard 5V ±10% Supply Range**
- **Pin Compatible with JEDEC Standard AT27C256R**
- **Low-power CMOS Operation**
    - **20 µA Max (Less than 1 µA Typical) Standby for V_{CC} = 3.6V**
    - **29 mW Max Active at 5 MHz for V_{CC} = 3.6V**
- **JEDEC Standard Packages**
    - **32-lead PLCC**
    - **28-lead SOIC**
    - **28-lead TSOP**
- **High-reliability CMOS Technology**
    - **2,000V ESD Protection**
    - **200 mA Latchup Immunity**
- **Rapid Programming Algorithm – 100 µs/Byte (Typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
    - **JEDEC Standard for LVTTL**
- **Integrated Product Identification Code**
- **Industrial Temperature Range**
- **Green (Pb/Halide-free) Packaging Option**

256K (32K x 8) Low-voltage OTP EPROM

AT27LV256A

1. Description

The AT27LV256A is a high-performance, low-power, low-voltage 262,144-bit one-time programmable read-only memory (OTP EPROM) organized as 32K by 8 bits. It requires only one supply in the range of 3.0V to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3.3V supply. At V_{CC} = 3.0V, any byte can be accessed in less than 55 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3.3V, the AT27LV256A consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1 µA at 3.3V.

The AT27LV256A is available in industry-standard JEDEC-approved one-time programmable (OTP) plastic PLCC, SOIC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV256A operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV256A has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256A programs exactly the same way as a standard 5V AT27C256R and uses the same programming equipment.
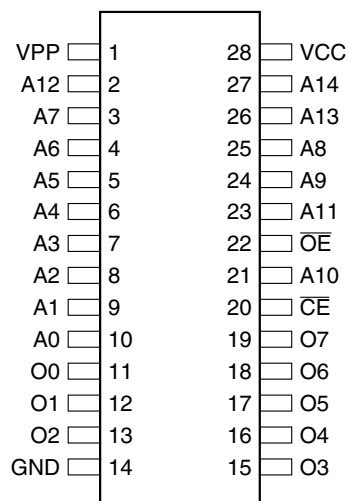
2. Pin Configurations

Pin Name	Function
A0 - A14	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

2.1 28-lead SOIC Top View

```
VPP  [ 1      28 ]  VCC
A12  [ 2      27 ]  A14
A7   [ 3      26 ]  A13
A6   [ 4      25 ]  A8
A5   [ 5      24 ]  A9
A4   [ 6      23 ]  A11
A3   [ 7      22 ]  OE
A2   [ 8      21 ]  A10
A1   [ 9      20 ]  CE
A0   [ 10     19 ]  O7
O0   [ 11     18 ]  O6
O1   [ 12     17 ]  O5
O2   [ 13     16 ]  O4
GND  [ 14     15 ]  O3
```

2.3 28-lead TSOP (Type 1) Top View

```
OE   [ 22     21 ]  A10
A11  [ 23     20 ]  CE
A9   [ 24     19 ]  O7
A8   [ 25     18 ]  O6
A13  [ 26     17 ]  O5
A14  [ 27     16 ]  O4
VCC  [ 28     15 ]  O3
VPP  [ 1      14 ]  GND
A12  [ 2      13 ]  O2
A7   [ 3      12 ]  O1
A6   [ 4      11 ]  O0
A5   [ 5      10 ]  A0
A4   [ 6       9 ]  A1
A3   [ 7       8 ]  A2
```

2.2 32-lead PLCC Top View

```
            A7  A12 VPP NC  VCC A14 A13
             4   3   2   1  32  31  30
A6   [ 5                         29 ] A8
A5   [ 6                         28 ] A9
A4   [ 7                         27 ] A11
A3   [ 8                         26 ] NC
A2   [ 9                         25 ] OE
A1   [ 10                        24 ] A10
A0   [ 11                        23 ] CE
NC   [ 12                        22 ] O7
O0   [ 13                        21 ] O6
             14  15  16  17  18  19  20
             O1  O2  GND NC  O3  O4  O5
```
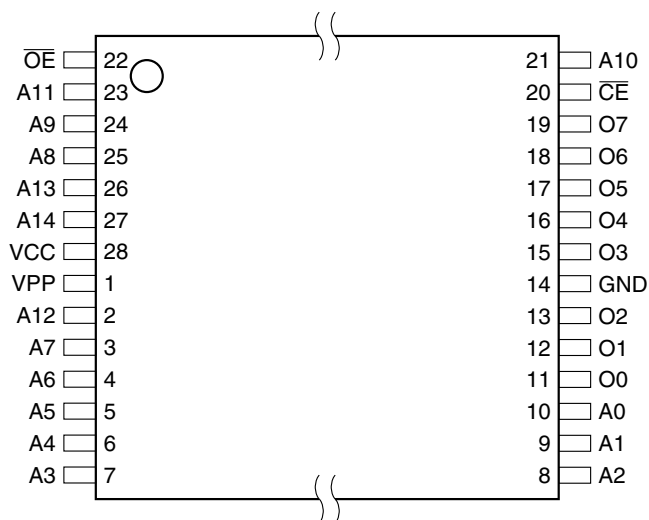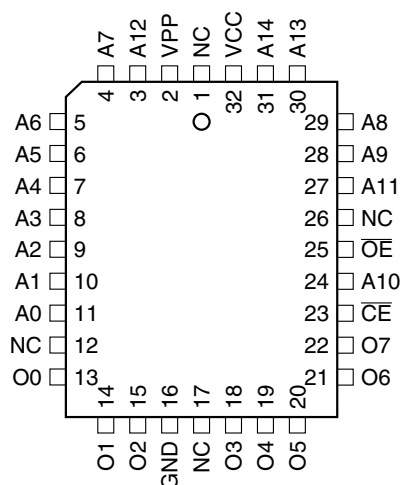
Note: 1. PLCC Package Pins 1 and 17 are Don't Connect.

3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram
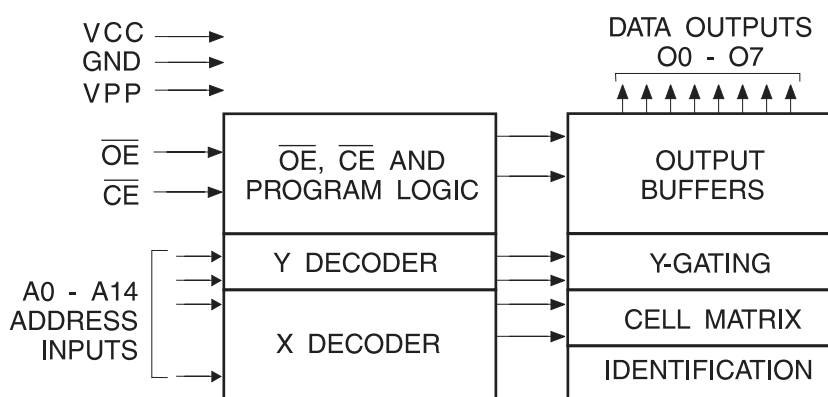
5. Absolute Maximum Ratings*

Temperature Under Bias.................................. -40°C to +85°C
Storage Temperature .... -65°C to +125°C
Voltage on Any Pin with Respect to Ground ....-2.0V to +7.0V[1]
Voltage on A9 with Respect to Ground ....-2.0V to +14.0V[1]
V_{PP} Supply Voltage with Respect to Ground ....-2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

6. Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read[2]	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable[2]	V_{IL}	V_{IH}	$X^{(1)}$	V_{CC}	V_{CC}	High Z
Standby[2]	V_{IH}	$X^{(1)}$	$X^{(1)}$	V_{CC}	V_{CC}	High Z
Rapid Program[3]	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify[3]	$X^{(1)}$	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify[3]	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit[3]	V_{IH}	V_{IH}	$X^{(1)}$	V_{PP}	V_{CC}	High Z
Product Identification[3][5]	V_{IL}	V_{IL}	A9 = V_H[4] A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.

2. Read, output disable, and standby modes require, 3.0V $\leq V_{CC} \leq$ 3.6V, or 4.5V $\leq V_{CC} \leq$ 5.5V.

3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.

4. V_H = 12.0 ± 0.5V.

5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

	AT27LV256A	
	-55	**-90**
Industrial Operating Temperature (Case)	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply	3.0V to 3.6V	3.0V to 3.6V
	5V ±10%	5V ±10%

8. DC and Operating Characteristics for Read Operation

| Symbol	Parameter	Condition	Min	Max	Units
V$_{CC}$ = 3.0V to 3.6V					
I$_{LI}$	Input Load Current	V$_{IN}$ = 0V to V$_{CC}$		±1	µA
I$_{LO}$	Output Leakage Current	V$_{OUT}$ = 0V to V$_{CC}$		±5	µA
I$_{PP1}$[2]	V$_{PP}$[1] Read/Standby Current	V$_{PP}$ = V$_{CC}$		10	µA
I$_{SB}$	V$_{CC}$[1] Standby Current	I$_{SB1}$ (CMOS), $\overline{CE}$ = V$_{CC}$ $_{\pm}$ 0.3V		20	µA
		I$_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to V$_{CC}$ + 0.5V		100	µA
I$_{CC}$	V$_{CC}$ Active Current	f = 5 MHz, I$_{OUT}$ = 0 mA, $\overline{CE}$ = V$_{IL}$		8	mA
V$_{IL}$	Input Low Voltage		-0.6	0.8	V
V$_{IH}$	Input High Voltage		2.0	V$_{CC}$ + 0.5	V
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 2.0 mA		0.4	V
V$_{OH}$	Output High Voltage	I$_{OH}$ = -2.0 mA	2.4		V
V$_{CC}$ = 4.5V to 5.5V					
I$_{LI}$	Input Load Current	V$_{IN}$ = 0V to V$_{CC}$		±1	µA
I$_{LO}$	Output Leakage Current	V$_{OUT}$ = 0V to V$_{CC}$		±5	µA
I$_{PP1}$[2]	V$_{PP}$[1] Read/Standby Current	V$_{PP}$ = V$_{CC}$		10	µA
I$_{SB}$	V$_{CC}$[1] Standby Current	I$_{SB1}$ (CMOS), $\overline{CE}$ = V$_{CC}$ $\pm$ 0.3V		100	µA
		I$_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to V$_{CC}$ + 0.5V		1	mA
I$_{CC}$	V$_{CC}$ Active Current	f = 5 MHz, I$_{OUT}$ = 0 mA, $\overline{CE}$ = V$_{IL}$		20	mA
V$_{IL}$	Input Low Voltage		-0.6	0.8	V
V$_{IH}$	Input High Voltage		2.0	V$_{CC}$ + 0.5	V
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 2.1 mA		0.4	V
V$_{OH}$	Output High Voltage	I$_{OH}$ = -400 µA	2.4		V

Notes: 1. V$_{CC}$ must be applied simultaneously with or before V$_{PP}$ and removed simultaneously with or after V$_{PP}$

2. V$_{PP}$ may be connected directly to V$_{CC}$, except during programming. The supply current would then be the sum of I$_{CC}$ and I$_{PP}$

9. AC Characteristics for Read Operation
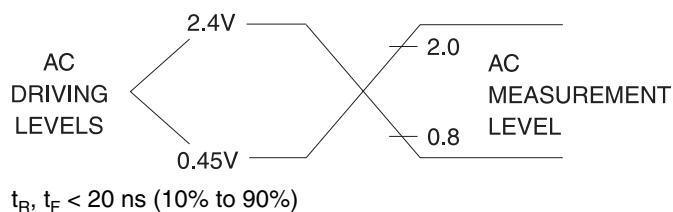
V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V

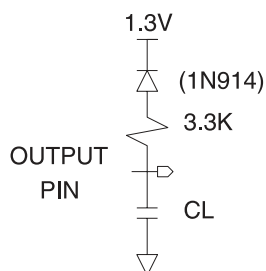| Symbol	Parameter	Condition	AT27LV256A				Units
			-55		-90		
			Max	Min	Min	Max	
t_{ACC}[3]	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		55		90	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		55		90	ns
t_{OE}[2][3]	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		35		50	ns
t_{DF}[4][5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First			30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First		0		0		ns

10. AC Waveforms for Read Operation[1]
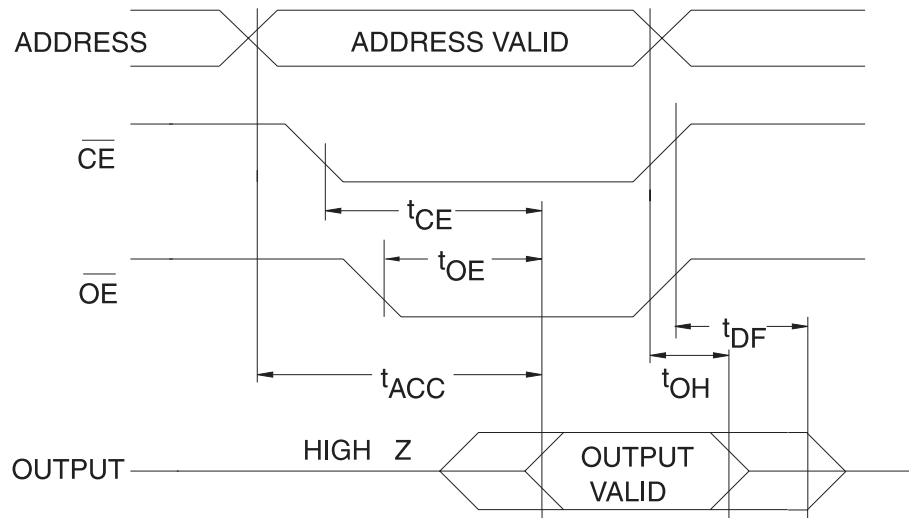
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

11. Input Test Waveforms and Measurement Levels

AC DRIVING LEVELS

2.4V

0.45V

2.0

0.8

AC MEASUREMENT LEVEL

t_R, t_F < 20 ns (10% to 90%)

12. Output Test Load

1.3V

(1N914)

3.3K

OUTPUT PIN

CL

Note: CL = 100 pF including jig capacitance.

13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms[1]

```
                                              READ
                              PROGRAM         (VERIFY)

              VIH
ADDRESS                          ADDRESS STABLE
              VIL
                    tAS                    tOE              tAH
              VIH
DATA                           DATA IN                DATA OUT
              VIL                                      VALID
                    tDS              tDH                    tDFP

              13.0V
VPP
              5.0V
                    tPRT        tVPS

              6.5V
VCC
              5.0V
                                tVCS
              VIH
CE
              VIL
                    tPW              tOES

              VIH
OE
              VIL
```
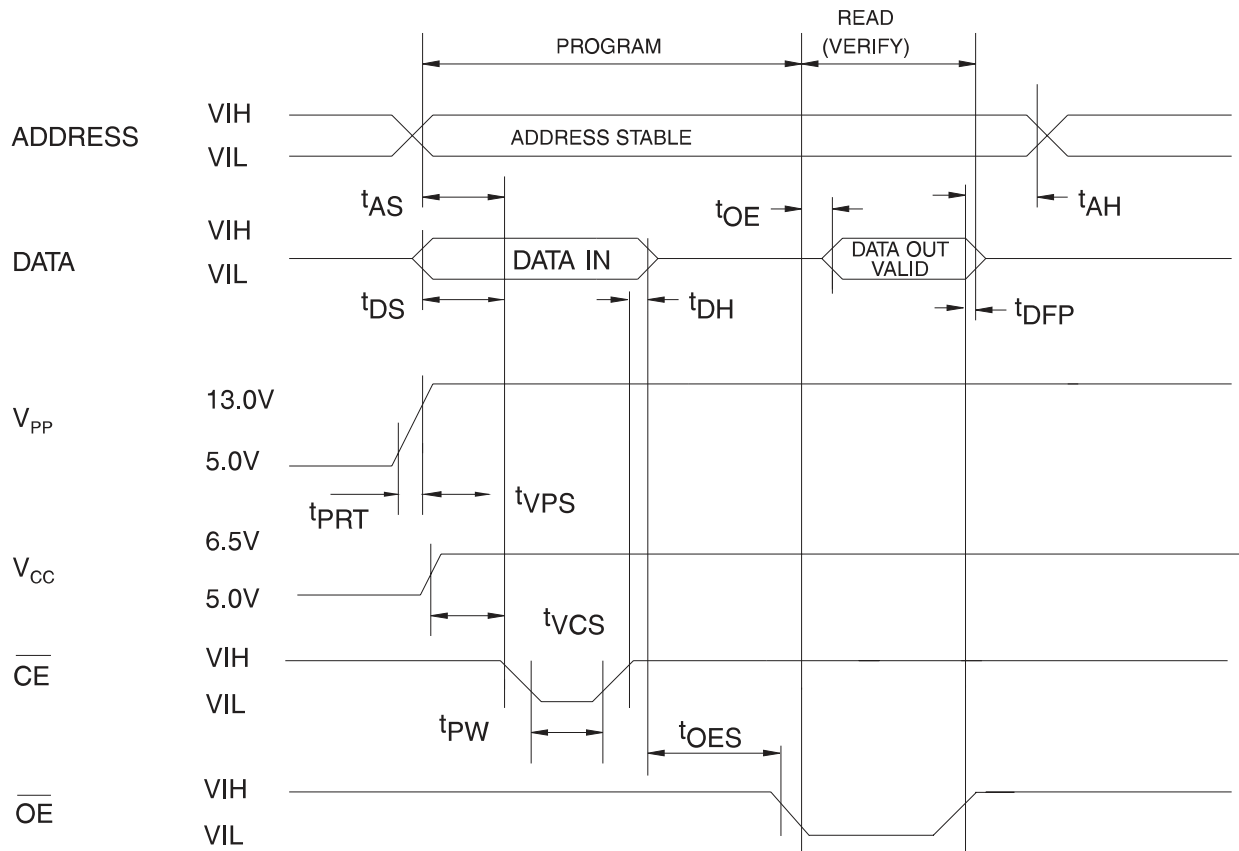
Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the AT27LV256A a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

AT27LV256A

15. DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		± 10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

Symbol	Parameter	Test Conditions[1]	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$[2]			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

3. Program Pulse width tolerance is 100 µsec $\pm 5\%$.

17. Atmel's AT27LV256A Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256A has the same Product Identification Code as the AT27C256R. Both are programming compatible.

18. Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.
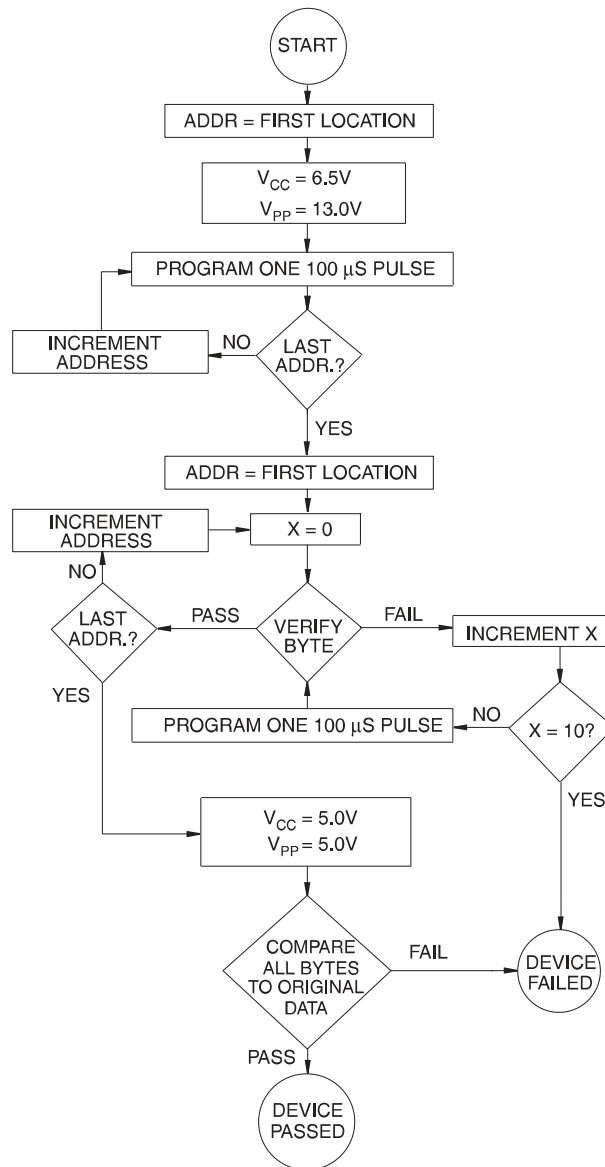
19. Ordering Information

19.1 Standard Package

t$_{ACC}$ (ns)	I$_{CC}$ (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	8	0.02	AT27LV256A-55JI AT27LV256A-55RI AT27LV256A-55TI	32J 28R[1] 28T	Industrial (-40° C to 85° C)
90	8	0.02	AT27LV256A-90JI AT27LV256A-90RI AT27LV256A-90TI	32J 28R[1] 28T	Industrial (-40° C to 85° C)

Note: ☐ Not recommended for new designs. Use Green package option.

19.2 Green Package Option (Pb/Halide-free)

t$_{ACC}$ (ns)	I$_{CC}$ (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	8	0.02	AT27LV256A-55JU AT27LV256A-55RU AT27LV256A-55TU	32J 28R[1] 28T	Industrial (-40° C to 85° C)
90	8	0.02	AT27LV256A-90JU AT27LV256A-90RU AT27LV256A-90TU	32J 28R[1] 28T	Industrial (-40° C to 85° C)

Note: 1. The 28-pin SOIC package is not recommended for new designs.

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28R	28-lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Thin Small Outline Package (TSOP)

20. Packaging Information

20.1   32J – PLCC

1.14(0.045) X 45°

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45°

0.318(0.0125)
0.191(0.0075)

E1   E

B

e

B1   E2

D1

D

A2

A1

A

0.51(0.020)MAX
45° MAX (3X)

D2
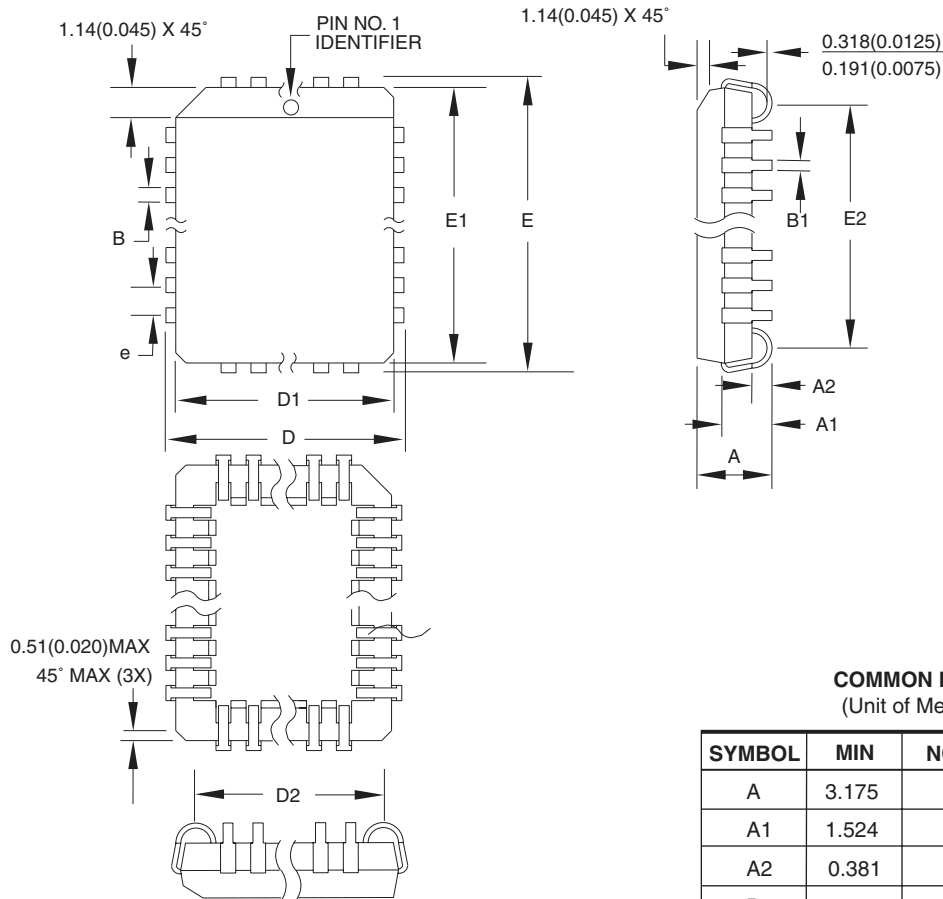
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes: 1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	2325 Orchard Parkway San Jose, CA 95131	**TITLE** **32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	**DRAWING NO.** 32J	**REV.** B

20.2 28R – SOIC
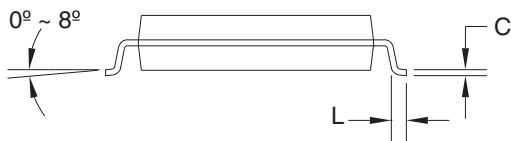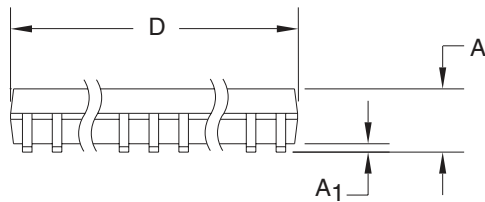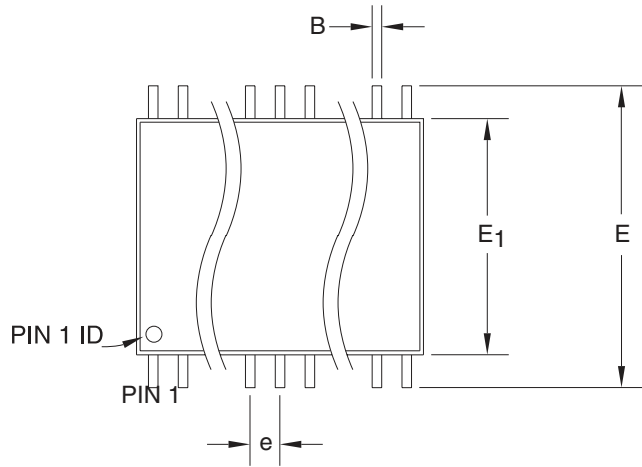
Note: 1. Dimensions D and E1 do not include mold Flash
or protrusion. Mold Flash or protrusion shall not exceed
0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.39	–	2.79	
A1	0.050	–	0.356	
D	18.00	–	18.50	Note 1
E	11.70	–	12.50	
E1	8.59	–	8.79	Note 1
B	0.356	–	0.508	
C	0.203	–	0.305	
L	0.94	–	1.27	
e	1.27 TYP			

5/18/2004

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**28R,** 28-lead, 0.330" Body Width, Plastic Gull Wing Small Outline (SOIC)	28R	C

20.3   28T – TSOP

PIN 1

Pin 1 Identifier Area

D1   D

e   b

E   A2   A

A1

0° ~ 5°

c

L

L1

SEATING PLANE   GAGE PLANE
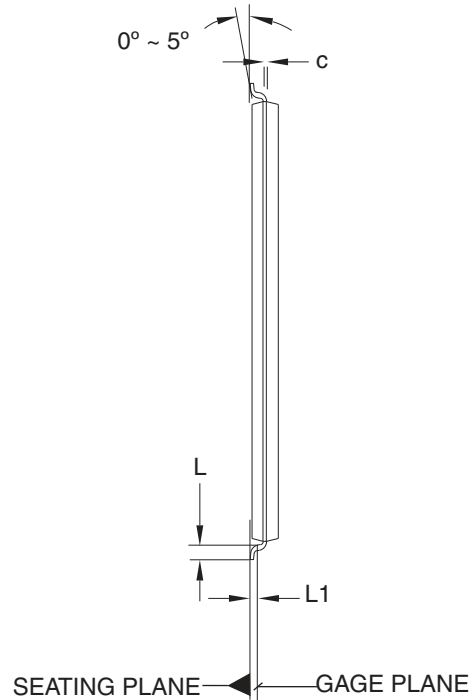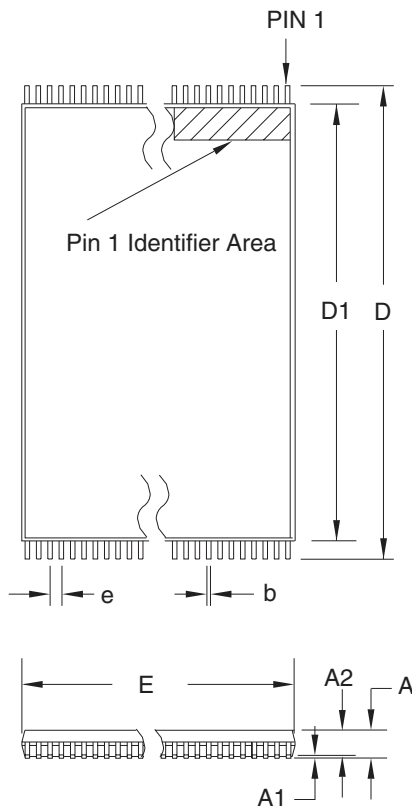
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes: 1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable
protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

	2325 Orchard Parkway San Jose, CA 95131	**TITLE** **28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	**DRAWING NO.** 28T	**REV.** C

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