DATA SHEET

74F258A

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

FEATURES

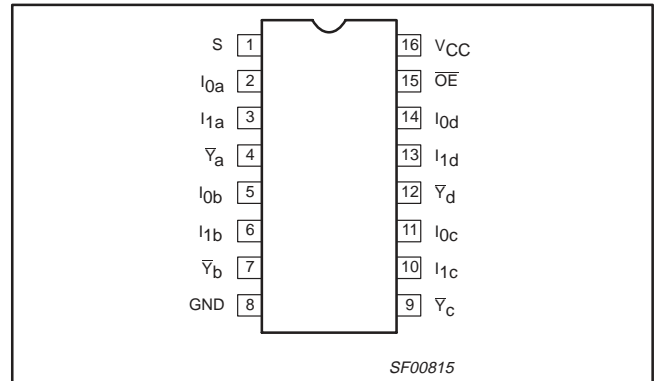- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F257A for non-inverting version

DESCRIPTION

The 74F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form.

The 74F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

PIN CONFIGURATION

Pin	Name		Pin	Name
1	S		16	V_{CC}
2	I_{0a}		15	$\overline{OE}$
3	I_{1a}		14	I_{0d}
4	$\overline{Y}_a$		13	I_{1d}
5	I_{0b}		12	$\overline{Y}_d$
6	I_{1b}		11	I_{0c}
7	$\overline{Y}_b$		10	I_{1c}
8	GND		9	$\overline{Y}_c$

SF00815

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
16-pin plastic DIP	N74F258AN	SOT38-4
16-pin plastic SO	N74F258AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

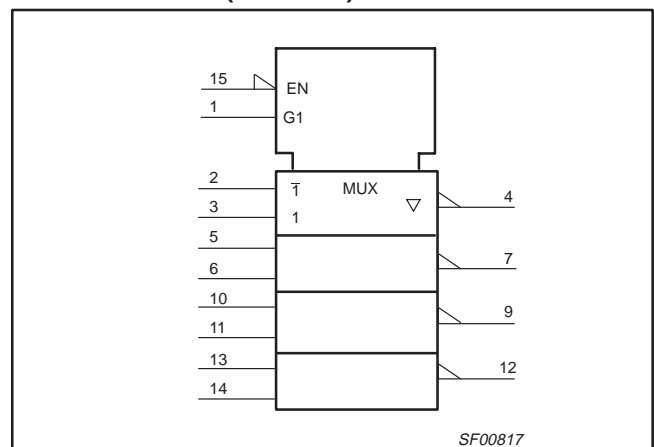| PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
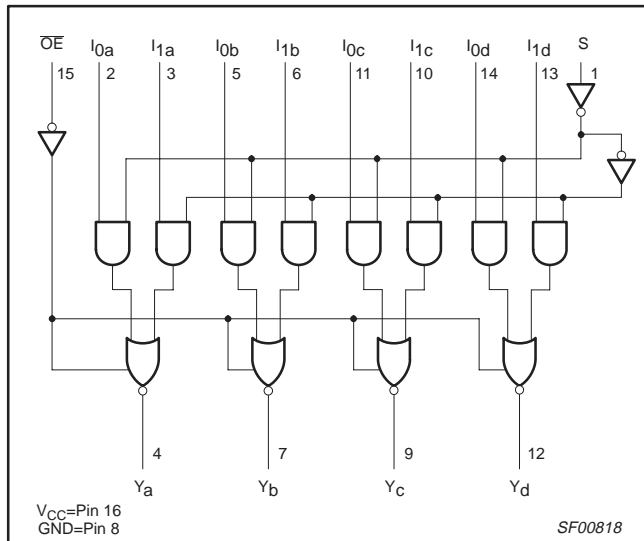
LOGIC SYMBOL

V_{CC}=Pin 16
GND=Pin 8

SF00816
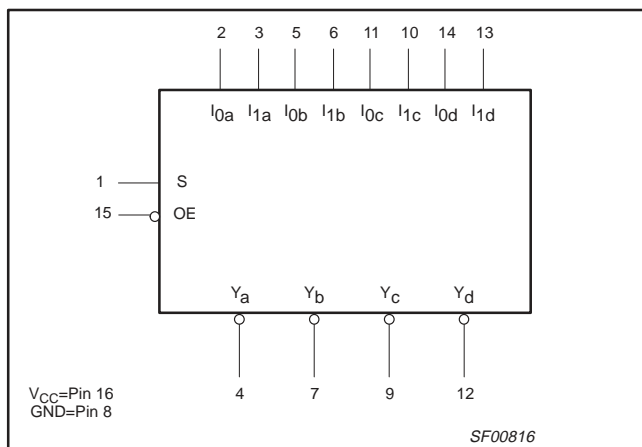
LOGIC SYMBOL (IEEE/IEC)

SF00817

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

LOGIC DIAGRAM

V_CC=Pin 16
GND=Pin 8

SF00818

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	$\pm10\%V_{CC}$	2.4			V
		V_{IH} = MIN, I_{OL} = MAX	$\pm5\%V_{CC}$	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	$\pm10\%V_{CC}$		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	$\pm5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	μA
I_{OZL}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 0.5V				−50	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)	I_{CCH}	I_{1n}=4.5V, $\overline{OE}$=I_{0n}=S=GND		8.5	11.5	mA
		I_{CCL} V_{CC} = MAX	I_{1n}=S=4.5V, $\overline{OE}$=I_{0n}=GND		17	23	mA
		I_{CCZ}	I_{1n}=$\overline{OE}$=4.5V,I_{0n}=S=GND		16	22	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = −55°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns ns

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)
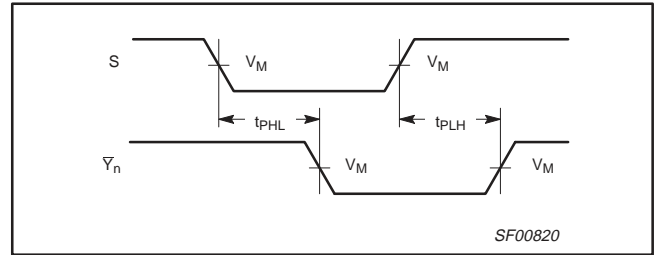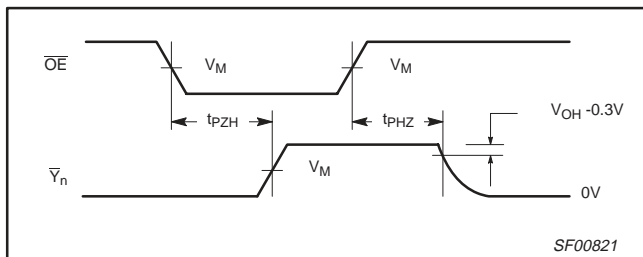
74F258A

AC WAVEFORMS
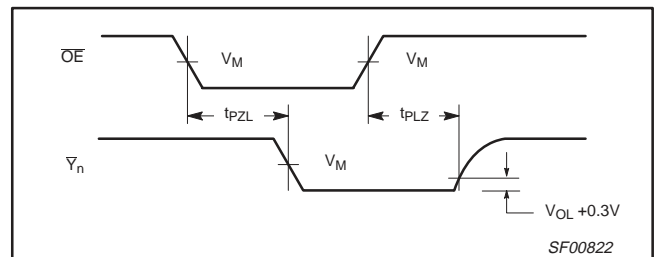
For all waveforms, V_M = 1.5V.
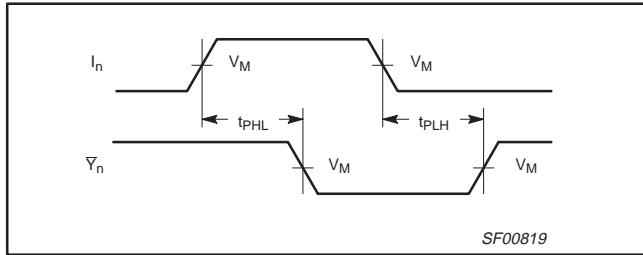
**Waveform 1. Propagation Delay
Data and Select to Output**

SF00819

**Waveform 2. Propagation Delay
Select to Output**

SF00820

**Waveform 3. 3-State Output Enable Time to High Level and
Output Disable Time from High Level**

SF00821

**Waveform 4. 3-State Output Enable Time to Low Level and
Output Disable Time from Low Level**

SF00822

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

Input Pulse Definition

SF00777

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;
   see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance;
   see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of
   pulse generators.

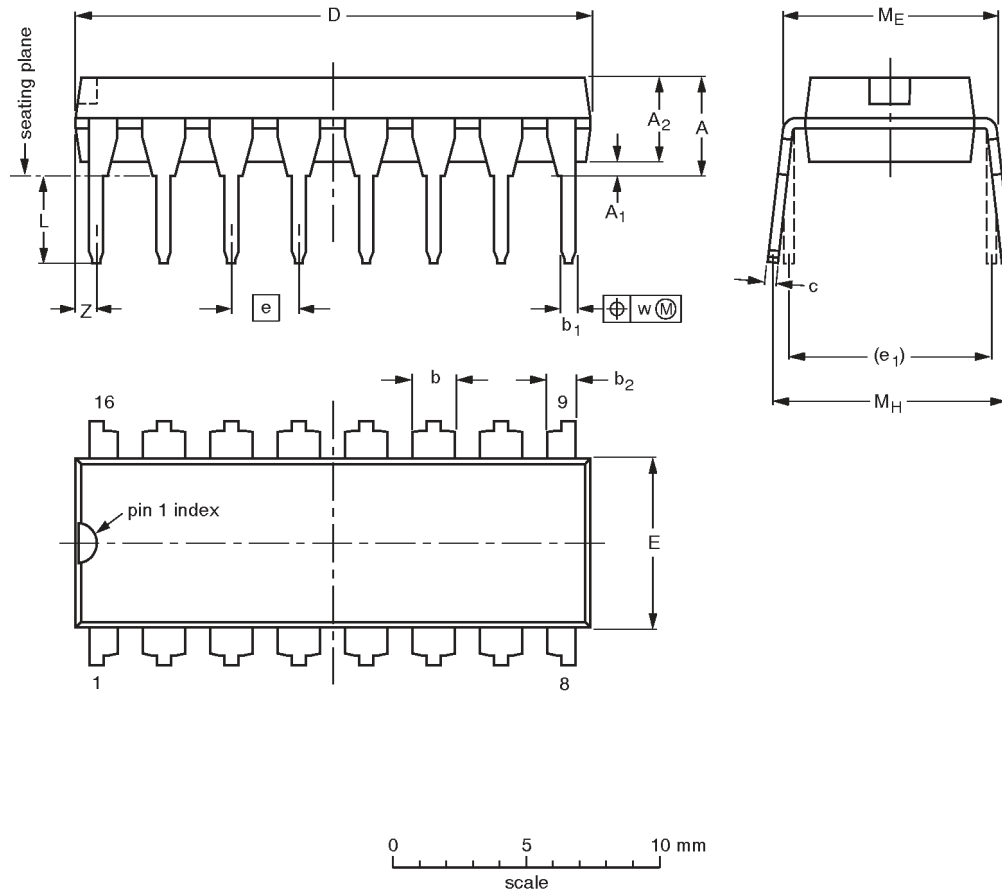| family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

DIP16:   plastic dual in-line package; 16 leads (300 mil)   **SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	b$_2$	c	D$^{(1)}$	E$^{(1)}$	e	e$_1$	L	M$_E$	M$_H$	w	Z$^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)   74F258A

SO16:   plastic small outline package; 16 leads; body width 3.9 mm   SOT109-1


```
0        2.5        5 mm
|__|__|__|__|__|__|__|__|
           scale
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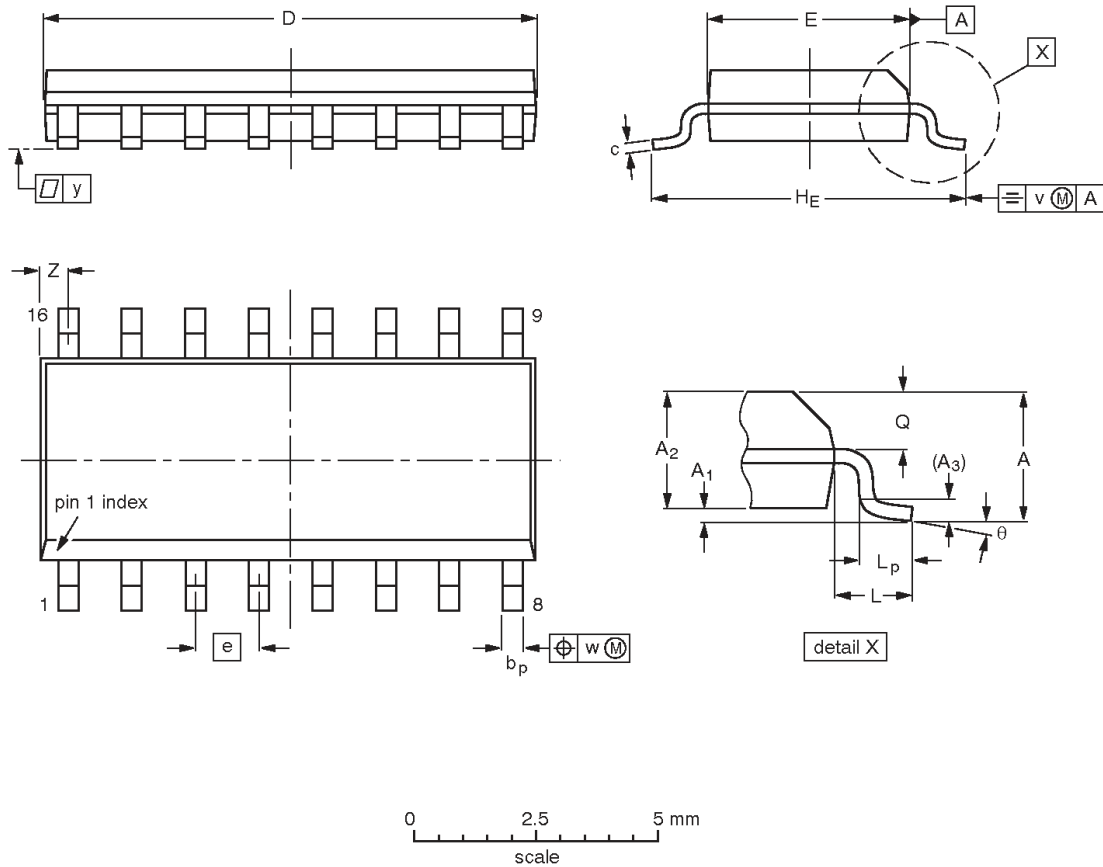
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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