Active ORing Controller IC with Load Disconnect Feature

Description

The PI2002 *Cool-ORing*™ solution is a high-speed Active ORing controller IC with a load disconnect feature designed for use with back-to-back N-channel MOSFETs in redundant power system architectures. The PI2002 *Cool-ORing* controller enables an extremely low power loss solution with fast dynamic response to fault conditions, critical for high availability systems. The PI2002 controls back-to-back MOSFETs providing true bi-directional switch capabilities to protect against both power source and load fault conditions.

The gate drive output turns the MOSFETs on in normal steady state operation, while achieving high-speed turn-off during input power source fault conditions, that cause reverse current flow, with auto-reset once the fault clears. The PI2002 has the added benefit of being able to protect against output load fault conditions that may induce excessive forward current and device over-temperature by removing gate drive from the back-to-back MOSFETs with an auto-retry programmable off-time. The back-to-back MOSFETs drain-to-drain voltage is monitored to detect normal forward, excessive forward, light load and reverse current flow. The PI2002 provides an active low fault flag output to the system during fault condition. A temperature sensing function turns off the MOSFETs and indicates a fault if the junction temperature exceeds 145°C.

Features

- Power Source & Load Fault Protection
- Fast Dynamic Response, with 120ns reverse & 150ns forward over-current turn-off delay time
- 4A gate discharge current
- Accurate back-to-back MOSFETs drain-to-drain voltage sensing to indicate system level fault conditions
- Programmable under & over-voltage detection
- Over temperature fault detection
- Programmable over-current Gate off time
- Programmable short circuit load detection function
- Active low fault flag output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- Active ORing with Load Disconnect
- High current Active ORing

Package Options

The PI2002 is offered in the following packages:

- 3mm x 3mm 10 Lead TDFN package
- 8 Lead SOIC

Typical Applications:

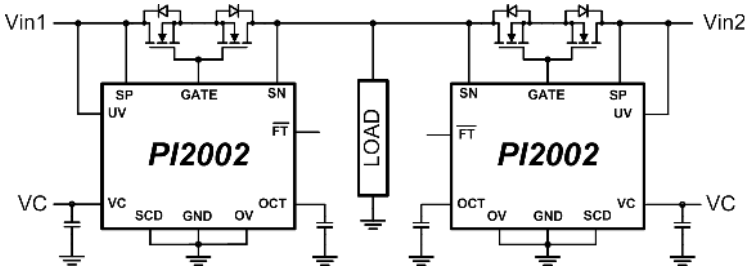


Figure 1a: PI2002 High Side ORing with load disconnect

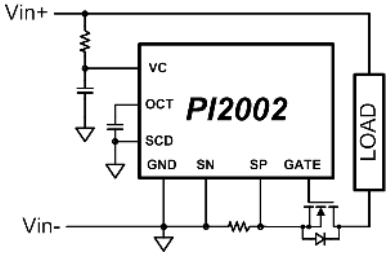
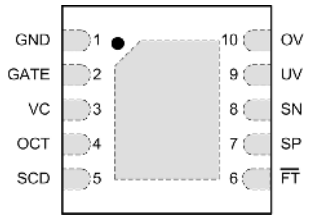


Figure 1b: PI2002 Low Side Disconnect Switch

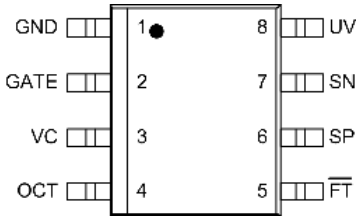
Pin Description

Pin Name	Pin Number		Description
	10-Pin DFN	SO-8	
GND	1	1	**Ground:** This pin is ground for the gate driver and control circuitry.
GATE	2	2	**Gate Drive Output:** This pin drives the gates of the external Back-to-Back N-channel MOSFETs. Under normal operating conditions, the GATE pin pulls high to 10V (typ) with respect to the SN pin. The controller turns the gate off during all fault conditions except the Low Forward Current condition.
VC	3	3	**Controller Input Supply:** This pin is the supply pin for the control circuitry and gate driver. Connect a 1µF capacitor between VC pin and the GND pin. Voltage on this pin is limited to 15.5V by an internal shunt regulator. For high voltage auxiliary supply applications connect a shunt resistor between VC and the auxiliary supply.
OCT	4	4	**Over-Current Timer Input:** Connecting a capacitor (≤ 20nF) sets the gate off time once an over-current condition is detected. No capacitor on this pin will result in minimum off time, 40µs. Pulling this input low will disable Gate drive.
SCD	5	n/a	**Short Circuit Detect Input:** This input pin is for setting the load voltage where a short circuit level is defined and detected. To enable slow MOSFET turn-on mode, connect SCD to VC. Connect to load point for minimum threshold (0.335V) or use resistor divider to increase threshold. Grounding pin enables the fast MOSFET turn on mode. This pin is not available in the SO-8 package and the controller is set for low Gate source current, 300µA.
$\overline{FT}$	6	5	**Fault State Output:** This open collector output pulls low 40µs after a fault condition occurs. Fault logic inputs are VC Under-Voltage, input Under-Voltage, input Over-Voltage, Forward Over-Current, Reverse Current, Low Forward Current (or shorted switches) and Over-Temperature. Leave this pin open if unused.
SP	7	6	**Positive Sense Input & Clamp:** Connect SP pin to the input power source side of the MOSFETs. The polarity and magnitude of the voltage difference between SP and SN provides an indication of current flow through the MOSFETs.
SN	8	7	**Negative Sense Input & Clamp:** Connect SN to the output load side of the MOSFET. The polarity and magnitude of the voltage difference between SP and SN provides an indication of current flow through the MOSFETs.
UV	9	8	**Input Under-Voltage Input:** The UV pin is used detects when the input is less than the Under-Voltage threshold resulting in a low Fault pin. The input voltage UV threshold is programmable through an external resistor divider. During an Under-Voltage fault, the Gate is pulled low. Connect UV to VC to disable this function.
OV	10	n/a	**Input Over-Voltage Input:** The OV pin detects when the input is greater than the Over-Voltage threshold resulting in a low Fault pin. OV "AND" a Forward Current condition turns the MOSFETs off. The input voltage OV threshold is programmable through an external resistor divider. Connect OV to GND to disable this function. This pin is not available in the SO-8 package and OV function is disabled.

Package Pin-Outs



10 Lead TDFN (3mm x 3mm)
Top view



8 Lead SOIC (5mm x 6mm)
Top view

Absolute Maximum Ratings

VC	-0.3V to 17.3V / 40mA
SP, SN, OV, OCT	-0.3V to 8.0V / 10mA
UV, SCD, $\overline{FT}$	-0.3V to 17.3V / 10mA
GATE	-0.3V to 17.3V / 5A
GND	-0.3V / 5A peak
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to Thermal shutdown
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF, C_{GATE} = 4nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range[3]	V_{VC-GND}	4.5		13.2	V	No VC Limiting Resistors
Quiescent Current	I_{VC}		3.7	4.2	mA	Normal Operating Conditions No Faults
Clamp Voltage	V_{VC-CLM}	15	15.5	16	V	I_{VC}=10mA
VC Clamp Shunt Resistance	R_{VC}			7.5	Ω	Delta I_{VC}=10mA
VC Under-Voltage Rising Threshold	V_{VCUVR}		4.3	4.5	V	
VC Under-Voltage Falling Threshold	V_{VCUVF}	4.0	4.15		V	
VC Under-Voltage Hysteresis	V_{VCUVHS}		150		mV	
FAULT						
Under-Voltage Rising Threshold	V_{UVR}		500	540	mV	
Under-Voltage Falling Threshold	V_{UVF}	440	475		mV	
Under-Voltage Threshold Hysteresis	V_{UVHS}		25		mV	
Under-Voltage Bias Current	I_{UV}	-1		1	µA	
Over-Voltage Rising Threshold	V_{OVR}		500	540	mV	
Over-Voltage Falling Threshold	V_{OVF}	440	475		mV	
Over-Voltage Threshold Hysteresis	V_{OV-HS}		25		mV	
Over-Voltage Bias Current	I_{OV}	-1		1	µA	
Fault Output Low Voltage	V_{FTL}		200	500	mV	I_{FT}=2mA, VC>4.5V
Fault Output High Leakage Current	I_{FT-LC}			10	µA	V_{FT}=14V
Fault Delay Time	t_{FT-DEL}	20	40	60	µs	Includes output glitch filter
Over Temperature Fault[1]	T_{FT}		145		°C	
Over Temperature Fault Hysteresis[1]	T_{FT-HS}		-10		°C	

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF, C_{GATE} = 4nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
GATE DRIVER						
Gate Source Current	I_{G-SC}		-1.5		mA	V_G = 1V, Normal Operating Conditions, No Faults V_{SCD}=0V
Gate Source Current	I_{G-SC}		-0.30		mA	V_G = 1V, Normal Operating Conditions, No Faults V_{SCD}=Vc
Pull Down Peak Current(1)	I_{G-PD}	1.5	4.0		A	
Gate Pull-down Resistance (1)	R_{G-PD}		0.3		Ω	V_G = 1.5V @ 25°C
AC Gate Pull-down Voltage (1)	V_{G-PD}			0.2	V	$T_{RVS-DLY}$ + 50nsec
DC Gate Pull-down Voltage to GND	V_{G-PD}		0.8	1.2	V	I_G=100mA, in reverse fault
Gate Voltage @ VC UVLO	V_{G-UVLO}		0.7	1	V	I_G =10µA, 1.5<VC< V_{VCUVLO}
Gate Fault Condition Clear(1)	V_{G-CL}		45		%	
Gate to SN Clamp Voltage	V_{G-SN}	9	10	11	V	I_G = 100µA
Gate Voltage High	V_G	VC-0.5V	VC-0.25V		V	VC- V_{SN} < V_{G-CLMP}
Gate Fall Time	t_{G-F}		10	15	ns	90% to 10% of V_G max.
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-0.1		5.5	V	V_{CM} =SP & SN w/respect to GND
VC to SN differential(1)	V_{VC-SP}	3.5			V	
Differential Operating Input Voltage	V_{SP-SN}	-50		125	mV	SP-SN
SP Input Bias Current	I_{SP}		3.5		µA	V_{CM} =1.25V
SN Input Bias Current	I_{SN}		-37		µA	V_{CM} =1.25V
SN (SP) Voltage	$V_{SN(SP)}$			5.5	V	SP=0V (SN=0V)
Reverse Comparator Off Threshold	V_{RVS-TH}	-10	-6	-2	mV	V_{CM} =3.3V
Reverse Comparator Hysteresis	V_{RVS-HS}	2	3	5	mV	V_{CM} =3.3V
Reverse Fault to Gate Turn-off Delay Time	$T_{RVS-DLY}$		120	150	ns	
Forward Comparator On Threshold	V_{FWD-TH}	2	5	9	mV	V_{CM} =3.3V
Forward Comparator Hysteresis	V_{FWD-HS}	-5	-3	-2	mV	V_{CM} =3.3V
Forward Over-Current Comparator Threshold	V_{FOC-TH}	104	112	120	mV	V_{CM} =3.3V
Forward Over-Current Comparator Hysteresis	V_{FOC-HS}	-8	-6	-4	mV	V_{CM} =3.3V
Forward Over-Current to Gate Turn-off Delay	$t_{FOC-DLY}$		150	180	ns	

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF, C_{GATE} = 4nF

OCT						
OCT Source Current	I_{OCTSC}		-10		µA	V_{OCT} = 1.25V
OCT Clamp Voltage	V_{OCT-CL}	2.2	3.2	4.2	V	No Fault
OCT Threshold Voltage High	V_{OCT-Hi}		1.75		V	SP=3.3V, SN=0V
OCT Threshold Voltage Low	V_{OCT-Lo}		0.875		V	SP=3.3V, SN=0V
OCT OFF	$T_{OCT-OFF}$		350		µs	FOC fault condition
OCT Gate Drive Disable	V_{OCT-Lo}			500	mV	I_{OCT} = -100uA
OCT Sink Current	I_{OCTSK}	5	10		mA	V_{OCT} =2.25V SP-SN=125mV
SCD						
SCD Bias Current	Iscd	-1		1	µA	V_{SCD}=0V
SCD Threshold Voltage High	V_{ThSCDR}	300	340	380	mV	V_{SP-SN}=20mV, V_G=1V
;SCD Threshold Voltage Low	V_{ThSCDF}		310		mV	
SCD Hysteresis	V_{ThSCDR} - V_{ThSCDF}	25	50	75	mV	V_{SP-SN}=20mV, V_G=1V

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Refer to the *Auxiliary Power Supply* section in the *Application Information* section for details on the VC requirement to meet the MOSFET Vgs requirement.

Functional Description:

The PI2002 controller IC product is designed to drive back-to-back N-channel MOSFETs in Active ORing applications that also require a load disconnect feature. The PI2002 used with external back-to-back MOSFETs can function as an ideal ORing diode in the high-side of a redundant power system coupled with a load disconnect switch, significantly reducing power dissipation and eliminating the need for heatsinking.

The PI2002 provides the ability to block current in both directions by driving two MOSFETs in a back-to-back configuration as shown in Figure 1a. This configuration offers the ability to protect the load and the MOSFET, by pulling the gate low, during Reverse Current, Forward Over-Current, Under-Voltage, Over-Voltage and Over-Temperature faults. The fault flag is also issued during these fault conditions.

Differential Amplifier:

The PI2002 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to three comparators: Reverse comparator, Forward comparator, and Forward over-current comparator.

Reverse Current Comparator: RVS

The reverse current comparator provides the most critical function in the controller, detecting negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will enable the gate discharge circuit and turn off the MOSFETs in typically 120ns.

The reverse comparator has typically 3mV of hysteresis referenced to SP-SN.

Forward Current Comparator: FWD

The FWD comparator detects when a forward current condition exists and SP is 5mV (typical) positive with respect to SN. When SP-SN is less than 5mV it will indicate a fault condition on the $\overline{FT}$ pin during a light load while maintaining gate drive to the MOSFETs. The PI2002 will initiate a gate shutdown if the Forward "AND" the over-voltage (OV) condition are true.

Forward Over-Current Comparator: FOC

The FOC comparator indicates an excessive forward current condition when SP is 112mV higher than SN. The PI2002 controller will initiate a fault condition when the GATE output voltage is more than 45% of the regulated gate to SN voltage and SP-SN is higher than 112mV, the MOSFETs will turn off then retry after a controlled off-time determined by the capacitor value on the OCT input pins.

Over-Current Timer: OCT

OCT off-time is set by the OCT a capacitor as shown in Figure 3.

The OCT block will control the off-time of the MOSFETs after a FOC fault condition has occurred. The equivalent block diagram is shown in Figure 2. As the Set input at the OCT timer goes high, $\overline{Out}$ will go low, pulling the GATE pin low. At the same time a one shot of 40µs discharges the OCT capacitor, then releases it charging the capacitor again. $\overline{Out}$ and GATE pins stay low until the OCT pin reaches the OCT high threshold (V_{OCT-Hi}), then $\overline{Out}$ goes high and the GATE pin sources current to charge the MOSFET gates. As soon as the GATE voltage reaches 45% of the GATE to SN clamp voltage, or 45% of {VC-V(SN) -0.25V}, the Clamp Detector asserts a low signal again at the NOR gate. If $\overline{FOC}$ is still low then the GATE pin will be pulled low and will start a new off-time cycle of the Over-Current timer.

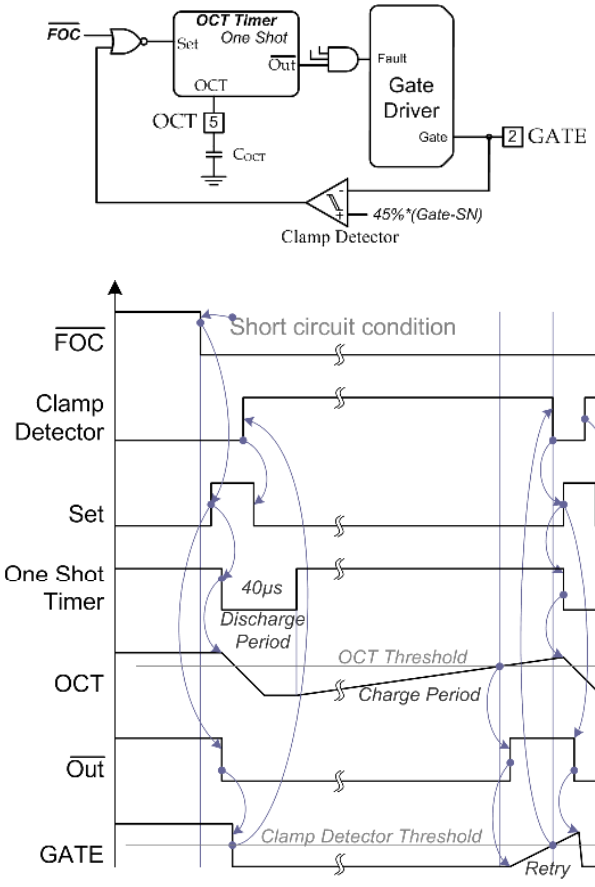


Figure 2: OCT block and timing diagram

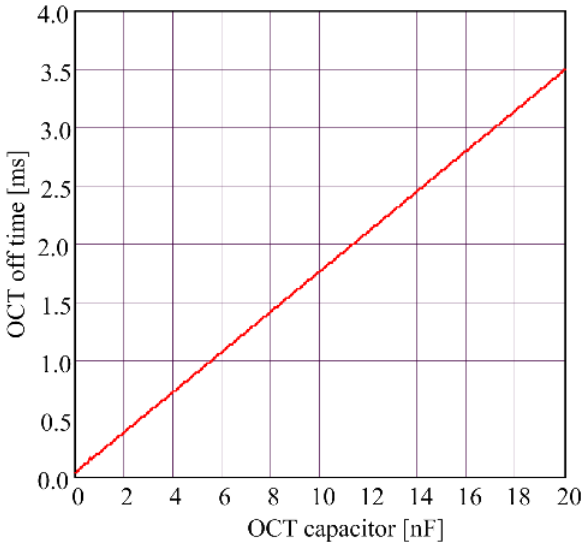


Figure 3: *OCT Off time vs. OCT capacitor value*

Short Circuit Detect: SCD

This comparator block input (for 10L-TDFN package only) can be connected to the load directly or programmed to a higher voltage with a resistor divider. The SCD function allows the user to define the (Hard Short) voltage level expected if a non-ideal short circuit occurs at the load. To prevent damage of the MOSFETs under this condition (V_{SCD}<335mV) the gate charge current (I_{G-SC}) is increased by a factor of approximately 5 times resulting in fast charging of the MOSFET gates. This feature enables the capability to distinguish between a faulted load versus powering capacitive and low resistive loads without entering the OCT mode. This pin can be grounded to provide a fast gate charging or pulled to VC for lower gate current to drive highly capacitive loads with resulting slow gate charge under the fault condition. If the resulting temperature rise of the MOSFETs is thermally coupled to the controller, invoking a thermal shutdown, the thermal time constant of the system will determine the average duty cycle further protecting the MOSFETs.

The SCD pin is not available in the SO-8 package version and is internally preset for slow gate charge, where the Gate source current is 300µA.

VC and Internal Voltage Regulator:

The PI2002 has a separate input (VC) that provides power to the control circuitry and the gate driver. An internal regulator clamps the VC voltage to 15.5V.

For high side applications, the VC input should be high enough above the bus voltage to properly enhance the external N-channel MOSFETs.

The internal regulator circuit has a comparator to monitor VC voltage and initiates a FAULT condition when VC is lower than the VC Under-Voltage Threshold.

UV:

The Under-Voltage (UV) input trip point can be programmed through an external resistive divider to monitor the input voltage. The UV comparator initiates a gate low condition turning the MOSFETs off and initiates a fault condition pulling the $\overline{FT}$ pin low, when UV falls below the Under-Voltage Falling Threshold.

OV:

The Overvoltage (OV) input trip point (for 10L-TDFN package only) can be programmed through an external resistive divider to monitor the input voltage. The OV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low when OV rises above the Overvoltage Rising Threshold. The PI2002 will turn the Gate output off if the OV and the Forward Current conditions are both true. The low resistance redundant paths of an Active ORing system tend to force all the input sources to the same voltage making it difficult to identify the noncompliant source. By ANDing OV with the Forward Current Threshold the noncompliant source is identified and disconnected from the system.

The OV pin is not available in the SO-8 package version and is disabled.

Over-Temperature Detection:

The internal Over-Temperature block monitors the junction temperature of the controller. The Over-Temperature threshold is set to 145°C with -10°C of hysteresis. When the controller temperature exceeds this threshold, the Over-Temperature circuit pulls GATE pin low and initiates a fault condition and pulls the $\overline{FT}$ pin low. By maintaining proper thermal matching between the controller and the power MOSFETs, this function can be used to protect the MOSFETs from thermal runaway conditions.

Gate Driver:

The gate driver (GATE) output is configured to drive external N-channel MOSFETs. In the high state, the gate driver applies a current source that is dependent on the SCD pin voltage. The controller regulates the gate voltage to 10V above the SN pin when the VC voltage is 10.5V higher than the SN pin. Otherwise the gate voltage (V_G) to V_{SN} will be {V_{G-SN} = VC - V_{SN} – 0.5V}. Note that VC is the controller internal regulated voltage.

When a reverse current fault is initiated, the gate driver pulls the GATE pin low and discharges the FET gate with 4A peak capability.

When the input source voltage is applied and before the MOSFET is fully enhanced, a voltage greater than the Forward Over-Current (FOC) Threshold may be present across the MOSFET. To avoid an erroneous FOC detection, a VGS detector blanks the FOC and FWD comparators from initiating a fault, until the GATE pin reaches 45% of $V_{G\text{-}CLMP}$. If VC is too low to establish the Gate Clamp condition the reference for detection is 45% of {VC-V(SN) - 0.25V}.

The GATE pin pulls low under the following fault conditions:

- Reverse Current
- Forward Over-Current "AND" clamp detector is cleared
- Over Temperature
- Input Under-Voltage
- Input Over-Voltage "AND" nominal Forward Current
- VC pin Under-Voltage

Fault:

The fault circuit output is an open collector with 40µs delay to prevent any false triggering. The $\overline{FT}$ pin will be pulled low when any of the following faults occurs:

- Reverse Current
- Forward Over-Current "AND" clamp detector is cleared
- Forward Low Current "AND" clamp detector is cleared
- Over Temperature
- Input Under-Voltage
- Input Over-Voltage "AND" nominal Forward Current
- VC pin Under-Voltage

The Forward Current fault condition occurs when the MOSFETs gates are high but are not conducting a significant level of forward current or may indicate the MOSFETs are shorted either internally or externally ($V_{D1\text{-}D2}$ < 6mV).

The VGS detector prevents FOC or FWD from initiating a fault when the MOSFET gate is low. The gate to SN voltage has to reach sufficient voltage to establish the Rds(on) condition before these faults are detected.

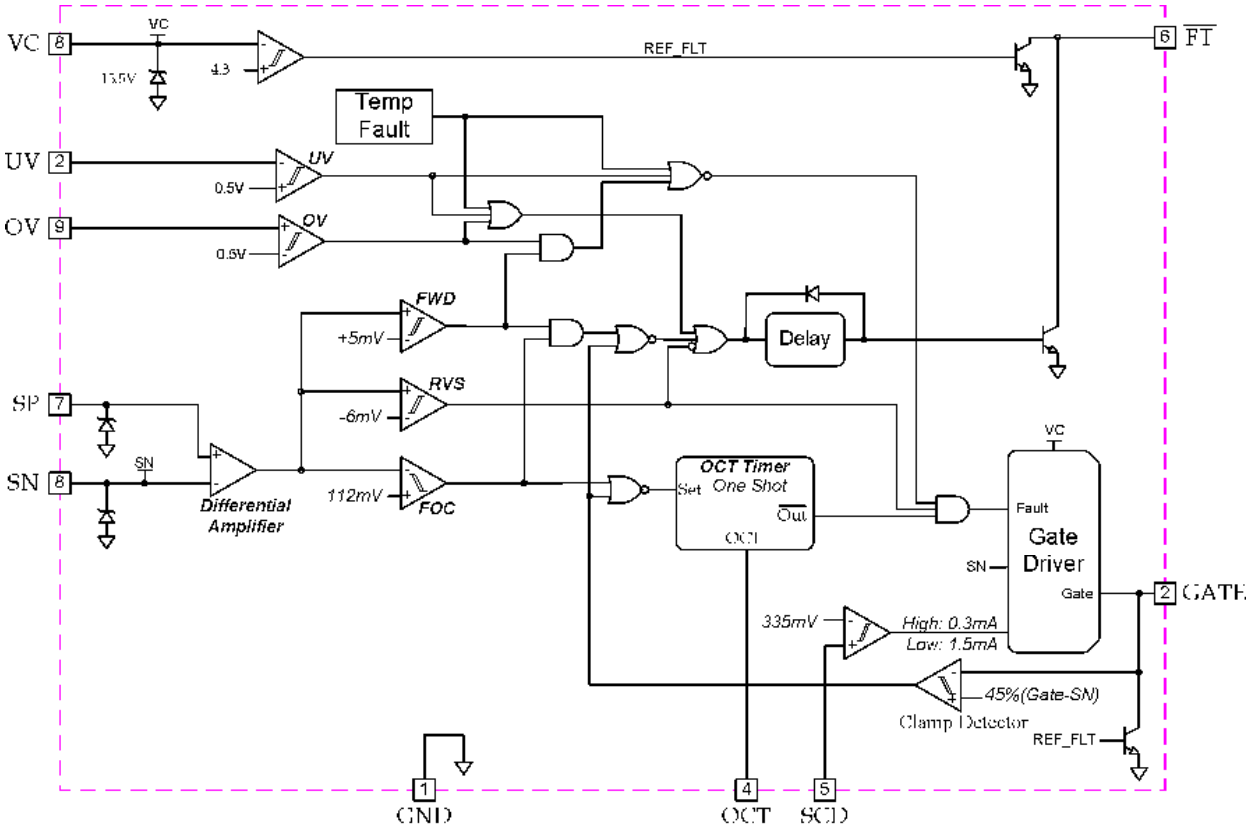


Figure 4: PI2002 Controller Internal Block Diagram (10 Lead TDFN package pin out shown)

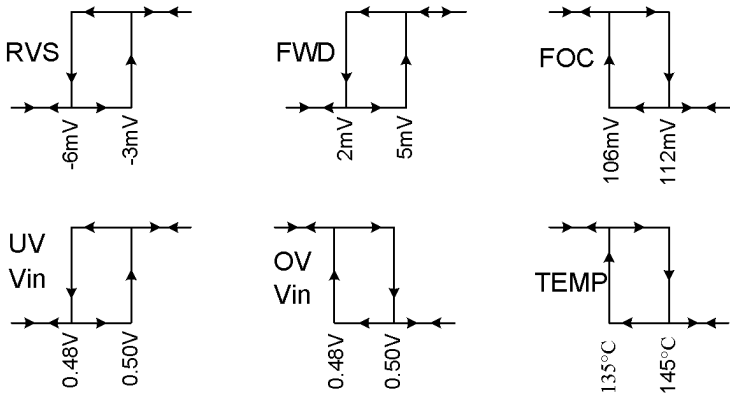


Figure 5: Comparator hysteresis, values are for reference only, please refer to the electrical specifications

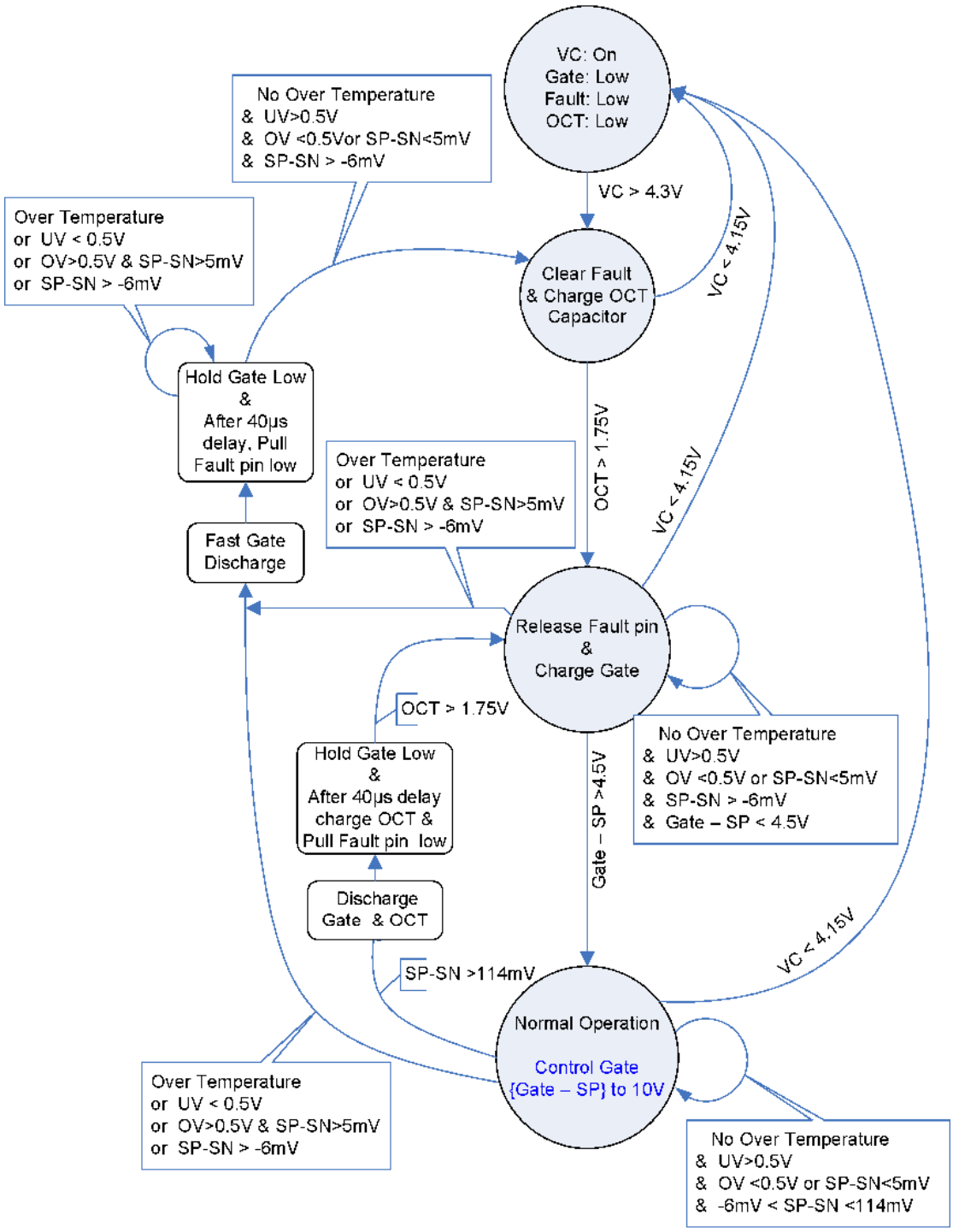


Figure 6: PI2002 State Diagram

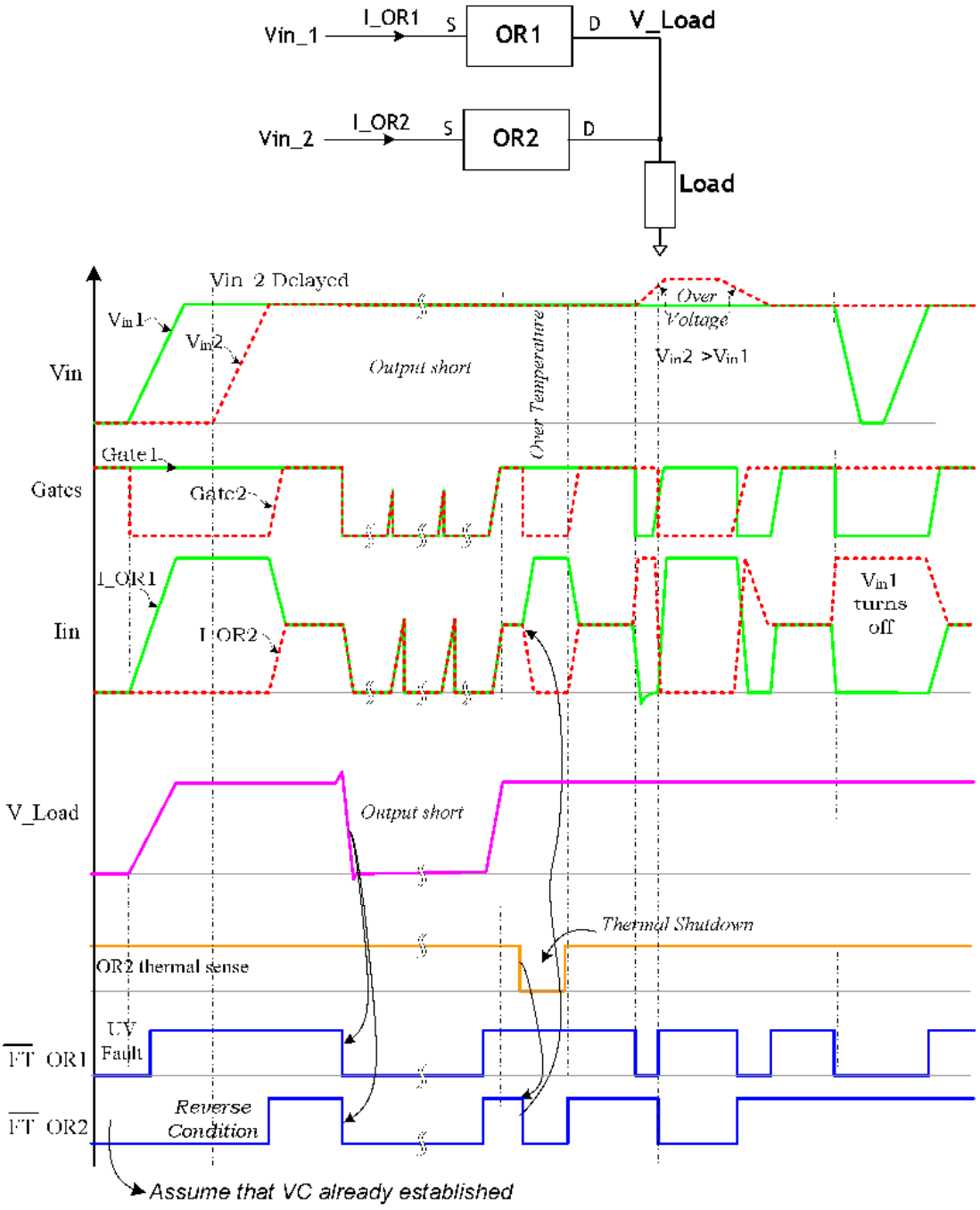


Figure 7: Timing diagram for two **PI2002** controllers in an Active ORing and Load Disconnect application

Typical Characteristics:

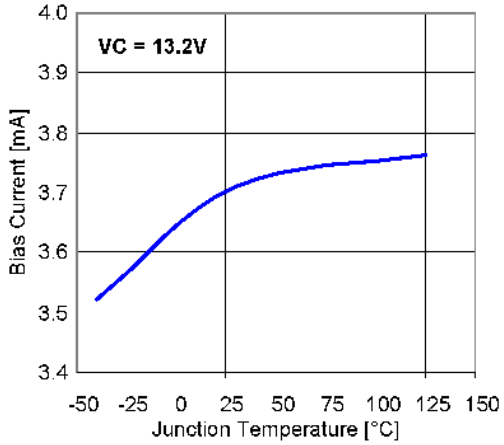


Figure 8: Controller bias current vs. temperature

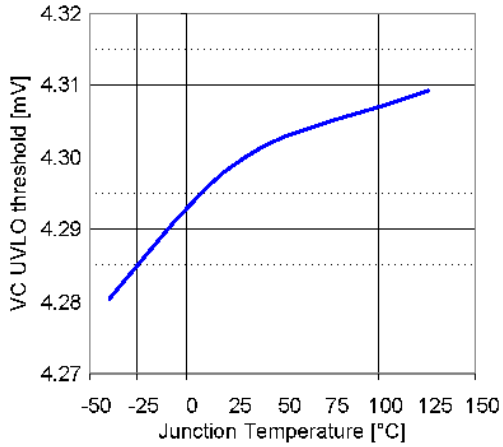


Figure 9: VC UVLO threshold vs. temperature

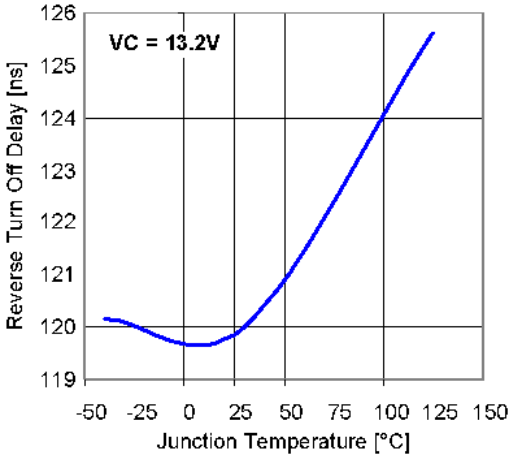


Figure 10: Reverse condition gate turn-off delay time vs. temperature.

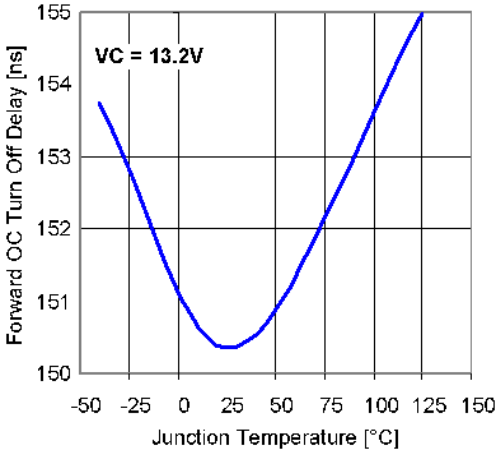


Figure 11: Forward Over-Current condition gate turn-off delay time vs. temperature.

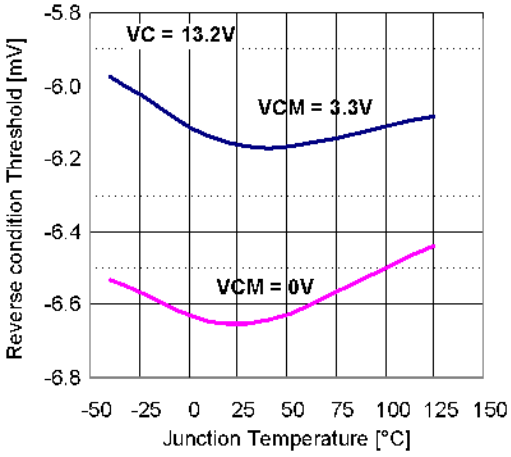


Figure 12: Reverse comparator threshold vs. temperature. ***VCM:*** *Common Mode Voltage*.

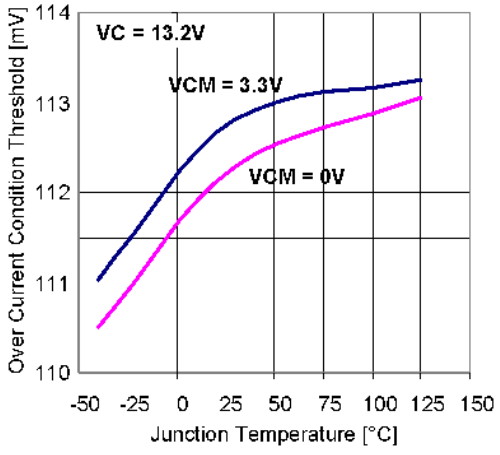


Figure 13: FOC comparator threshold vs. temperature. ***VCM:*** *Common Mode Voltage*.

Typical Characteristics: Continued

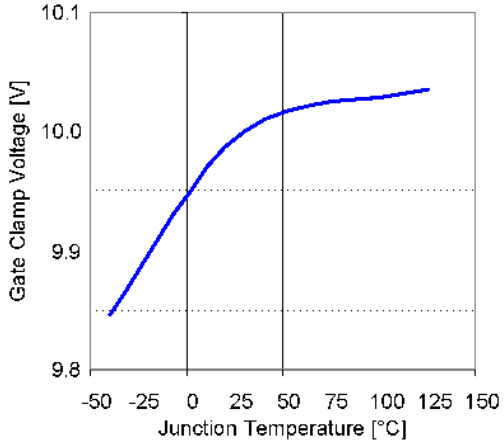


Figure 14: Gate to SP clamp voltage vs. temperature.

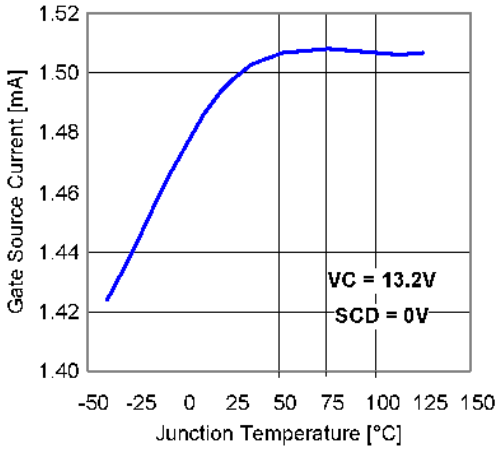


Figure 15: Gate output source current vs. temperature

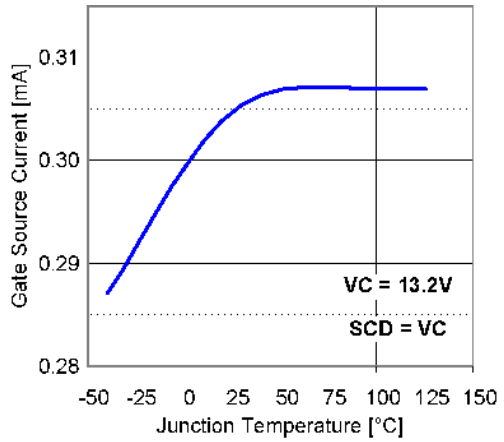


Figure 16: Gate output source current vs. temperature

Application Information:

The PI2002 is designed to replace ORing diodes and load disconnect switches in high current redundant power architectures. Replacing a traditional diode with a PI2002 controller IC and two low on-state resistance back-to-back N-channel MOSFETs will result in significant power dissipation reduction as well as board space reduction, efficiency improvement, input power source and output load protection and additional protection features. This section describes in detail the procedure to follow when designing with the PI2002 Active ORing controller and two back-to-back N-Channel MOSFETs. Two design examples are presented, one Active ORing with load disconnect design example and one low side disconnect switch example.

Fault Indication:

$\overline{FT}$ output pin is an open collector and should be pulled up to the logic voltage or to the controller VC via a resistor (10KΩ)

Over-Current Timer: OCT

Connect a capacitor, equal or less than 20nF, to set off time after over-current shutdown (see Figure 3).

Short Circuit Detect: SCD

Connect SCD pin to VC to avoid inrush current into a high capacitive load, or connect SCD to GND pin for fast MOSFET turn on.

Note: The SCD pin is not available in the SO-8 package and the controller is set for low Gate source current, 300µA.

Auxiliary Power Supply (Vaux):

Vaux is an independent power source required to supply power to the PI2002 VC input. The Vaux voltage should be higher than Vin (redundant power source output voltage) by the required gate-to-source voltage (Vgs) to fully enhance the MOSFET, plus 0.5V maximum gate to VC headroom (VHD_{VC-G})

$Vaux = Vin + Vgs + VHD_{VC-G}$

Where, VHD_{VC-G} is defined as the 0.5V maximum drop from VC in the *Gate Voltage High* (V_G) specification in the Gate Driver section of the Electrical Specification.

For example, if the bus voltage is 3.3V and the MOSFET requires 4.5V of Vgs to fully enhance the MOSFET, then Vaux should be at least 3.3V + 4.5V + 0.5V = 8.3V.

If Vaux is higher than 15V then a bias resistor (Rbias) is required, and should be connected between the PI2002 VC pin and Vaux. The resistor is selected based on the input voltage range.

Minimize the resistor value for low Vaux voltage levels to avoid a voltage drop that may reduce the VC voltage lower than required to drive the gate of the MOSFET. Select the value of Rbias using the following equations:

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}}$$

Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias}$$

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage (15V).

Where:

$Vaux_{\min}$: Vaux minimum voltage

$Vaux_{\max}$: Vaux maximum voltage

VC_{Clamp} : Controller clamp voltage, 15.5V

$IC_{\max}$: Controller maximum bias current (4.2mA)

N-Channel MOSFET Selection:

There are several factors that affect the MOSFET selection including cost, on-state resistance (Rds(on)), current rating, power dissipation, thermal conductivity, drain-to-source breakdown voltage (BVdss), gate-to-source voltage rating (Vgs), and gate threshold voltage ($Vgs_{(TH)}$).

The first step is to select suitable MOSFETs based on the BVdss requirement for the application. The BVdss voltage rating should be higher than the applied Vin voltage plus expected transient voltages. Stray parasitic inductance in the circuit can also contribute to significant transient voltage conditions, particularly during MOSFET turn-off after a reverse current fault has been detected. In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFET. Depending on the output impedance of the system, the reverse current may reach over 60A in some conditions before the MOSFET is turned off. Such high current conditions will store energy even in a small parasitic element. For example, a 1nH parasitic inductance with 60A reverse current will store 1.8µJ ($½Li^2$). When the MOSFET is turned off, the stored energy will be released and will produce high negative voltage ringing at the MOSFETs input. This event will create a high voltage difference across the MOSFETs.

Note:

Since the two MOSFETs are connected in to back-to-back configuration, the maximum breaking voltage is BVdss of one MOSFET plus one diode forward voltage.

The MOSFET current rating and maximum power dissipation are closely related. Generally the lower the MOSFET Rds(on), the higher the current capability and the lower the resultant power dissipation. This leads to reduced thermal management overhead, but will ultimately be higher cost compared to higher Rds(on) parts. It is important to understand the primary design goal objectives for the application in order to effectively trade off the performance of one MOSFET versus another.

Power dissipation in active ORing circuits is derived from the total source current and the on-state resistance of the selected MOSFET.

MOSFET power dissipation:

$$Pd_{MOSFET} = Is^2 * Rds(on)$$

Where :
Is : Source Current
Rds(on) : MOSFET on-state resistance

Note:
In the calculation use Rds(on) at maximum MOSFET temperature because Rds(on) is temperature dependent. Refer to the normalized Rds(on) curves in the MOSFET manufacturers datasheet. Some MOSFET Rds(on) values may increase by 50% at 125°C compared to values at 25°C.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise_{MOSFET} = Rth_{JA} * Pd_{MOSFET} = Rth_{JA} * Is^2 * Rds(on),$$

Where:
Rth_{JA}: Junction-to-Ambient thermal resistance

Rds(on) and PI2002 sensing:
The PI2002 senses voltage across the ORing MOSFETs via the SP and SN pins to determine the status of the current through the MOSFETs. Refer Figure 1a. When the MOSFETs are fully enhanced, the total drop across the back to back MOSFETs (and between SP and SN) is; V_{SD}=Rds(on)*Is * 2.

The reverse current threshold is set for -6mV and when the differential voltage between the SP & SN pins is more negative than -6mV, i.e. SP-SN≤-6mV, the PI2002 detects a reverse current fault condition and pulls the MOSFET gate pin low to turn off the MOSFET and prevent further reverse current. The reverse current fault protection disconnects the power source fault condition from the redundant bus and allows the system to keep running.

The GATE pin output voltage is clamped to 11V maximum with respect to the SN pin. The 11V clamp should be adequate for protecting MOSFETs with maximum Vgs ratings of ±12V or greater.

OV/UV resistor selection:
The UV and OV comparator inputs are used to monitor the input voltage and will indicate a fault condition when this voltage is out of range. The UV and OV pins can be configured in two different ways, either with a divider on each pin, or with a three-resistor divider to the same node, enabling the elimination of one resistor. Under-Voltage is monitored by the UV pin input and Over-Voltage is monitored with the OV pin input.

Note: The OV pin is not available in the SO-8 package and OV function is disabled.

The Fault pin ($\overline{FT}$) will indicate a fault (active low) when the UV pin is below the threshold or when the OV pin is above the threshold. The UV and OV thresholds are 0.50V typical with 25mV hysteresis and their input current is less than ±1µA. It is important to consider the maximum current that will flow in the resistor divider and maximum error due to UV and OV input current. Set the resistor current to 100µA or higher to maintain 1% accuracy for UV and OV due to the bias current.

The three-resistor voltage divider configuration for both UV and OV to monitor the same voltage node is shown in Figure 17:

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

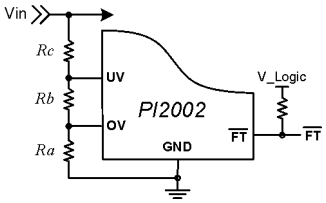


Figure 17: UV & OV three-resistor divider configuration.

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

Set Ra value based on system allowable current

$$I_{Ra}\ Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

$$Rb = Ra \bullet \left(\frac{V(OV)}{V(UV)} - 1 \right)$$

$$Rc = (Ra + Rb) \bullet \left(\frac{V(UV)}{V_{TH}} - 1 \right)$$

Where:
$V(UV_{TH})$: UV threshold voltage
$V(OV_{TH})$: OV threshold voltage
V(UV) : UV voltage

I_{Ra} : Ra current.

Alternatively, a two-resistor voltage divider configuration can be used and is shown in (Figure 18).

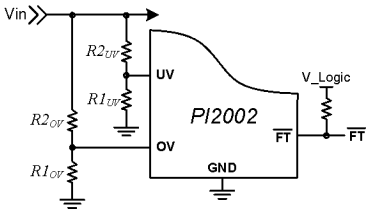


Figure 18: Two-resistor divider configuration

The UV resistor voltage divider can be obtained from the following equations:

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{UV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

I_{RUV} : $R1_{UV}$ current

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{OV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right)$$

Where:

$V(OV_{TH})$: OV threshold voltage

I_{ROV} : $R1_{OV}$ current

Typical application Example 1:
High Side Active ORing:

Requirement:
Redundant Bus Voltage = 3.3V
Load Current = 15A (assume through each redundant path)
Maximum Ambient Temperature = 75°C
Auxiliary Voltage = 12V (11V to 13V)

Solution:

1. A single PI2002 with two suitable external MOSFETs for each redundant 3.3V power source should be used, configured as shown in the circuit schematic in Figure 19
2. **Select a suitable N-Channel MOSFET:** Most industry standard MOSFETs have a Vgs rating of +/-12V or higher. Select an N-Channel MOSFET with a low Rds(on) which is capable of supporting the full load current with some margin, so a MOSFET capable of at least 18A in steady state is reasonable. An exemplary MOSFET having these characteristic is FDS6162N7 from Fairchild.

From FDS6162N7 datasheet:

- N-Channel MOSFET
- V_{DS}= 20V
- I_D = 23A continuous drain current
- $V_{GS(MAX)}$= ± 12V
- $R_{\theta JA}$= 40°C/W
- $R_{DS(on)}$=2.9mΩ typical at I_D=23A, V_{GS}≥4.5V, T_J=25°C

Reverse current threshold is:

$$I_{RVS} = \frac{V_{RVS-TH}}{2 * Rds(on)} = \frac{-6mV}{2 * 2.9m\Omega} = -1.03A$$

Forward over-current threshold is:

$$I_{FOC} = \frac{V_{FOC-TH}}{2 * Rds(on)} = \frac{114mV}{2 * 2.9m\Omega} = 19.66A$$

Power dissipation final junction temperature for each MOSFET:
Rds(on) is 3.5mΩ maximum at 25°C & 4.5Vgs and will increase as the temperature increases. Add 25°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (75°C + 25°C) Rds(on) will increase by 28%.

$Rds(on) = 3.5m\Omega * 1.28 = 4.48m\Omega$ maximum at 100°C

$Trise = Rth_{JA} * Is^2 * Rds(on)$

Maximum Junction temperature

$T_{J\max} = T_A + Trise$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.48m\Omega\right) = 115°C$$

Recalculate based on calculated Junction temperature, 115°C.

At 115°C Rds(on) will increase by 32%.

$$Rds(on) = 3.5m\Omega * 1.32 = 4.62m\Omega$$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.62m\Omega\right) = 116.5°C$$

3. **Vaux:** Make sure Vaux voltage is higher than Vin (power source output) by the voltage required to fully enhance the MOSFET. Minimum required Vaux = Vin + Vgs + 0.5V = 3.3V + 4.5V + 0.5V = 8.3V. Since 8.3V is less than the 11V minimum Aux supply voltage, there is sufficient voltage available to drive the gate of the MOSFET.
4. **SP and SN pins:** Connect the SP pin to the MOSFET drain pin at the input and the SN pin to the MOSFET drain pin at the load side.
5. **OCT pin:** Connect 18nF capacitor between OCT pin and the GND pin to achieve the maximum off time after forward over-current condition occurs.
6. **SCD pin:** Connect the SCD pin to the GND pin for fast MOSFET enhancement.
7. $\overline{FT}$ **pin**: Connect to the logic input and to the logic power supply via a 10KΩ resistor.
8. **Program UV and OV to monitor input voltage:** Program UV at 3.0V and OV at 3.6V

   Use the three-resistor divider configuration:

$$I_{Ra} = 200\mu A$$

$$Ra = \frac{V(UV_{TH})}{I_{Ra}} = \frac{500mV}{200\mu A} = 2.5k\Omega \text{ or } 2.49k\Omega\ 1\%$$

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right) = 2.49k\Omega\left(\frac{3.6V}{3.0V} - 1\right) = 498\Omega$$

or 499Ω 1%

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

$$= (2.49k\Omega + 499\Omega)\left(\frac{3.0V}{500mV} - 1\right) = 14.95k\Omega$$

or 15kΩ 1%

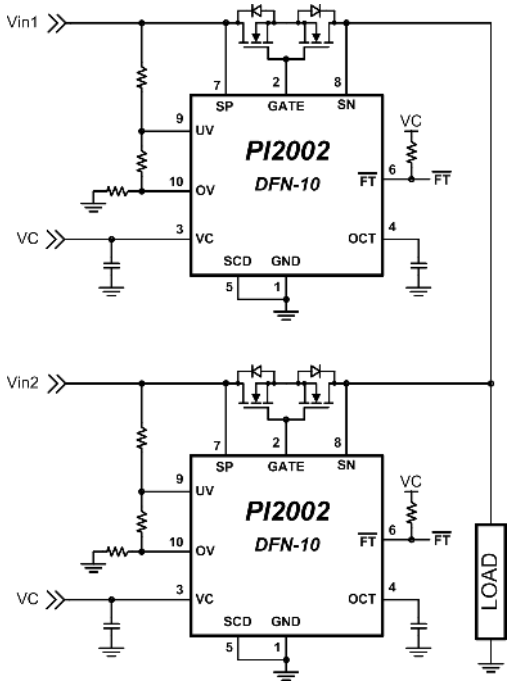


Figure 19: High side Active ORing function.

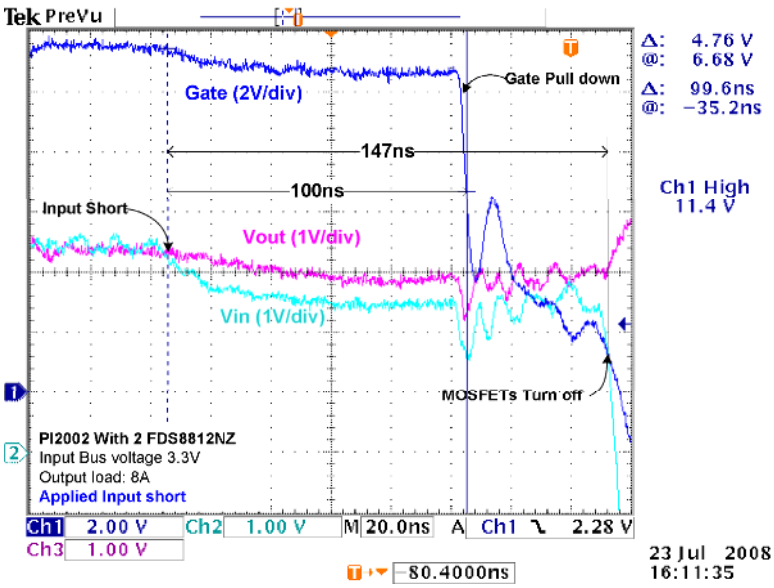


Figure 20: PI2002 performance in example 1, applied short at Vin1.

Typical application Example 2:
Low side disconnect switch

Requirement:

Bus Voltage = -48V (-36V to -60V, 100V for 100ms transient)

Maximum operating load current = 5A

Load current shutdown set at = 6A

Maximum Ambient Temperature = 60°C

Solution:

1. A PI2002 with a suitable MOSFET for -48V power source should be used and configured as shown in Figure 22. The VC is biased from the return line through a bias resistor.
2. **Select a suitable N-Channel MOSFET:** Select the N-Channel MOSFET with voltage rating higher than the input voltage, Vin, plus any expected transient voltages, with a low Rds(on) that is capable of supporting the full load current with margin. For instance, a 100V rated MOSFET with 10A current capability is suitable. An exemplary MOSFET having these characteristic is Si4486EY from Vishay Siliconix.

From Si4486EY datasheet:

- N-Channel MOSFET
- V_{DS}= 100V
- I_D = 23A continuous drain current at 125°C
- $V_{GS(MAX)}$ = ± 20V
- $R_{\theta JA}$= 50°C/W
- $R_{DS(on)}$=20mΩ typical at V_{GS}=10V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{20m\Omega} = -300mA$$

Power dissipation:

Rds(on) is 25mΩ maximum at 25°C & 10Vgs and will increase as the temperature increases. Add 40°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (60°C + 40°C) Rds(on) will increase by 63%.

$Rds(on) = 25m\Omega * 1.63 = 41m\Omega$ maximum at 100°C

Maximum Junction temperature

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 41m\Omega\right) = 111°C$$

Recalculate based on calculated Junction temperature, 111°C.

At 111°C Rds(on) will increase by 71%.

$Rds(on) = 25m\Omega * 1.71 = 4.75m\Omega$ maximum at 111°C

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 42.75m\Omega\right) = 113°C$$

Vaux: Connect each controller to the return path with a separate bias resistor, Rbias.

To reduce $Rbias$ power dissipation, VC_{clamp} is selected at 13V which is less than the actual PI2002 clamp voltage (15V typical). 13V is higher than PI2002 maximum gate clamp voltage (11V).

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}} = \frac{36V - 13V}{4.2mA} = 5.48K\Omega$$

or 5.49KΩ

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clampMIN})^2}{Rbias} = \frac{(60V - 15V)^2}{5.49K\Omega} = 369mW$$

3. **Select sense resistor:** Sense resistor is selected based on load current shutdown. Where

   $$R_{Sense} = \frac{V_{FOC-TH}}{I_{Shutdown}} = \frac{114mV}{6A} = 19m\Omega$$

   Select 20mΩ resistor

   20mΩ Sense Resistor power dissipation at maximum operating current

   $$Pd_{RSense} = I_{\max}{}^2 * R_{Sense} = (5A)^2\, 20m\Omega = 0.5W$$

   As an exemplary selected 1206 20mΩ/1W/1% sense resistor from Vishay-Dale:

   Part Number: WSL1206R0200FEK

   Maximum current turn off:

   $$Isd_{MAX} = \frac{V_{FOC-TH-MAX}}{R_{Sense}} = \frac{121mV}{20m\Omega} = 6.05A$$

   Minimum current turn off:

   $$Isd_{MIN} = \frac{V_{FOC-TH-MIN}}{R_{Sense}} = \frac{107mV}{20m\Omega} = 5.35A$$

4. **SP and SN pins:** Connect the SP pin to the MOSFET source and controller GND pin, and connect the SN pin to Vin- and the drain of the MOSFET.

5. **OCT pin:** Connect 18nF capacitor between OCT pin and the GND pin to achieve the maximum off time after forward over-current condition occurs.

6. **SCD pin:** Connect the SCD pin to the VC pin for slow MOSFET turn on to avoid over-current shutdown due to inrush current.

7. $\overline{FT}$ **pin**: Connect the $\overline{FT}$ pin to logic input and to the logic power supply or to the VC pin via a resistor.

UV and OV inputs: UV and OV are not used in this example. Connect UV pin to VC pin and OV pin to GND pin do not leave them unconnected.

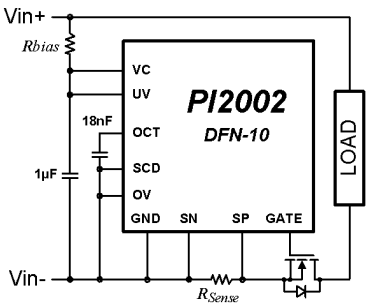


Figure 22: PI2002 (10L-TDFN package) in low side disconnect switch application

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for a TDFN PI2002 and SO-8/PowerPak MOSFET is shown in Figure 23:

- It is best to connect the gate of the MOSFETs to the GATE pin of the controller with a short and wide trace.
- The GND pin of the controller carries high peak current and it should be returned to the ground plane through a low impedance path.
- Connections from the SP and SN pins to Vin and Vout respectively very close to the MOSFETs, SP to Q1 drain pin and SN to Q2 drain pin.
- The VC bypass capacitor should be located as close as possible to the VC and GND pins. Place the PI2002 and VC bypass capacitor on the same layer of the board. The VC pin and C_{VC} PCB trace should not contain any vias.
- Connect all MOSFET Q1 Drain pins together with a wide trace to reduce trace parasitics and to accommodate the high current input. Similarly, connect all MOSFET Q2 Drain pins together with a wide trace to accommodate the high current output. Q1 and Q2 Sources should be very close from each other and their pins should be connected with a short trace.
- Connect the power source very close to the Q1 drain connection to reduce the effects of stray parasitics. If a short trace is not possible, connect C3 (typically 1µF) as shown in Figure 23.

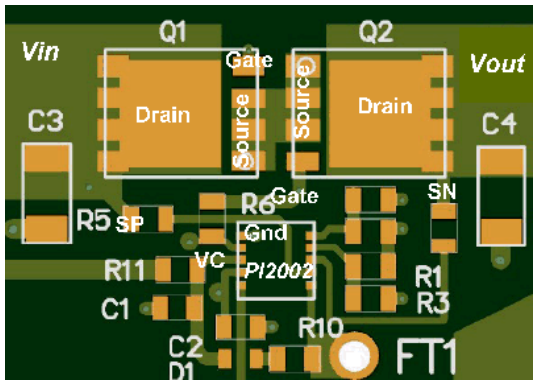
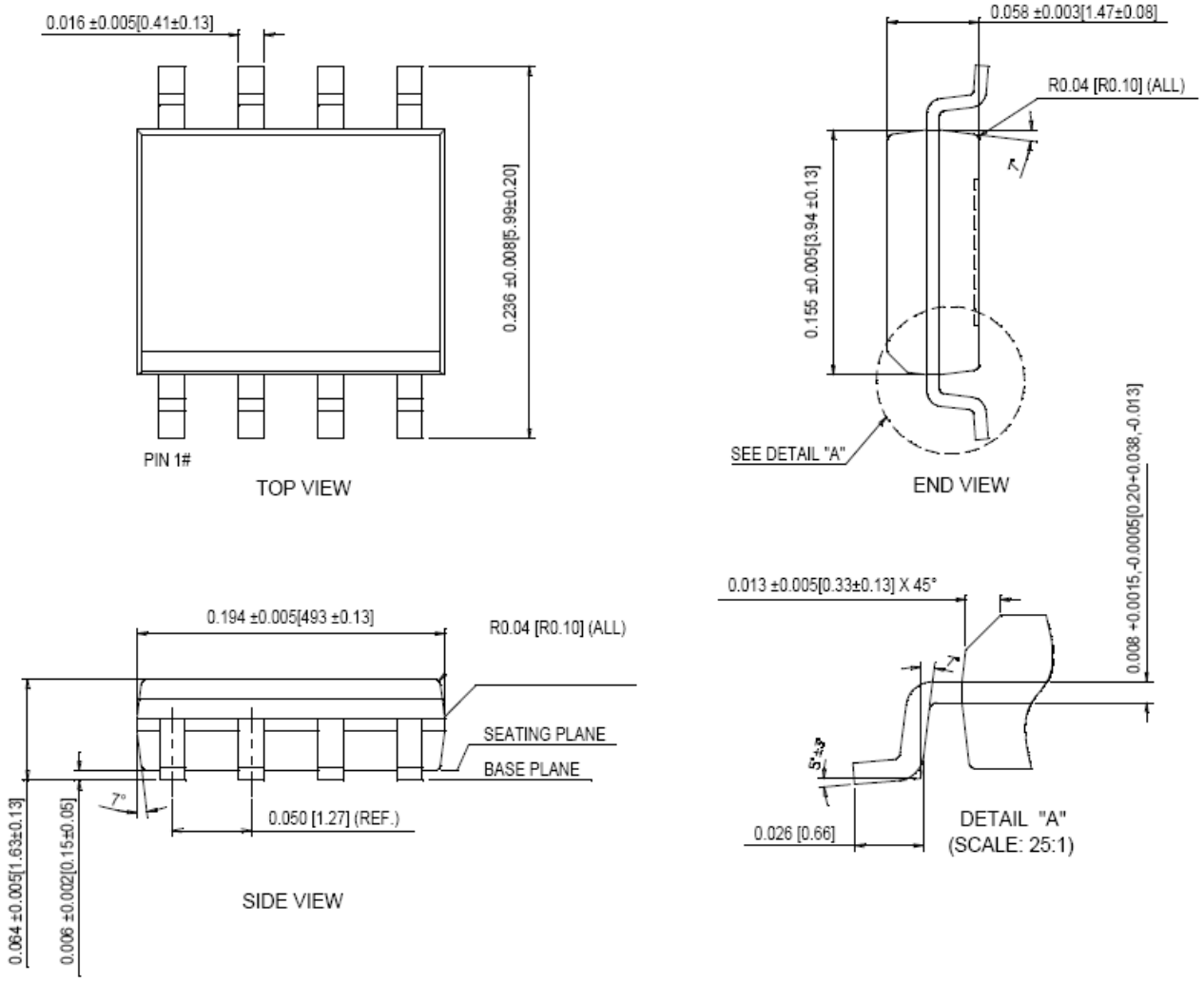


Figure 23: PI2002 and MOSFET layout recommendation

Figure 24: PI2002 Mounted on PI2002-EVAL1
Please visit www.picorpower.com for information on PI2002-EVAL1

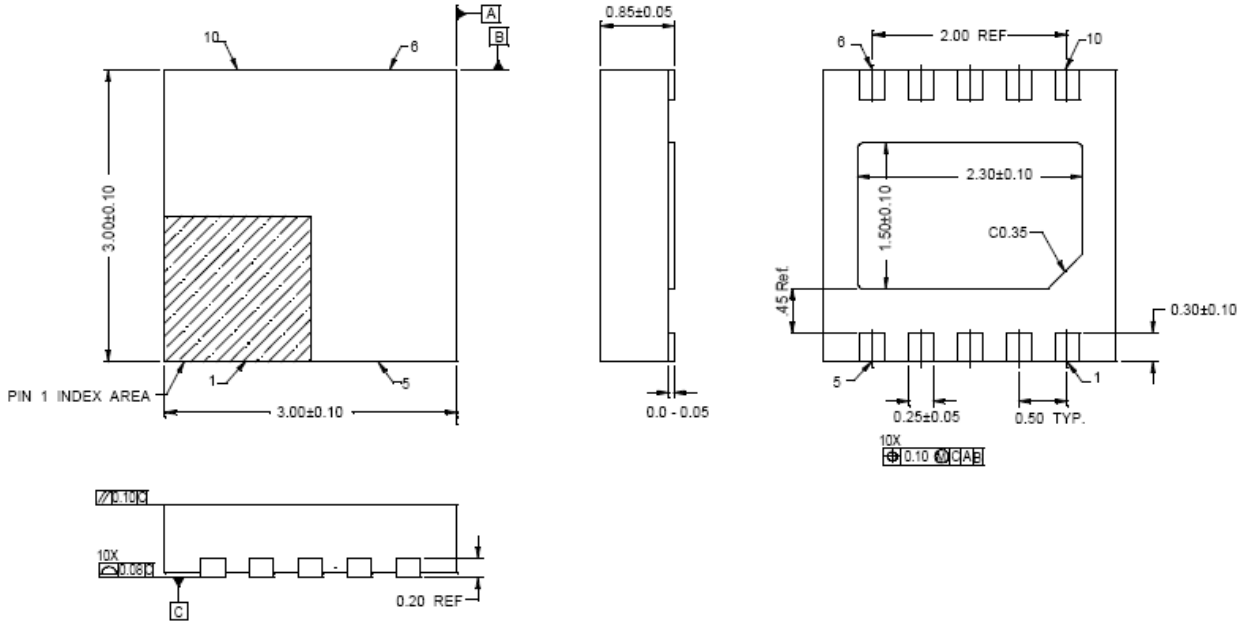
Package Drawings: 8 Lead SOIC



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN INCHES [MM]
2. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 [0.15] PER SIDE
3. FORMED LEADS SHALL BE PLANAR WITH REPECT TO ONE ANOTHER WITHIN 0.003 [0.08] AT SEATING PLANE
4. GENERAL ANGLE TOLERANCES TO BE +/-2"
5. GENERAL TOLERANCES TO BE +/- 0.005 [0.13]
6. THIS POD COMPLIES TO MS-012 ISSUE C

Package Drawings: 10 Lead TDFN



NOTES :

1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity does not exceed .05mm
3. Package is variation of JEDEC MO-229
4. Warpage does not exceed .05mm

Ordering Information

Part Number	Package	Transport Media
PI2002-00-QEIG	3mm x 3mm 10L TDFN	Tape &Reel
PI2002-00-SOIG	8L SOIC	Tape &Reel

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Vicor products are guaranteed for two years from date of shipment against defects in material or workmanship when in normal use and service. This warranty does not extend to products subjected to misuse, accident, or improper application or maintenance. Vicor shall not be liable for collateral or consequential damage. This warranty is extended to the original purchaser only.

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Vicor Corporation
25 Frontage Road
Andover, MA 01810
USA

Picor Corporation
51 Industrial Drive
North Smithfield, RI 02896
USA

Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com
Tel: 800-735-6200
Fax: 978-475-6715