5A, 18V, 650kHz ADAPTIVE COT STEP-DOWN CONVERTER

Description

The AP65550 is an adaptive, constant-on-time mode synchronous buck converter providing high-efficiency, excellent transient response and high DC output accuracy for low-voltage regulation in digital TVs and monitors.

The constant-on-time control scheme handles wide input/output voltage ratios and provides low external component count. The internal proprietary circuit enables the device to adopt both low equivalent series resistance (ESR) output capacitors, such as SP-CAP or POSCAP and ultra-low ESR ceramic capacitors.

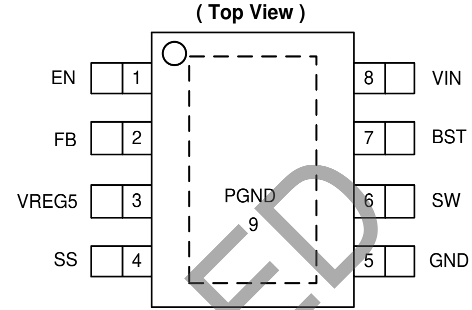
The adaptive, on-time control supports seamless transition between continuous conduction mode (CCM) at higher load conditions and discontinuous conduction mode (DCM) at lighter load conditions.

DCM allows AP65550 to maintain high efficiency at light load conditions. The AP65550 also features programmable soft-start, UVLO, OTP and OCP to protect the circuit.

This regulator is available in SO-8EP and U-DFN3030-10 packages.

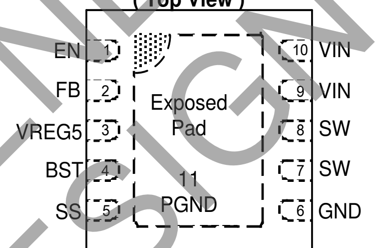
Pin Assignments

(Top View)



SO-8EP

(Top View)



U-DFN3030-10

Features Applications

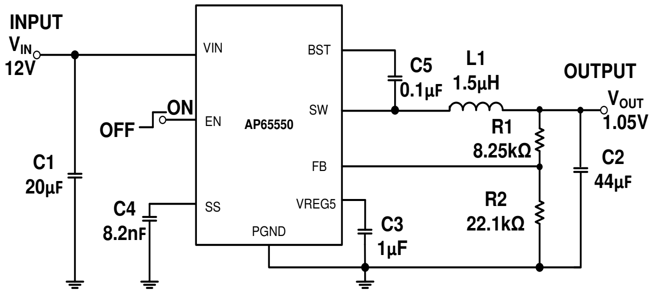
- Fixed Frequency Emulated Constant On-Time Control
- Good Stability Independent of the Output Capacitor ESR
- Fast Load Transient Response
- Synchronous Rectification: 65mΩ Internal High-Side Switch and 36mΩ Internal Low-Side Switch
- Wide Input Voltage Range: 4.5V to 18V
- Output Voltage Range: 0.765V to 6V
- 5A Continuous Output Current
- 650kHz Switching Frequency
- Built-in Over Current Limit
- Built-in Thermal Shutdown Protection
- Programmable Soft-Start
- Pre-Biased Start-Up
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Gaming Consoles
- Flat Screen TV Sets and Monitors
- Set-Top Boxes
- Distributed Power Systems
- Home Audio
- Consumer Electronics
- Network Systems
- FPGA, DSP and ASIC Supplies
- Green Electronics

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



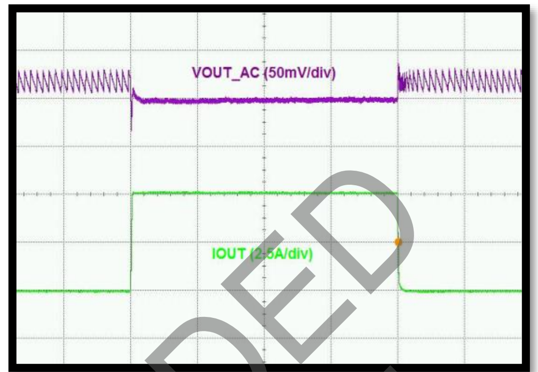


Figure 1 Typical Application Circuit

Pin Descriptions

Pin Name	Pin Number		Function
	SO-8EP	U-DFN3030-10	
EN	1	1	Enable input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn off. Pull up with 100kΩ resistor to VIN for automatic startup.
FB	2	2	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage.
VREG5	3	3	Internal power supply output pin to connect an additional capacitor. Connect a 1µF (typical) capacitor as close as possible to the VREG5 and PGND. This pin is not active when EN is low.
SS	4	5	Soft-start control input pin. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period.
GND	5	6	Ground pin is the main power ground for the switching circuit.
SW	6	7, 8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
BST	7	4	Bootstrap pin. A bootstrap capacitor is connected between the BST pin and SW pin. The voltage across the bootstrap capacitor drives the internal high-side NMOS switch. A 0.1µF (typical) capacitor is required for proper operation.
VIN	8	9, 10	Supply input pin. A capacitor should be connected between the VIN pin and PGND pin to keep the DC input voltage constant.
PGND	9 (Exposed Pad)	11 (Exposed Pad)	Power ground. Exposed pad must be connected to a single point GND and as large of PGND plane as possible for maximum thermal performance.

Functional Block Diagram

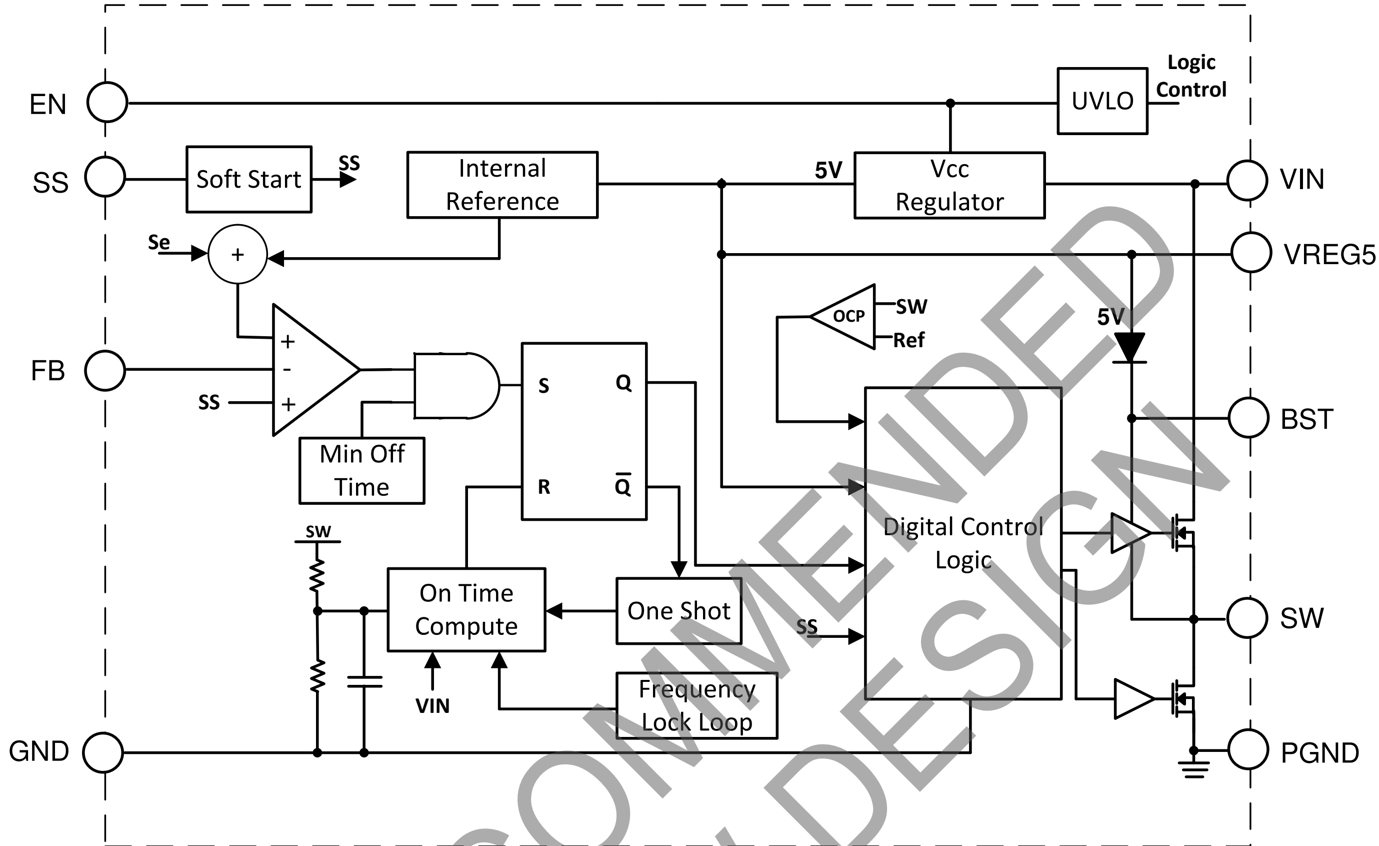


Figure 2 Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to 20	V
V_{VREG5}	VREG5 Pin Voltage	-0.3V to +6.0	V
V_{SW}	Switch Node Voltage	-1.0 to VIN +0.3	V
V_{BST}	Bootstrap Voltage	-0.3 to VSW +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +6.0	V
V_{SS}	Soft-start PIN	-0.3V to +6.0	V
V_{GND}	GND Pin Voltage	-0.3 to 0.3	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	2	kV
MM	Machine Model	200	V

Notes: 4. Stresses greater than the '*Absolute Maximum Ratings*' specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SO-8EP	39.4	°C/W
θ_{JC}	Junction to Case	SO-8EP	8.6	°C/W
θ_{JA}	Junction to Ambient	U-DFN3030-10	42	°C/W
θ_{JC}	Junction to Case	U-DFN3030-10	6	°C/W

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

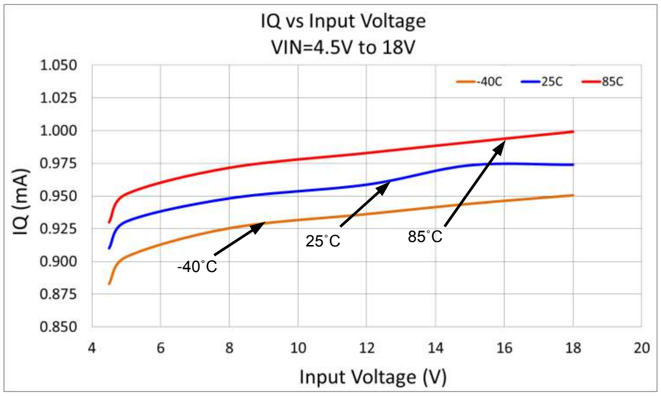
Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.5	18.0	V
T_J	Operating Junction Temperature Range	-40	+125	°C
T_A	Operating Ambient Temperature Range	-40	+85	°C

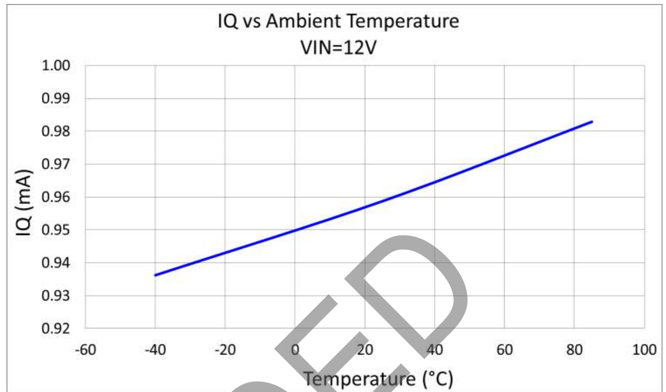
Notes: 6. Test condition: SO-8EP, U-DFN3030-10: Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper with minimum recommended pad layout.
7. The device function is not guaranteed outside of the recommended operating conditions.

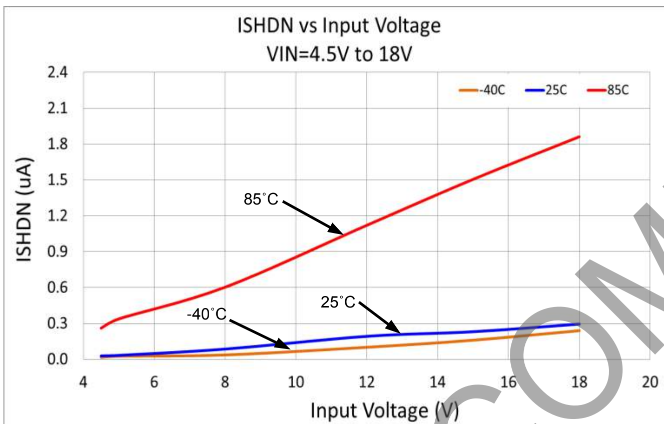
Electrical Characteristics (@T_A = +25°C, V_{IN} = 12V, unless otherwise specified.)

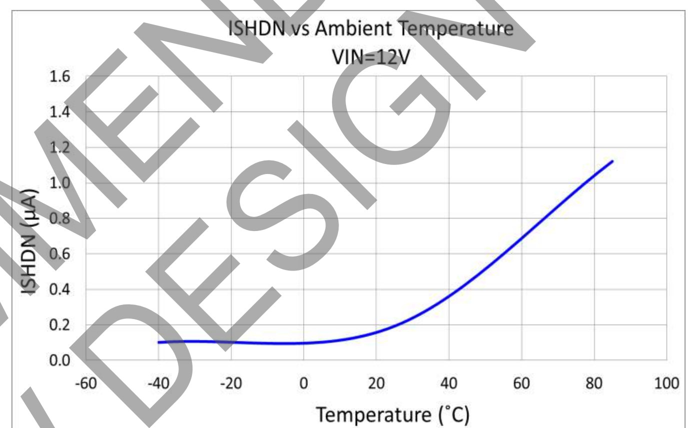
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE (VIN PIN)						
Input Voltage	V_{IN}	—	4.5	—	18	V
Quiescent Current	I_Q	V_{FB}=0.85V	—	0.9	—	mA
Shutdown Supply Current	I_{SHDN}	V_{EN}=0V	—	3.6	10	μA
UNDER VOLTAGE LOCKOUT						
UVLO Threshold	V_{UVLO}	V_{IN} Rising Test VREG5 Voltage	3.45	3.75	4.05	V
UVLO Hysteresis	V_{HYS}	V_{IN} Falling Test VREG5 Voltage	0.19	0.32	0.45	V
ENABLE (EN PIN)						
EN High-level Input Voltage	V_{ENH}	—	1.9	—	—	V
EN Low-level Input Voltage	V_{ENL}	—	—	—	0.6	V
VOLTAGE REFERENCE (FB PIN)						
Feedback Voltage	V_{FB}	V_{OUT}=1.05V, T_A = -40°C to +85°C, CCM	0.753	0.765	0.777	V
Feedback Bias Current	I_{FB}	V_{FB}=0.8V	-0.1	0	0.1	μA
VREG5 OUTPUT						
VREG5 Output Voltage	V_{VREG5}	6.0V<V_{IN}<18V 0<I_{VREG5}<5mA	4.7	5.1	5.5	V
Source Current Capability	—	V_{IN}=6V, V_{VREG5}=4V	—	110	—	mA
Load Regulation	—	0<I_{VREG5}<5mA	—	—	60	mV
Line Regulation	—	6.0V<VIN<18V I_{VREG5}=5mA	—	—	20	mV
MOSFET						
High-side Switch On-Resistance	R_{DSONH}	—	—	65	—	mΩ
Low-side Switch On-Resistance	R_{DSONL}	—	—	36	—	mΩ
CURRENT LIMIT						
Valley Current Limit	I_{LIM}	L=1.5μH, T_A = -40°C to +85°C	5.6	6.4	7.9	A
ON-TIME TIMER						
On Time	t_{ON}	V_{IN}=12V, VOUT=1.05V	—	150	—	ns
Minimum Off Time	$t_{OFF-MIN}$	V_{FB}=0.7V	—	260	310	ns
THERMAL SHUTDOWN						
Thermal Shutdown	T_{OTSD}	—	—	+160	—	°C
Thermal Shutdown Hysteresis	T_{HYS}	—	—	+30	—	°C
SOFT START (SS PIN)						
Soft-Start Source Current	$I_{SS-SOURCE}$	V_{SS}=1.2V	4.2	6.0	7.8	μA
Soft-Start Discharge Current	$I_{SS-DISCHARGE}$	V_{SS}=0.5V	0.1	0.2	—	mA

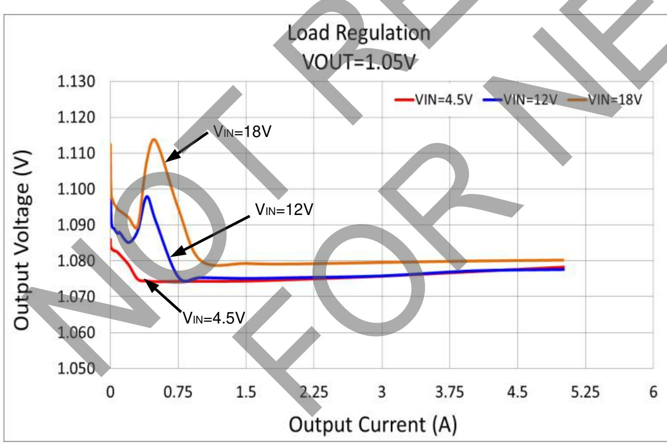
Typical Performance Characteristics (@T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, unless otherwise specified.)

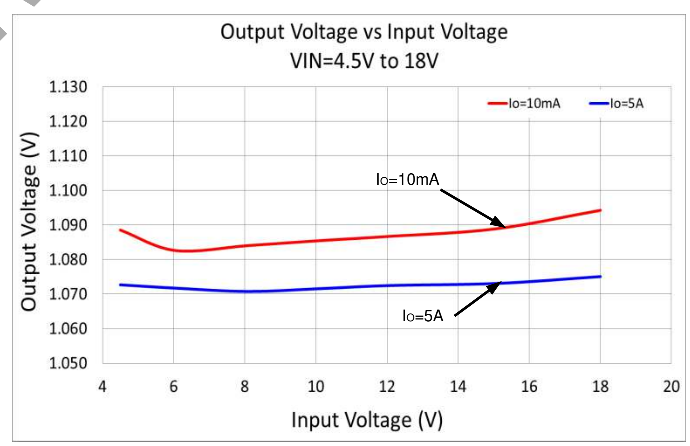




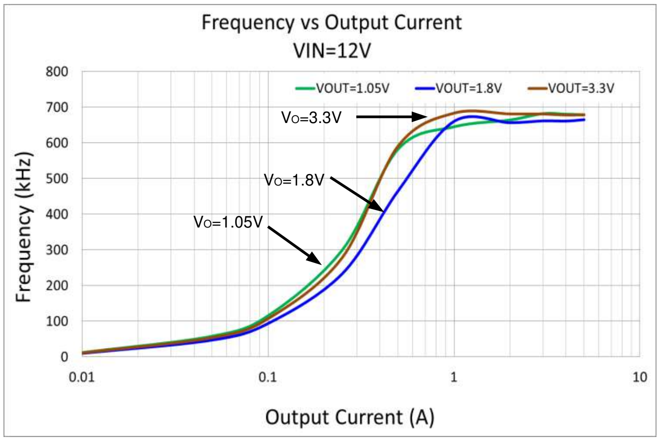


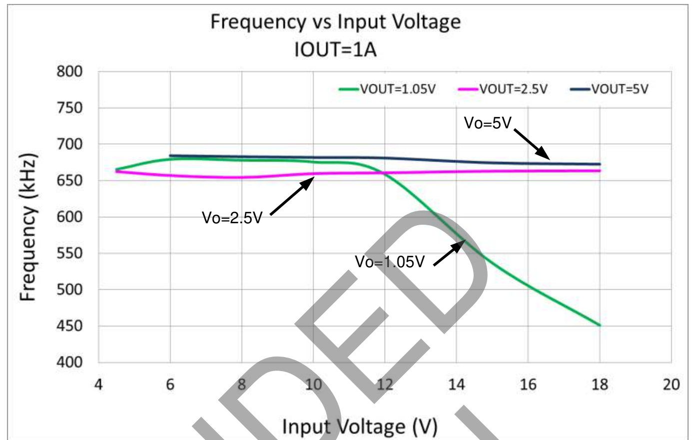


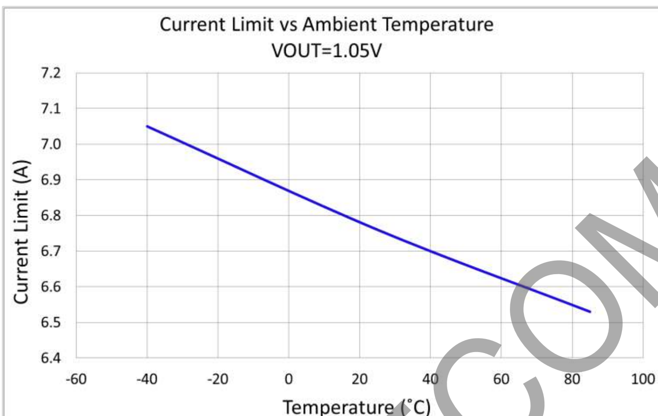


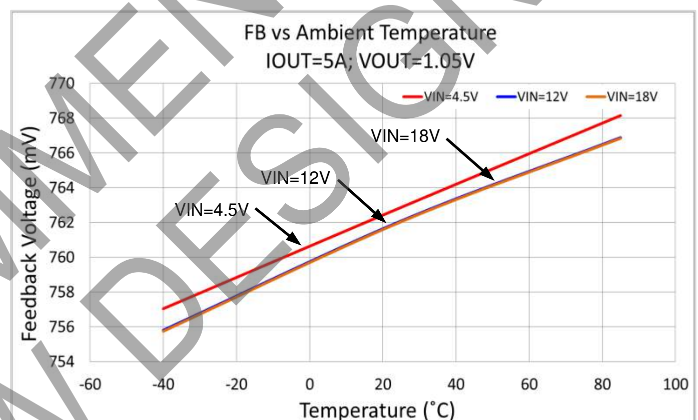


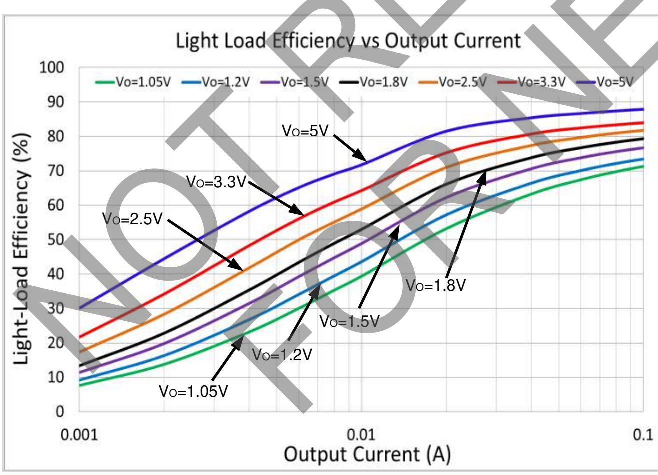
Typical Performance Characteristics (continued) (@T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, unless otherwise specified.)

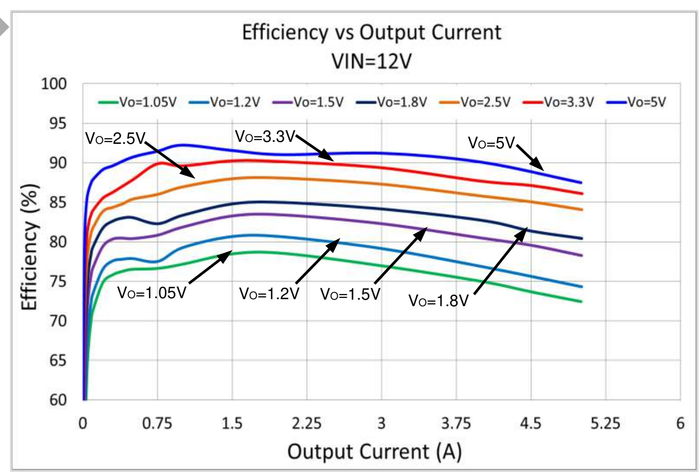








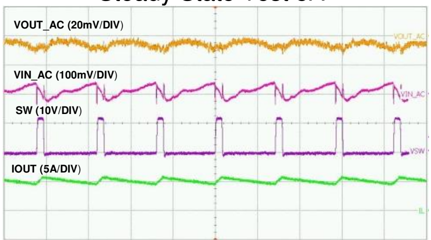




Typical Performance Characteristics (continued)

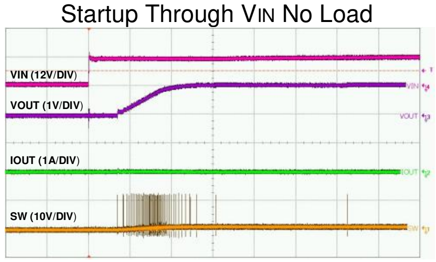
(@T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.05V, L = 1.5µH, C1 = 20µF, C2 = 44µF, unless otherwise specified.)

Steady State Test 5A



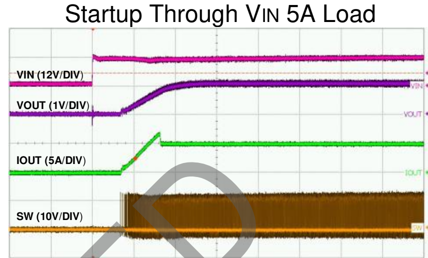
Time-1µs/div

Startup Through VIN No Load



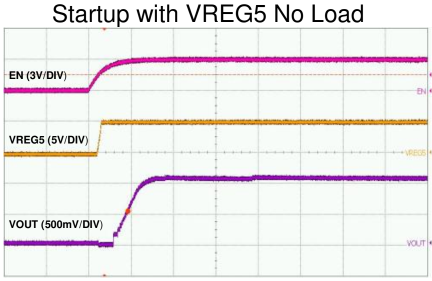
Time-500µs/div

Startup Through VIN 5A Load



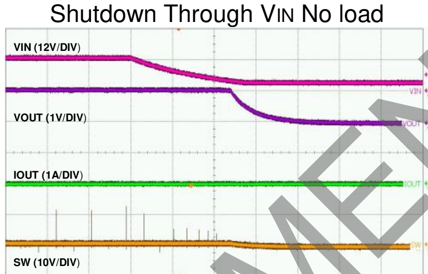
Time-500µs/div

Startup with VREG5 No Load



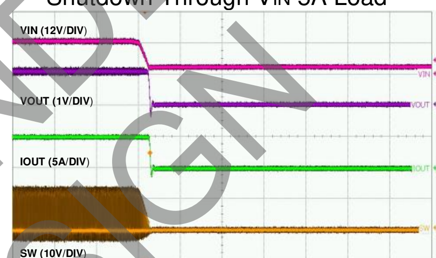
Time-1ms/div

Shutdown Through VIN No load



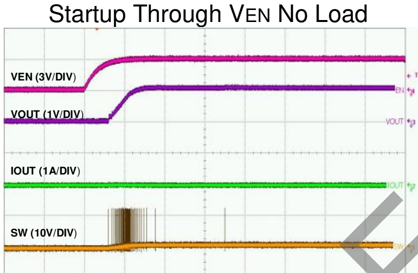
Time-50ms/div

Shutdown Through VIN 5A Load



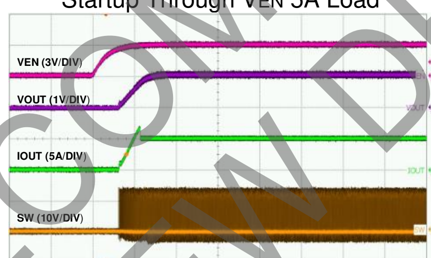
Time-500µs/div

Startup Through VEN No Load



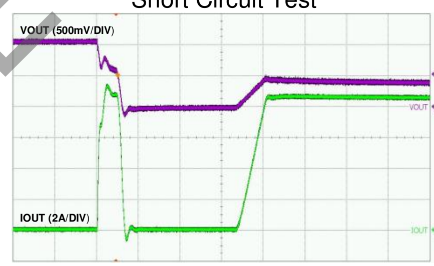
Time-1ms/div

Startup Through VEN 5A Load



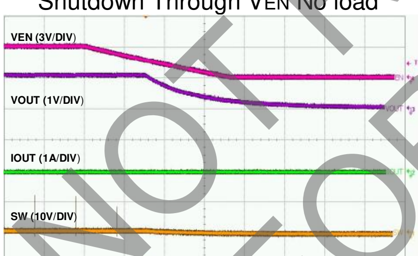
Time-1ms/div

Short Circuit Test



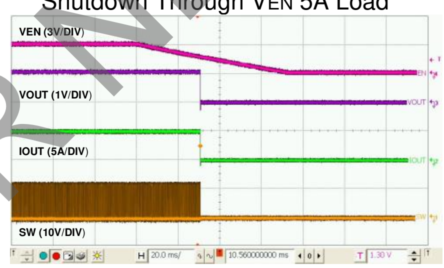
Time-100µs/div

Shutdown Through VEN No load



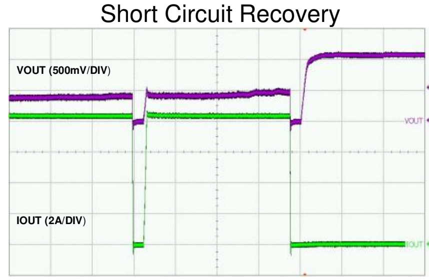
Time-20ms/div

Shutdown Through VEN 5A Load



Time-20ms/div

Short Circuit Recovery



Time-1ms/div

Application Information

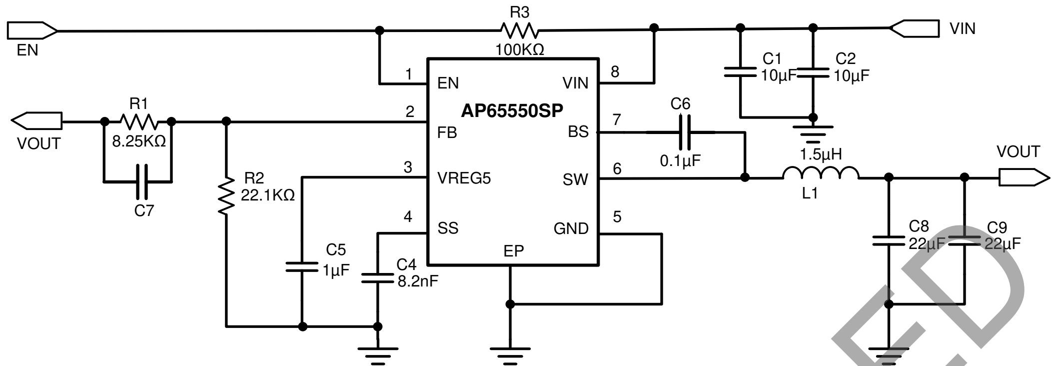


Figure 3 Typical Application of AP65550SP (SO-8EP) Evaluation Board

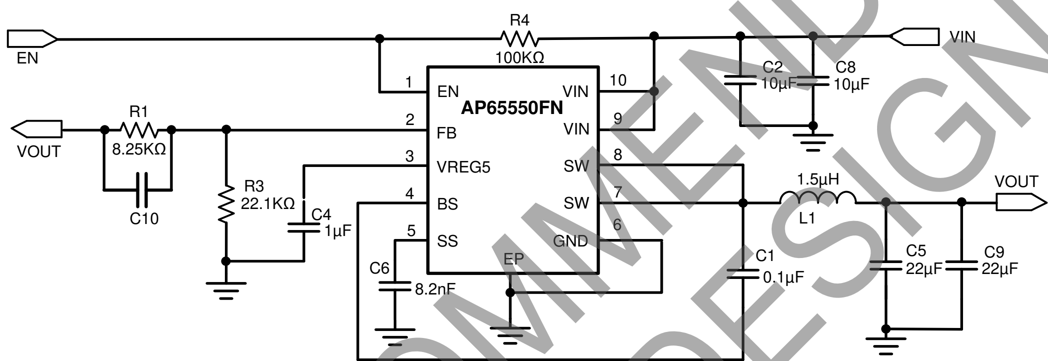


Figure 4 Typical Application of AP65550FN (U-DFN3030-10) Evaluation Board

PWM Operation and Adaptive On-time Control

The AP65550 is a synchronous step-down converter with internal power MOSFETs. Adaptive constant on-time (aCOT) control is employed to provide fast, transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot timer, ON-time period. This one shot is calculated by the converter's input voltage (V_{IN}) and the output voltage (V_{OUT}) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET turned off after the fixed on time expire and turn on the low-side MOSFET. Once the output voltage dropped below the output regulation, the low-side turned off. The one-shot timer then reset and the high-side MOSFET is turned on again.

AP65550 uses an adaptive on-time control scheme and does not have a dedicated in-board oscillator. It runs with a pseudo-constant frequency of 650kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S}$$

V_{OUT} is the output voltage
V_{IN} is the input voltage
f_S is the switching frequency

After an ON-time period, the AP65550 goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.765V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is about 260ns typical.

Application Information (continued)

Power Save Mode

The AP65550 is designed with Power Save Mode (PSM) at light load conditions for high efficiency. The AP65550 automatically reduces the switching frequency and changes the Ton time to Tmin-on time during a light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.765V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing V_{OUT} ripple at light load condition. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON}$$

T_{ON} is on-time

Enable

Above the 'EN high-level input voltage', the internal regulator is turned on and the quiescent current can be measured above this threshold. The enable (EN) input allows the user to control turning on or off the regulator. To enable the AP65550, EN must be pulled above the 'EN high-level input voltage.' To disable the AP65550, EN must be pulled below 'EN low-level input voltage.'

In Figures 3 and 4, EN has a positive voltage through a 100KΩ pull-up to VIN.

Soft-Start

The soft-start time of the AP65355 is programmable by selecting different C_{SS} values. When the EN pin becomes high, the C_{SS} is charged by a current source, generating a ramp signal fed into non-inverting input of the error comparator. Reference voltage V_{REF}, or the internal soft-start voltage SS, (whichever is smaller), dominates the behavior of the non-inverting inputs of the error amplifier. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The capacitor value required for a given soft-start ramp time can be expressed as:

$$t_{SS} = 63 \times 10^3 \times C_{SS}$$

Where C_{SS} is the required capacitor between SS pin and PGND and t_{SS} is the desired soft-start time.

Overcurrent Protection (OCP)

Figure 5 shows the overcurrent protection (OCP) scheme of AP65550. In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between PGND pin and SW pin is lower than the overcurrent trip level, V_{LIMIT}, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin when the measured voltage is higher than limit voltage. After 6µs, the internal OCL (Over Current Logic) threshold is set to a lower level and SS pin is discharged such that output is 0V. Then the switching action is blanked out for one t_{SS} before soft start re-initiated and OCP threshold is restored to higher value.

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, V_{LIMIT} has 4ppm/°C temperature coefficient to compensate this temperature dependency of $R_{DS(ON)}$.

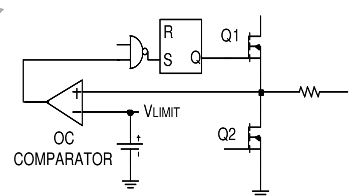


Figure 5 Overcurrent Protection Scheme

Application Information (continued)

Undervoltage Lockout

The AP65550 provides an undervoltage lockout circuit to prevent it from undefined status during startup. The UVLO circuit shuts down the device when V_{IN} drops below 3.45V. The UVLO circuit has 320mV hysteresis, which means the device starts up again when V_{REG} rises to 3.75V (non-latch).

Thermal shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP65550 shuts itself off, and both HS and LS MOSFETs will be turned off. The output is discharged with the internal transistor. When the junction cools to the required level (+130°C nominal), the device initiates soft-start as during a normal power-up cycle.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA})$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

T_A is the ambient temperature of the environment. The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

Setting the Output Voltage

The output voltage can be adjusted from 0.765 using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However the tradeoff is output voltage accuracy due to the bias current in the error amplifier. R1 can be determined by the following equation:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{0.765} - 1\right)$$

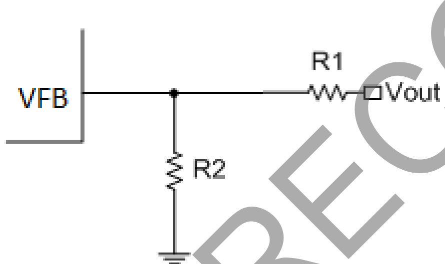


Figure 6 Feedback Divider Network

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)
1	6.81	22.1
1.05	8.25	22.1
1.2	12.7	22.1
1.5	21.5	22.1
1.8	30.1	22.1
2.5	49.9	22.1
3.3	73.2	22.1
5	124	22.1

Table 1 Resistor Selection for Common Output

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_S}$$

Where ΔI_L is the inductor ripple current and f_S is the switching frequency.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

Application Information (continued)

A 1µH to 3.3µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor's DC resistance should be less than 100mΩ. Use a larger inductance for improved efficiency under light load conditions.

The phase boost can be achieved by adding an additional feed forward capacitor (C7) parallel to R1.

Output Voltage (V)	C7(pF)	L1(µH)	C8+C9(µF)
1	—	1.0-1.5	22-68
1.05	—	1.0-1.5	22-68
1.2	—	1.0-1.5	22-68
1.5	—	1.5	22-68
1.8	5-22	1.5	22-68
2.5	5-22	2.2	22-68
3.3	5-22	2.2	22-68
5	5-22	3.3	22-68

Table 2 Recommended Component Selection

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMs rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used it must be surge protected, otherwise, capacitor failure could occur. For most applications greater than 10µF, ceramic capacitor is sufficient.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

Maximum capacitance required can be calculated from the following equation:
ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from the equation below:

$$V_{OUT\_RIPPLE} = \Delta I_{INDUCTOR} * ESR$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor will be sufficient.

$$C_O = \frac{L(I_{OUT} + \frac{\Delta I_{INDUCTOR}}{2})^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the VBST and SW pin. A 0.1µF ceramic capacitor is sufficient.

VREG5 Capacitor

To ensure the proper operation, a ceramic capacitor must be connected between the VREG5 and PGND pin. A 1µF ceramic capacitor is sufficient.

Application Information (continued)

PC Board Layout

1. The AP65550 works at 5A load current, heat dissipation is a major concern in layout the PCB. A 2oz Copper in both top and bottom layer is recommended.
2. Provide sufficient vias in the thermal exposed pad for heat dissipate to the bottom layer.
3. Provide sufficient vias in the Output capacitor PGND side to dissipate heat to the bottom layer.
4. Make the bottom layer under the device as PGND layer for heat dissipation. The PGND layer should be as large as possible to provide better thermal effect.
5. Make the Vin capacitors as close to the device as possible.
6. Make the VREG5 capacitor as close to the device as possible.
7. The thermal pad of the device should be soldered directly to the PCB exposed copper plane to work as a heatsink. The thermal vias in the exposed copper plane increase the heat transfer to the bottom layer.

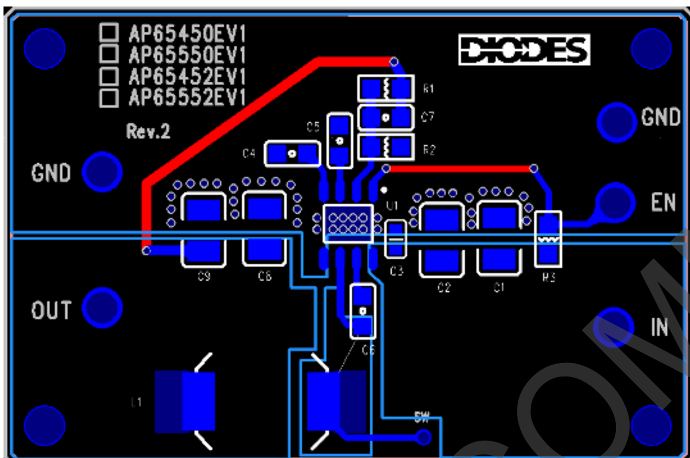


Figure 7 PC Board Layout for SO-8EP

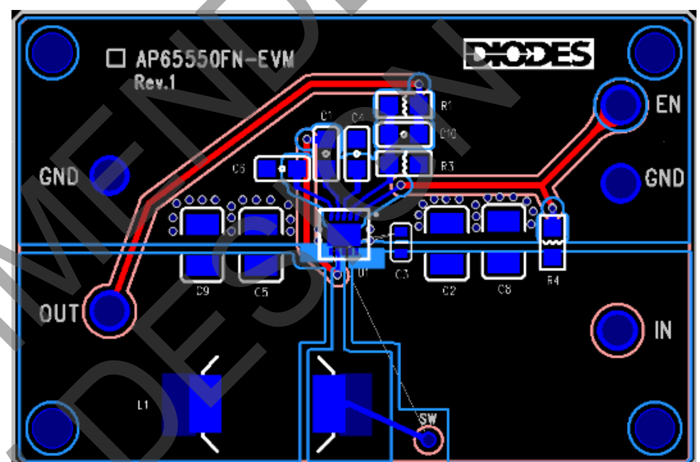
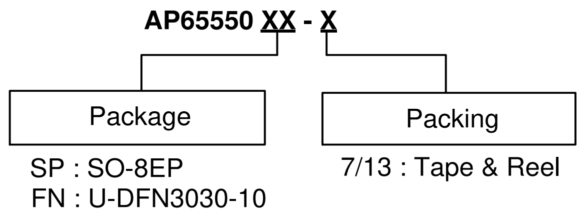


Figure 8 PC Board Layout for U-DFN3030-10

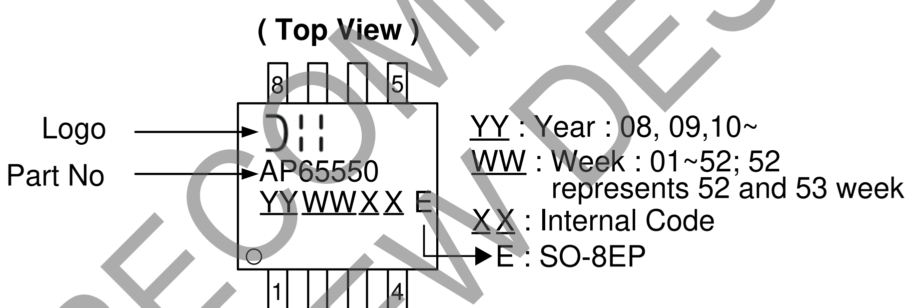
Ordering Information



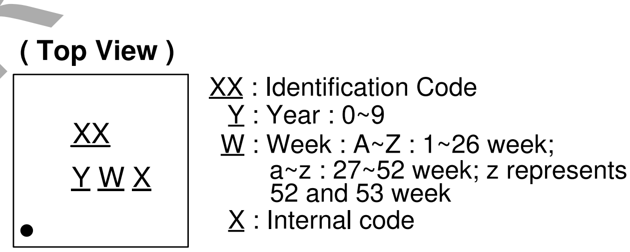
Part Number	Package Code	Package	Tape and Reel	
			Quantity	Part Number Suffix
AP65550SP-13	SP	SO-8EP	2,500	-13
AP65550FN-7	FN	U-DFN3030-10	3,000	-7

Marking Information

SO-8EP



U-DFN3030-10

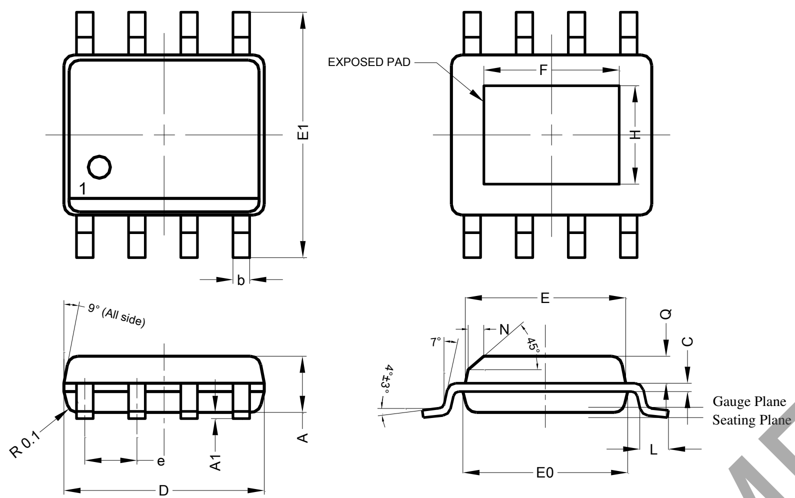


Part Number	Package	Identification Code
AP65550FN-7	U-DFN3030-10	TJ

Package Outline Dimensions

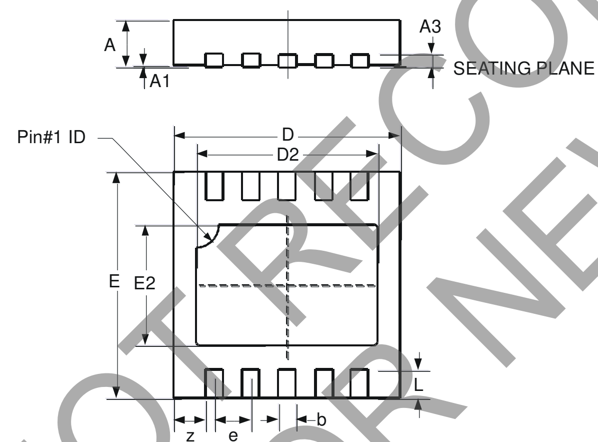
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8EP



SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

(2) Package Type: U-DFN3030-10

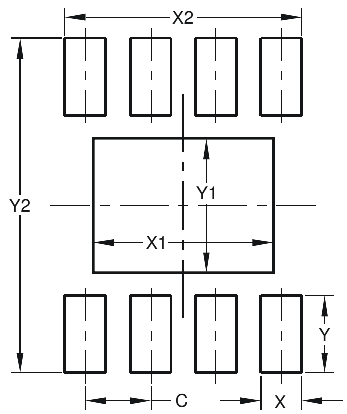


U-DFN3030-10			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
e	—	—	0.50
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

Suggested Pad Layout

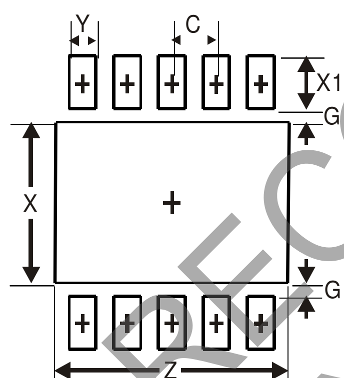
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SO-8EP



Dimensions	Value(in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

(2) Package Type: U-DFN3030-10



Dimensions	Value (in mm)
Z	2.60
G	0.15
X	1.80
X1	0.60
Y	0.30
C	0.50

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com