





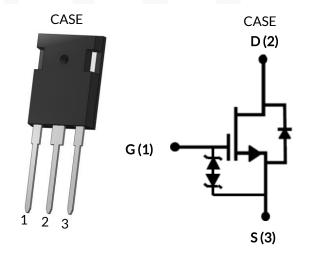








UJ4C075060K3S



Part Number	Package	Marking
UJ4C075060K3S	TO-247-3L	UJ4C075060K3S









750V-58m Ω SiC FET

Rev. A, October 2020

Description

The UJ4C075060K3S is a 750V, $58m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: $58m\Omega$ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 52nC
- ◆ Low body diode V_{FSD}: 1.31V
- ◆ Low gate charge: Q_G = 37.8nC
- ◆ Threshold voltage V_{G(th)}: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
Continuous drain current ¹		T _C = 25°C	28	Α
Continuous drain current	I _D	T _C = 100°C	20.6	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	62	Α
Single pulsed avalanche energy ³	E _{AS}	L=15mH, I _{AS} =1.8A	24.3	mJ
Power dissipation	P _{tot}	T _C = 25°C	155	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T _L		250	°C

- 1. Limited by $T_{J,max}$
- 2. Pulse width t_p limited by T_{J,max}
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Doromotor	Symbol	Test Conditions		Value		Units
Parameter	Symbol	rest Conditions	Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.75	0.97	°C/W













Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Units		
Parameter	Зуппон	Test Conditions	Min	Тур	Max	Offics
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_D =1mA	750			V
Total drain lankage current		V_{DS} =750V, V_{GS} =0V, T_{J} =25°C		0.7	40	^
Total drain leakage current	I _{DSS} V _G	V _{DS} =750V, V _{GS} =0V, T _J =175°C		15		μΑ
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		4.7	± 20	μΑ
		V_{GS} =12V, I_{D} =20A, T_{J} =25°C		58	74	
Drain-source on-resistance	R _{DS(on)}	V _{GS} =12V, I _D =20A, T _J =125°C		106		mΩ
		V _{GS} =12V, I _D =20A, T _J =175°C		147		
Gate threshold voltage	$V_{G(th)}$	V_{DS} =5V, I_{D} =10mA	4	4.8	6	V
Gate resistance	R_{G}	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Value		Units
Parameter	Syllibol	Test Conditions	Min	1.31 1.8 52 16 58	Max	Offics
Diode continuous forward current ¹	I _S	T _C =25°C			28	Α
Diode pulse current ²	I _{S,pulse}	T _C =25°C			62	А
Forward voltage	V_{FSD}	V _{GS} =0V, I _F =10A, T _J =25°C		1.31	1.75	V
1 of ward voltage	* F3D	V _{GS} =0V, I _F =10A, T _J =175°C		1.8		
Reverse recovery charge	Q _{rr}	V_R =400V, I_F =20A, V_{GS} =0V, R_{G_EXT} =20 Ω		52		nC
Reverse recovery time	t _{rr}	di/dt=1060A/μs, Τ _J =25°C		16		ns
Reverse recovery charge	Q _{rr}	V_R =400V, I_F =20A, V_{GS} =0V, R_{G_EXT} =20 Ω		58		nC
Reverse recovery time	t _{rr}	di/dt=1060A/μs, Τ _J =150°C		19		ns













Typical Performance - Dynamic

Parameter	Comple al	Test Conditions		Units		
Pai ailletei	Symbol		Min	Тур	Max	Units
Input capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V		1422		
Output capacitance	C _{oss}	f=100kHz		68		pF
Reverse transfer capacitance	C_{rss}	1-100KHZ		2.7		
Effective output capacitance, energy related	C _{oss(er)}	V_{DS} =0V to 400V, V_{GS} =0V		50		pF
Effective output capacitance, time related	C _{oss(tr)}	V_{DS} =0V to 400V, V_{GS} =0V		94		pF
C _{OSS} stored energy	E _{oss}	V _{DS} =400V, V _{GS} =0V		4		μJ
Total gate charge	Q_G	V _{DS} =400V, I _D =20A		37.8		nC
Gate-drain charge	Q_{GD}			8		
Gate-source charge	Q_{GS}	$V_{DS}=400V, I_D=20A,$ $V_{GS}=0V \text{ to } 15V$ $Note 4,$ $V_{DS}=400V, I_D=20A, Gate$ $Driver = 0V \text{ to } +15V,$ $Turn-on R_{G,EXT}=1\Omega,$		11.8		
Turn-on delay time	t _{d(on)}	Note 4,		13		_
Rise time	t _r			29		
Turn-off delay time	t _{d(off)}	$V_{GS} = 0V \text{ to } 15V$ $Note 4,$ $V_{DS} = 400V, I_D = 20A, Gate$ $Driver = 0V \text{ to } +15V,$ $Turn-on R_{G,EXT} = 1\Omega,$ $Turn-off R_{G,EXT} = 20\Omega$ $Inductive Load,$ $FWD: same device with$		78		ns
Fall time	t _f	-,		13		
Turn-on energy	E _{ON}	,		168		
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$		58		μJ
Total switching energy	E _{TOTAL}	T _J =25°C		226		
Turn-on delay time	t _{d(on)}	Note 4,		13		
Rise time	t _r	V _{DS} =400V, I _D =20A, Gate		31		
Turn-off delay time	t _{d(off)}	Driver =0V to +15V, Turn-on $R_{G,EXT}$ =1 Ω ,		84		ns
Fall time	t _f	Turn-off $R_{G,EXT}$ =20 Ω		14		
Turn-on energy	E _{ON}	Inductive Load, FWD: same device with		189		
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$		70		μJ
Total switching energy	E _{TOTAL}	T _J =150°C		259		

^{4.} Measured with the half-bridge mode switching test circuit in Figure 28.













Typical Performance - Dynamic (continued)

Turn-on delay time t _{d(on)} Turn-on energy including R _s energy E _{ON} Turn-on energy including R _s energy E _{ON} Turn-on delay time t _{d(on)}	Doromotor	Cymahal	Tast Conditions Value			l lmita	
Note 5, Note 6, Not	Parameter	Symbol	lest Conditions –	Min Typ Max			Units
Turn-off delay time $t_{d(off)}$ $V_{DS} = 400V, I_0 = 20A, Gate Driver = 0V to +15V, Reserved from the standard from $	Turn-on delay time	t _{d(on)}			13		
Turn-off delay time	Rise time	t _r	-		31		
Fall time	Turn-off delay time	t _{d(off)}			31		1115
Turn-off energy including R_S energy E_{OFF} and $C_{SI}=000$ and $R_G=1\Omega$, RC shubber $R_S=100$ and $R_G=1\Omega$, R	Fall time				9		
Total switching energy E_{OFF} E_{TOTAL} $E_{RS_{S}ON}$ E_{R	Turn-on energy including R_S energy	E _{ON}			186		
Total switching energy E TOTAL Shoulder R_{S} energy during turn-on E RS_{SON} ERS_{SON} CS_1=95pF, T_2=25°C 204 μJ Snubber R_{S} energy during turn-off ERS_{SOF} 0.9 13 Turn-on delay time t_{clon} 13 Note 5, V_{DS}=400V, I_{D}=20A, Gate Driver = 0V to +15V, R_{CRSF}=10. inductive Load, The Unit of the	Turn-off energy including R_S energy	E _{OFF}			18		
Solubber R _S energy during turn-off ERS_OFF CRS_OFF CRS_	Total switching energy	E _{TOTAL}			204		μJ
Turn-on delay time $t_{d(on)}$ Note 5, Vos=400V, I _D =20A, Gate Driver = 0V to ±15V, R _{G,EXT} =1Ω, inductive Load, Post of the string of the	Snubber R _S energy during turn-on	E _{RS_ON}	T _J =25°C		0.5		
Rise time	Snubber R _S energy during turn-off	E _{RS_OFF}			0.9		
Turn-off delay time $t_{d(off)}$ $V_{DS}=400V, I_{D}=20A, Gate Driver = 0V to +15V, R_{G,EXT}=1Ω, inductive Load, Ext=1Ω and R_{G}=1Ω, RC Subber R_{S} energy during turn-on ER_{S,ON} Same device with V to 10 same device with V to 10 subber R_{S} energy during turn-on ER_{S,ON} Shubber R_{S} energy during turn-off ER_{S,OFF} $	Turn-on delay time	t _{d(on)}			13		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Rise time	t _r	Note 5,		35]
Fall time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-off delay time	t _{d(off)}			34		ns
Turn-on energy including R_S energy E_{OR} E_{OFF}	Fall time				10		
Total switching energy E_{OFF} E_{TOTAL} E_{TOTAL} $E_{RS_1} = 10\Omega$ and $E_{RS_2} = 10$	Turn-on energy including R _S energy	E _{ON}	99		210		
Total switching energy E_{TOTAL} $C_{S1}=95pF$, $T_{J}=150^{\circ}C$ 0.5 $0.$	Turn-off energy including R _S energy	E _{OFF}	_		24		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Total switching energy	E _{TOTAL}			234		μJ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Snubber R _S energy during turn-on		T _J =150°C		0.5		
Rise time t_r Note 6, V _{DS} =400V, I _D =20A, Gate Driver = 0V to +15V, Turn-onf delay time 26 ns Fall time t_f Turn-on R _{G,EXT} =1Ω, Turn-on R _{G,EXT} =20Ω Inductive Load, FWD: UJ3D06510TS Tr=25°C 12 12 Turn-off energy E_{OFF} FWD: UJ3D06510TS Tr=25°C 56 μJ Turn-on delay time $t_{d(on)}$ Note 6, V _{DS} =400V, I _D =20A, Gate Driver = 0V to +15V, Turn-onf delay time 30 ns Turn-off delay time t_f Turn-onf R _{G,EXT} =1Ω, Turn-onf R _{G,EXT} =1Ω, Turn-onf R _{G,EXT} =1Ω, Turn-onf R _{G,EXT} =1Ω, Turn-onf R _{G,EXT} =20Ω Inductive Load, FWD: UJ3D06510TS Turn-onf R _{G,EXT} =20Ω Inductive Load, F	Snubber R _S energy during turn-off				0.9		
Rise time t_r V _{DS} =400V, I _D =20A, Gate 26 ns Turn-off delay time $t_{d(off)}$ Driver = 0V to +15V, Turn-on R _{GEXT} =1Ω, Turn-on R _{GEXT} =2ΩΩ Inductive Load, FWD: UJ3D06510TS 12 12 Turn-off energy E_{ON} Inductive Load, FWD: UJ3D06510TS 56 μJ Total switching energy E_{TOTAL} Note 6, VDS=400V, I _D =20A, Gate 13 VDS=400V, I _D =20A, Gate 30 Note 6, VDS=400V, I _D =20A, Gate 30 Note 6, VDS=400V, I _D =20A, Gate 15 Turn-on R _{GEXT} =1Ω, Turn-on R _{GEXT} =1Ω, Turn-on R _{GEXT} =1Ω, Turn-on R _{GEXT} =1Ω, Turn-on R _{GEXT} =20Ω Inductive Load, FWD: UJ3D06510TS 15 Turn-on R _{GEXT} =20Ω Inductive Load, FWD: UJ3D06510TS 162 Turn-on R _{GEXT} =20Ω Inductive Load, FWD: UJ3D06510TS 70 μJ	Turn-on delay time	t _{d(on)}	Note 6		13		
Turn-off delay time $t_{d(off)} = 0 \text{V to } +15 \text{V}, \\ Turn-off R_{G,EXT} = 1 \Omega, \\ Turn-off energy \\ Turn-of delay time t_{d(on)} = t_{d(on)} \\ Turn-off delay time \\ Turn-off delay time \\ Turn-off delay time \\ Turn-off energy \\ Turn-off R_{G,EXT} = 20 \Omega, \\ Turn-off R_{G,EXT} = 1 \Omega, \\ Turn-off R_{G,EXT} = 20 \Omega, \\ Turn-off R_{G,EXT} =$	Rise time				26		
Fall time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-off delay time	t _{d(off)}			78		ns
Turn-on energy E_{ON} Inductive Load, $FWD: UJ3D06510TS$ E_{OFF} Total switching energy E_{OFF} E_{TOTAL}	Fall time				12		
Turn-off energy E_{OFF} FWD: UJ3D06510TS T_J =25°C 198 198 198 198 198 198 198 198 198 198	Turn-on energy	E _{ON}			142		
Total switching energy E_{TOTAL} $T_J=25^{\circ}C$ 198 Turn-on delay time $t_{d(on)}$ Note 6, $V_{DS}=400V, I_D=20A, Gate$ 30 Turn-off delay time $t_{d(off)}$ Driver =0V to +15V, T_{UTN} -on energy E_{ON} Inductive Load, T_{UTN} -off energy E_{OFF} FWD:UJ3D06510TS $T_{UTN}=150^{\circ}C$	Turn-off energy	E _{OFF}			56		μJ
Rise time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Total switching energy		T _J =25°C		198		
Rise time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-on delay time	t _{d(on)}	Note 6		13		
Turn-off delay time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Rise time	t _r			30		
Turn-off R _{G,EXT} = 20Ω 15 Turn-off energy E_{ON} Inductive Load, T_{OFF} Turn-off energy T_{OFF} T_{OF	Turn-off delay time	t _{d(off)}	Driver =0V to +15V,		83		ns
Turn-on energy E_{ON} Inductive Load, 162 Turn-off energy E_{OFF} FWD:UJ3D06510TS 70 μ J	Fall time	t _f	/		15		
Turn-off energy E_{OFF} FWD:UJ3D06510TS 70 μ J	Turn-on energy	E _{ON}	- /		162		
T.=150°C	Turn-off energy	E _{OFF}			70		μJ
	Total switching energy		T _J =150°C		232		

^{5.} Measured with the chopper mode switching test circuit in Figure 30.

^{6.} Measured with the chopper mode switching test circuit in Figure 29.





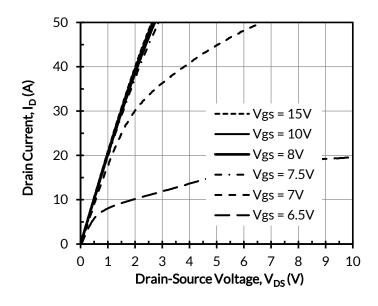








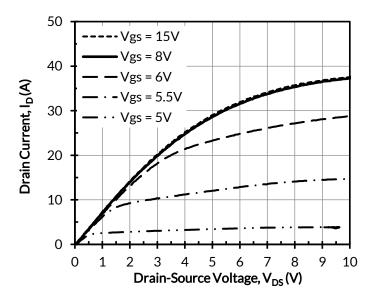
Typical Performance Diagrams



50 40 Drain Current, I_D (A) 30 Vgs = 15V 20 Vgs = 8V Vgs = 7V10 Vgs = 6.5V • Vgs = 6V 0 0 1 2 3 10 Drain-Source Voltage, V_{DS} (V)

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, $tp < 250\mu s$



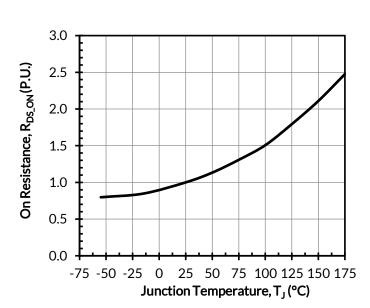


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 20A



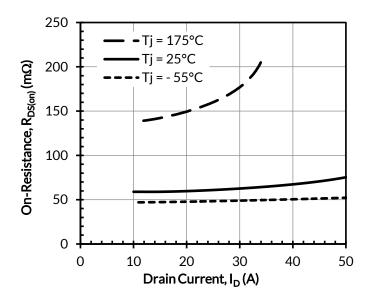












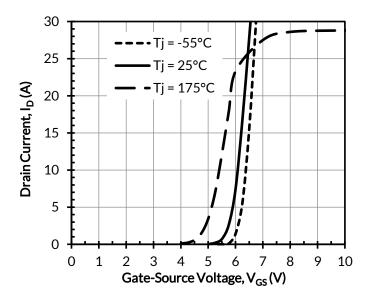
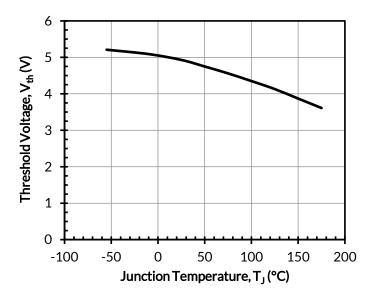


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V



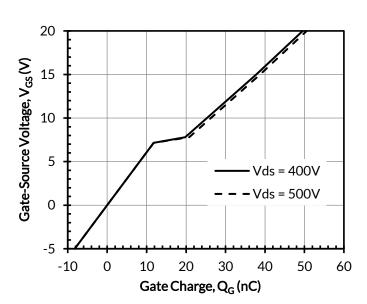


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at $I_D = 20A$













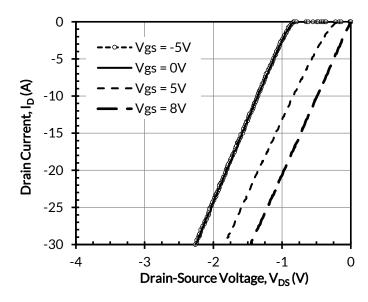


Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

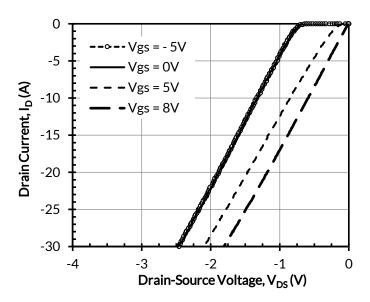


Figure 10. 3rd quadrant characteristics at T_J = 25°C

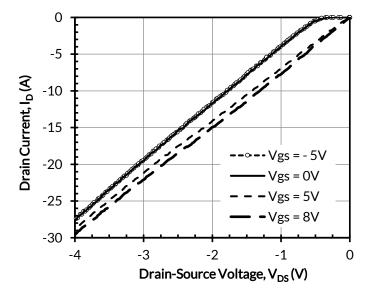


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

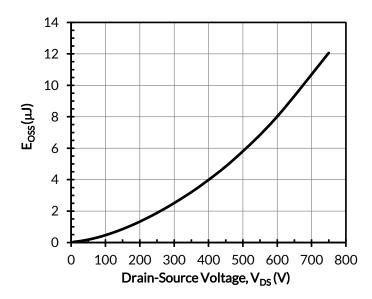


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$



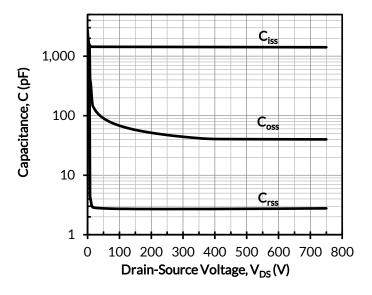








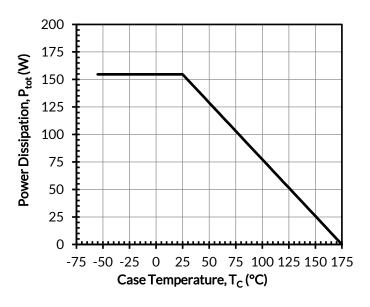




35 30 25 20 15 10 5 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T_C (°C)

Figure 13. Typical capacitances at f = 100kHz and $V_{GS} = 0V$

Figure 14. DC drain current derating



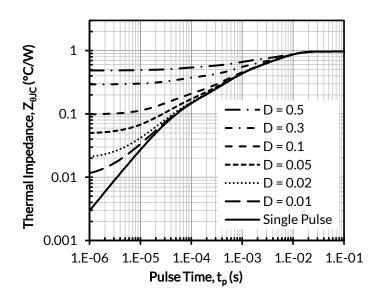


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













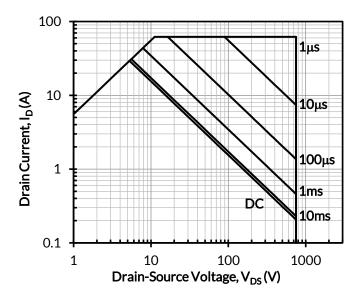


Figure 17. Safe operation area at $T_C = 25$ °C, D = 0, Parameter t_p

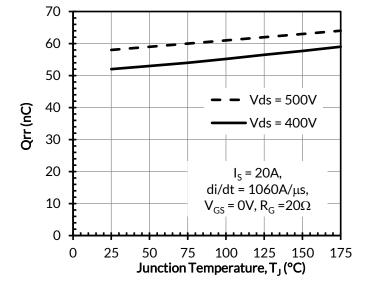


Figure 18. Reverse recovery charge Qrr vs. junction temperature

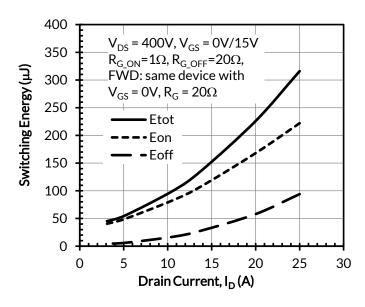


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

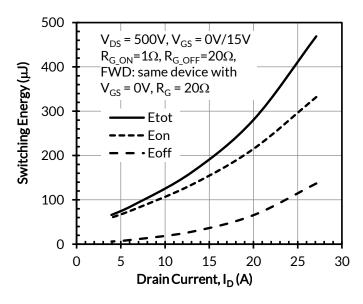


Figure 20. Clamped inductive switching energy vs. drain current at V_{DS} = 500V and T_J = 25°C



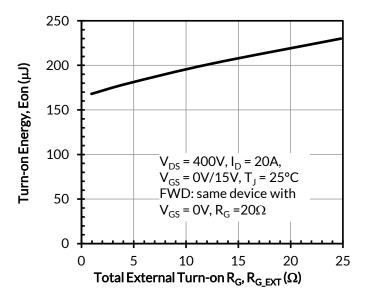








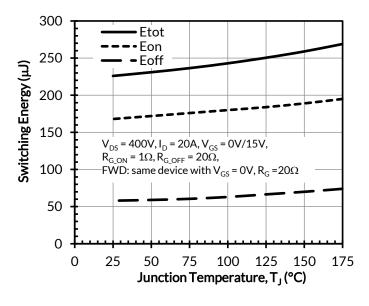




200 Turn-Off Energy, Eoff (إلىا) 150 100 $V_{DS} = 400V, I_{D} = 20A,$ $V_{GS} = 0V/15V, T_J = 25^{\circ}C$ 50 FWD: same device with $V_{GS} = 0V, R_G = 20\Omega$ 0 0 20 40 60 80 100 Total External Turn-off R_{G} , $R_{G,EXT}(\Omega)$

Figure 21. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

Figure 22. Clamped inductive switching turn-off energy vs. $R_{\text{G,EXT_OFF}}$



350 300 Switching Energy (µJ) 250 200 Eon Eoff 150 $V_{DS} = 500V, I_{D} = 20A, V_{GS} = 0V/15V$ $R_{G ON} = 1\Omega, R_{G OFF} = 20\Omega,$ 100 FWD: same device with V_{GS} 50 0 25 75 125 0 50 100 150 175 Junction Temperature, T₁ (°C)

Figure 23. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D = 20A

Figure 24. Clamped inductive switching energy vs. junction temperature at V_{DS} = 500V and I_D = 20A



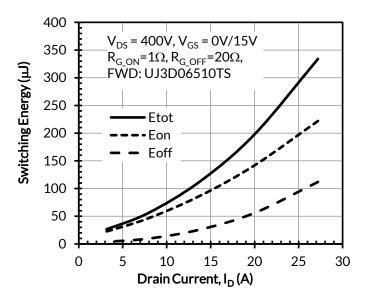








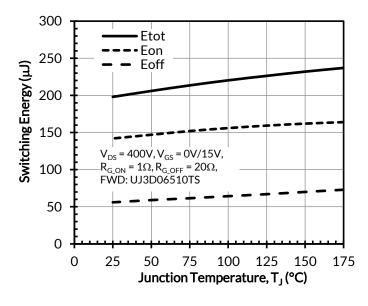




 $V_{DS} = 500V, V_{GS} = 0V/15V$ $R_{G_ON}=1\Omega$, $R_{G_OFF}=20\Omega$, FWD: UJ3D06510TS Switching Energy (µJ) Etot **Eoff** Drain Current, ID (A)

Figure 24. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

Figure 25. Clamped inductive switching energy vs. drain current at $V_{DS} = 500V$ and $T_J = 25^{\circ}C$



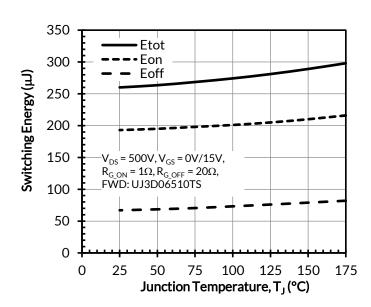


Figure 26. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_{D} = 20A

Figure 27. Clamped inductive switching energy vs. junction temperature at V_{DS} = 500V and I_D = 20A













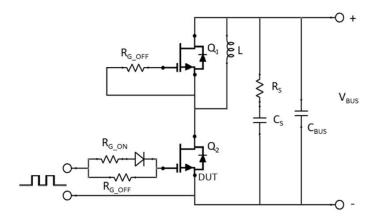


Figure 28. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_S = 2.5Ω , C_S=100nF) is used to reduce the power loop high frequency oscillations.

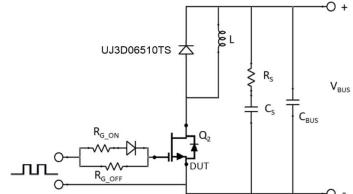


Figure 29. Schematic of the chopper mode switching test circuit. Note, a bus RC snubber (R_S = 2.5 Ω , C_S =100nF) is used to reduce the power loop high frequency oscillations.

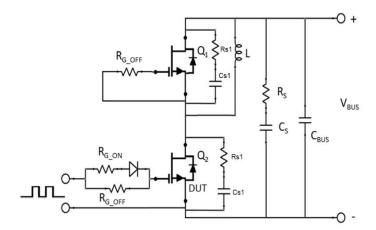


Figure 30. Schematic of the half-bridge mode switching test circuit with device RC snubbers (R_{s1} = 10 Ω , C_{s1} = 95pF) and a bus RC snubber (R_{S} = 2.5 Ω , C_{S} =100nF).













Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Disclaimer

UnitedSiC reserves the right to change or modify any of the products and their inherent physical and technical specifications without prior notice. UnitedSiC assumes no responsibility or liability for any errors or inaccuracies within.

Information on all products and contained herein is intended for description only. No license, express or implied, to any intellectual property rights is granted within this document.

UnitedSiC assumes no liability whatsoever relating to the choice, selection or use of the UnitedSiC products and services described herein.