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April 1st, 2010 Renesas Electronics Corporation

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Renesas

MOS FIELD EFFECT TRANSISTOR 2SK3225

SWITCHING N-CHANNEL POWER MOS FET

ORDERING INFORMATION DESCRIPTION The 2SK3225 is N-Channel MOS Field Effect Transistors PART NUMBER PACKAGE designed for high current switching applications. 2SK3225 TO-251 (MP-3) TO-252 (MP-3Z) **FEATURES** 2SK3225-Z edprodi · Low on-state resistance $R_{DS(on)1} = 18 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 17 \text{ A})$ $R_{DS(on)2} = 27 \text{ m}\Omega \text{ MAX.}$ (Vgs = 4.0 V, Ip = 17 A) Low input capacitance Ciss = 2100 pF TYP. · Built-in gate protection diode TO-251/TO-252 package (TO-251) ABSOLUTE MAXIMUM RATINGS (TA = 25°C) Drain to Source Voltage VDSS V Gate to Source Voltage VGSS(AC) +20 V +20. -10 Gate to Source Voltage V VGSS(DC) Drain Current (DC) D(DC) ±34 A Drain Current (Pulse) Note1 D(pulse) ±136 Α (TO-252) Total Power Dissipation (Tc = 25°C) PT1 40 w Total Power Dissipation ($T_A = 25^{\circ}C$) PT2 1.0 W **Channel Temperature** 150 °C Tch Storage Temperature °C Tstg -55 to +150 Single Avalanche Current Note2 15 А AS Single Avalanche Energy Note2 Eas 22 mJ

Note1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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 Printed in Japan
 The mark <R> shows major revised points.

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The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

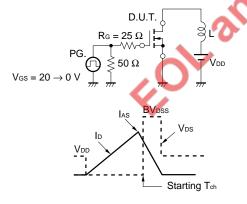
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 17 A	13	27		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 17 A		13	18	mΩ
	RDS(on)2	V _{GS} = 4.0 V, I _D = 17 A		18	27	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		2100		pF
Output Capacitance	Coss	V _{GS} = 0 V		550		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		220		pF
Turn-on Delay Time	t _{d(on)}	I _D = 17 A		32		ns
Rise Time	tr	V _{GS} = 10 V		300		ns
Turn-off Delay Time	t _{d(off)}	VDD = 30 V	く	110		ns
Fall Time	tr	R _G = 10 Ω		140		ns
Total Gate Charge	QG	ID = 34 A		45		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		7		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		13		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 34 A, VGS = 0 V		0.94		V
Reverse Recovery Time	trr	If = 34 A, V _{GS} = 0 V		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		95		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

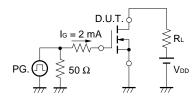
TEST CIRCUIT 2 SWITCHING TIME



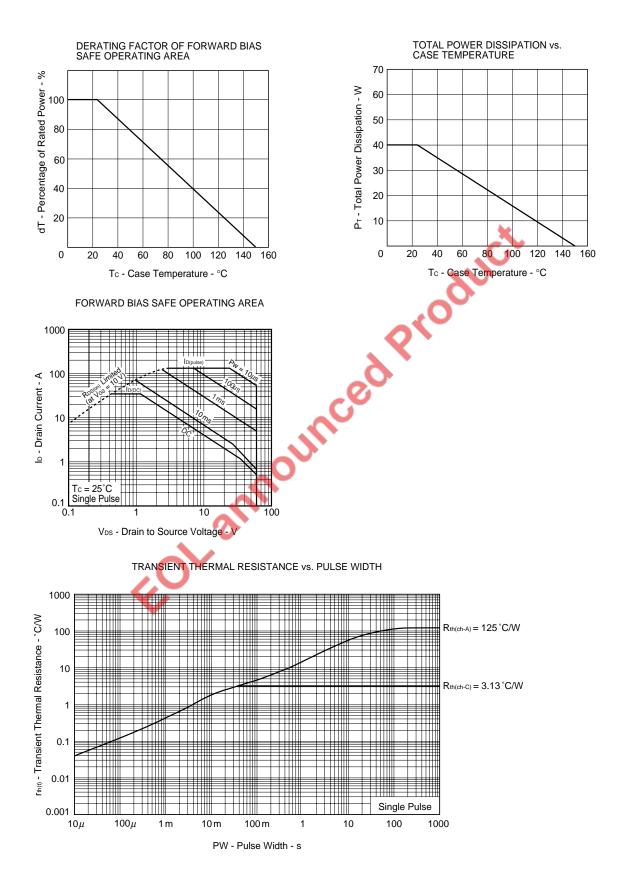
$PG. \bigcirc R_{G}$ V_{GS} $\tau = 1 \mu S$ Duty Cycle $\leq 1\%$

VGS Wave Form	V _{GS} 0 <u>10% -</u>	VGS	90%
I⊳ Wave Form	ID 0 <u>10%</u> td(on) ►	90%	+90% + 10% t _f t _{off}

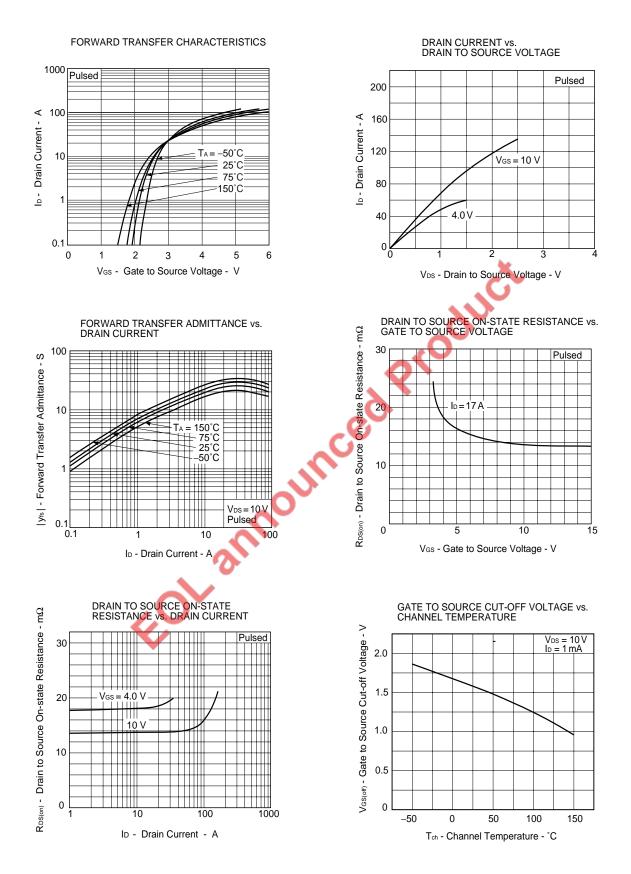
TEST CIRCUIT 3 GATE CHARGE

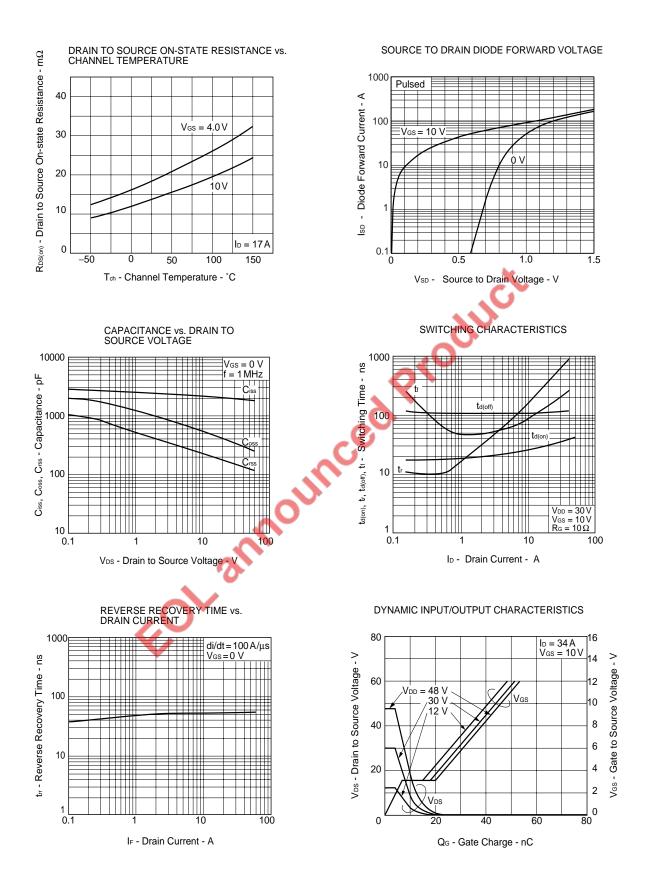


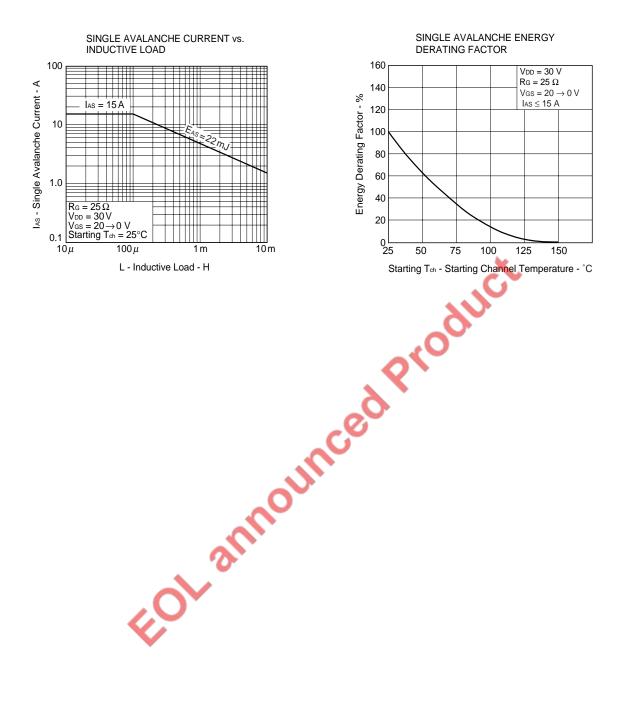
TYPICAL CHARACTERISTICS (TA = 25°C)



Data Sheet D13798EJ5V0DS



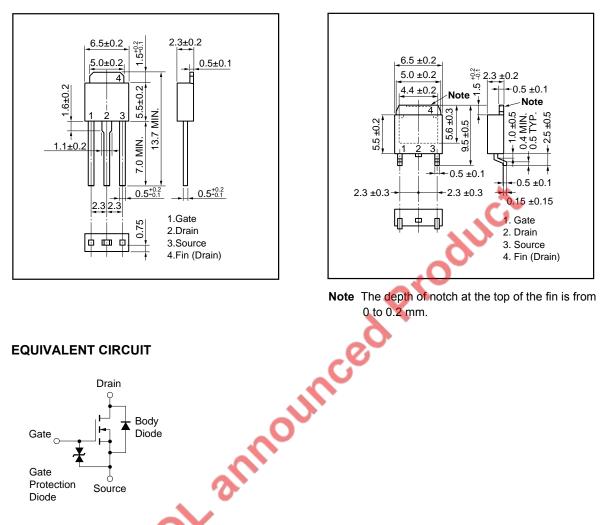




PACKAGE DRAWINGS (Unit : mm)

1)TO-251 (MP-3)

<R> 2)TO-252 (MP-3Z)



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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