CSD87313DMS 30-V Dual N-Channel NexFET™ Power MOSFETs

1 Features

- Low-Source-to-Source On Resistance
- Dual Common Drain N-Channel MOSFETs
- Optimized for 5-V Gate Drive
- Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

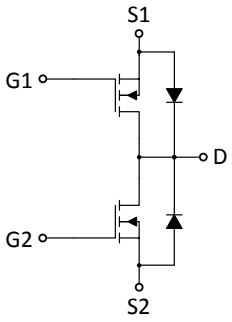
2 Applications

- USB Type-C™ and Power Delivery (PD) VBus Protection
- Battery Protection
- Load Switch

3 Description

The CSD87313DMS is a 30-V common drain, dual N-channel device designed for USB Type-C/PD and battery protection. This SON 3.3-mm × 3.3-mm device has low-source-to-source on resistance that minimizes losses and offers low-component count for space constrained applications.

Schematic



Product Summary

T_A = 25°C		VALUE		UNIT
V_{S1S2}	Source1-to-Source2 Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	28		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.0		nC
$R_{S1S2(on)}$	Max Source1-to-Source2 On Resistance	V_{GS} = 2.5 V	9.6	mΩ
		V_{GS} = 4.5 V	5.5	
$V_{GS(th)}$	Threshold Voltage	0.9		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD87313DMS	2500	13-Inch Reel	SON 3.30-mm × 3.30-mm Plastic Package	Tape and Reel
CSD87313DMST	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{S1S2}	Source1-to-Source2 Voltage	30	V
V_{GS}	Gate-to-Source Voltage(1)	±10	V
I_{S1S2}	Continuous Source Current(2)	17	A
I_{SM}	Pulsed Source Current, T_A = 25°C(2)(3)	120	A
P_D	Power Dissipation(2)	2.7	W
	Power Dissipation(4)	1	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse, I_D = 37 A, L = 0.1 mH, R_G = 25 Ω	67	mJ

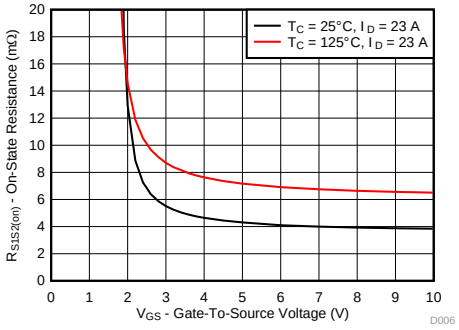
(1) V_{G1S1} should not exceed ±10 V and V_{G2S2} should not exceed ±10 V.

(2) Typical $R_{\theta JA}$ = 45°C/W when mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

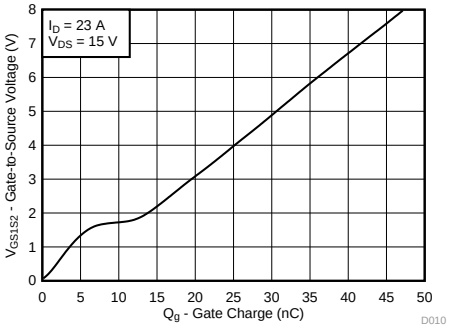
(3) Duty cycle ≤ 2%, pulse duration ≤ 300 µs.

(4) Typical $R_{\theta JA}$ = 125°C/W on a minimum 2-oz Cu pad.

$R_{S1S2(ON)}$ vs V_{GS}



Gate Charge



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4 Revision History

DATE	REVISION	NOTES
April 2017	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
I_{S1S2}	Source1-to-Source2 leakage current	V_{G1S1} = 0 V, V_{G2S2} = 0 V, V_{S1S2} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_{S1S2} = 250 µA	0.6	0.9	1.2	V
$R_{S1S2(on)}$	Source1-to-Source2 on resistance	V_{GS} = 2.5 V, I_{S1S2} = 20 A		6.7	9.6	mΩ
		V_{GS} = 4.5 V, I_{S1S2} = 23 A		4.6	5.5	
g_{fs}	Transconductance	V_{S1S2} = 3 V, I_{S1S2} = 23 A		149		S
DYNAMIC CHARACTERISTICS(1)						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 15 V, f = 1 MHz		3300	4290	pF
C_{OSS}	Output capacitance			281	365	pF
C_{RSS}	Reverse transfer capacitance			154	200	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 15 V, I_{S1S2} = 23 A V_{G1S1} = 4.5 V, V_{G2S2} = 0 V		28		nC
Q_{gd}	Gate charge gate-to-drain			6.0		nC
Q_{gs}	Gate charge gate-to-source			6.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			3.2		nC
$t_{d(on)}$	Turnon delay time	V_{S1S2} = 15 V, I_{S1S2} = 23 A V_{GS} = 4.5 V, R_{GEN} = 0 Ω		9		ns
t_r	Rise time			27		ns
$t_{d(off)}$	Turnoff delay time			41		ns
t_f	Fall time			13		ns
DIODE CHARACTERISTICS						
I_{fss}	Maximum continuous Source1-to-Source2 diode forward current(2)	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V			2	A
V_{fss}	Source1-to-Source2 diode forward voltage	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V, I_{fss} = 23 A		0.8	1.0	V

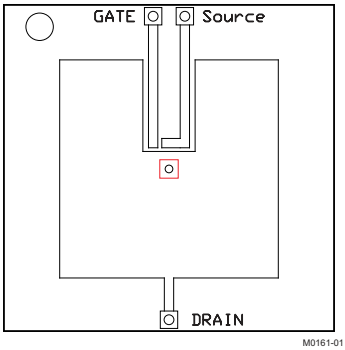
(1) Dynamic characteristic measurements are for a single FET.
(2) Typical $R_{\theta JA}$ = 125°C/W on a minimum 2-oz Cu pad.

5.2 Thermal Information

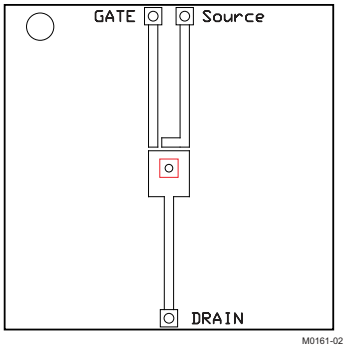
T_A = 25°C (unless otherwise stated)

THERMAL METRIC			UNIT
$R_{\theta JA}$	Junction-to-case thermal resistance(1)	125	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)	45	°C/W

(1) Device mounted on minimum 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



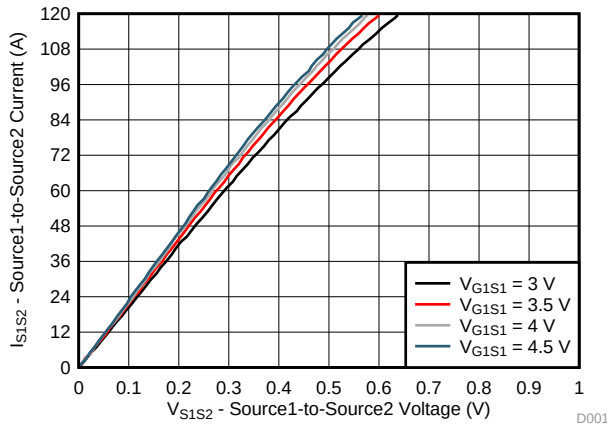
$R_{\theta JA}$ = 45°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



$R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

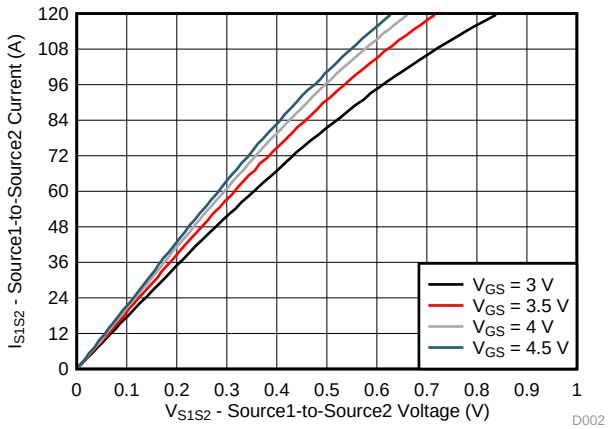
5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)



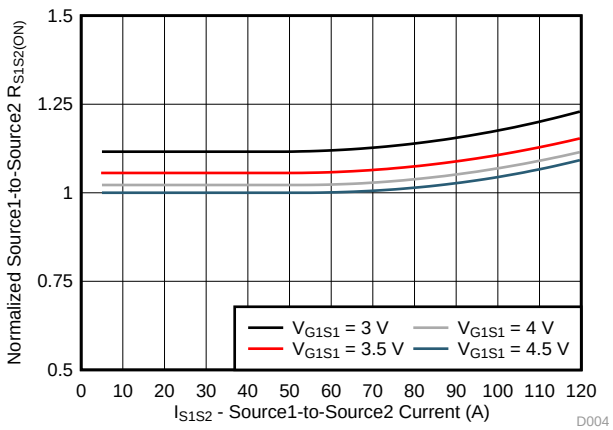
Pulse width = 250 µs, duty cycle = 0.5% V_{G2S2} = 4.5 V

Figure 1. Saturation Characteristics



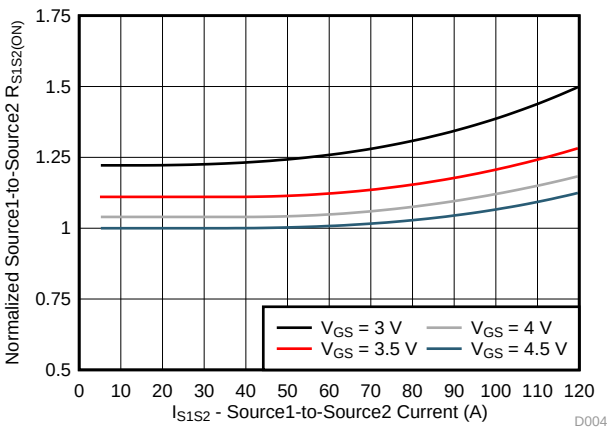
Pulse width = 250 µs, duty cycle = 0.5%

Figure 2. Saturation Characteristics



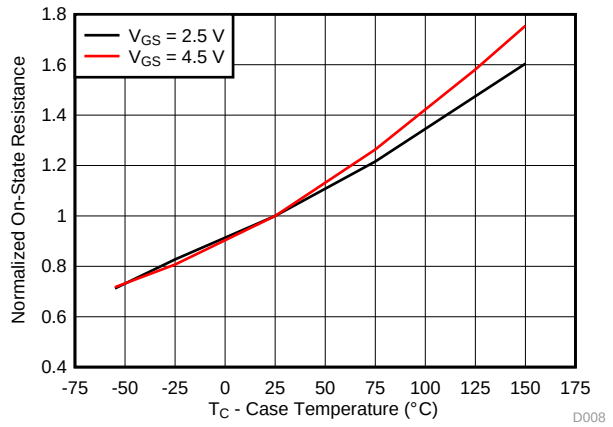
Pulse width = 250 µs, duty cycle = 0.5% V_{G2S2} = 4.5 V

Figure 3. Saturation Characteristics



Pulse width = 250 µs, duty cycle = 0.5%

Figure 4. Saturation Characteristics



I_{S1S2} = 23 A V_{GS} = 15 V

Figure 5. Normalized On-State Resistance vs Temperature

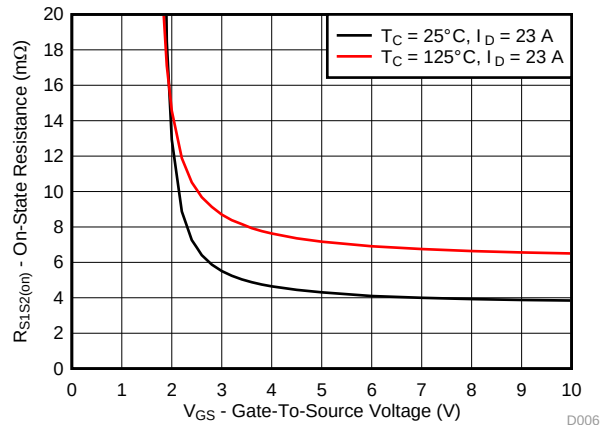


Figure 6. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

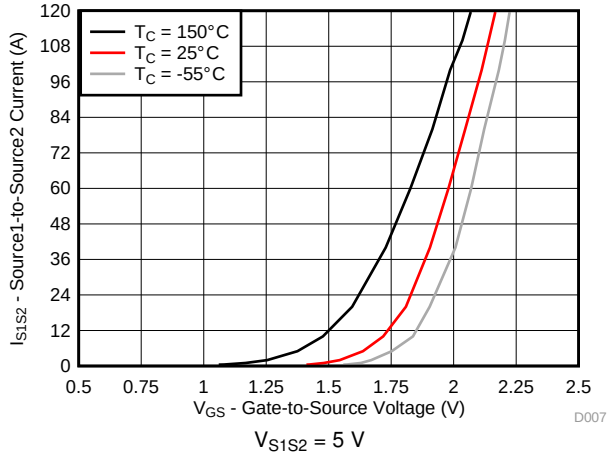


Figure 7. Transfer Characteristics

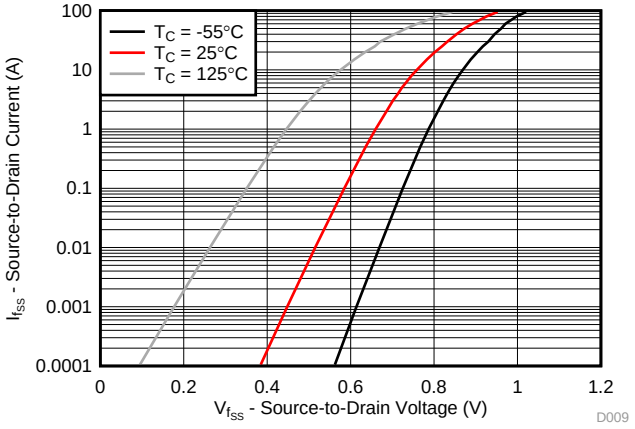


Figure 8. Typical Diode Forward Voltage

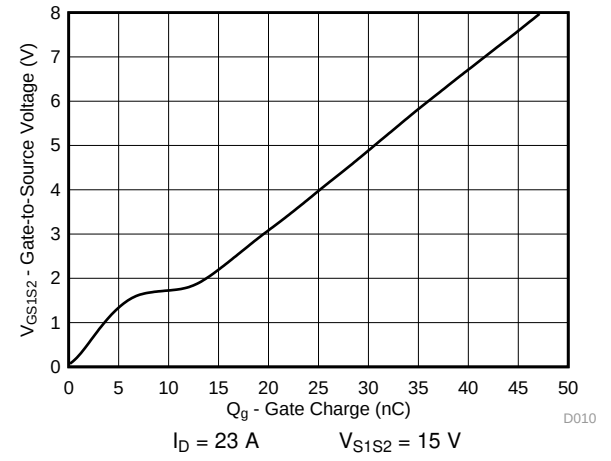


Figure 9. Gate Charge

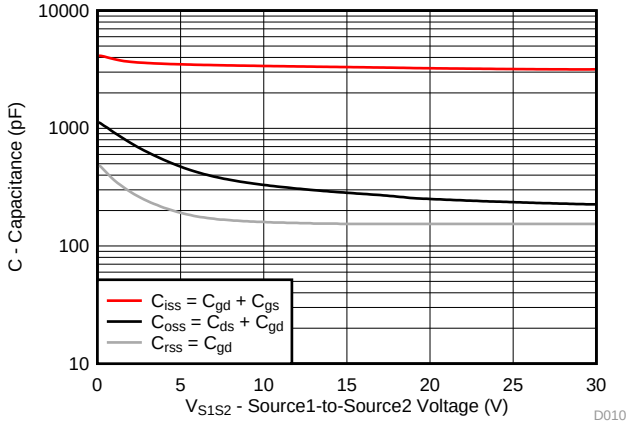


Figure 10. Capacitance

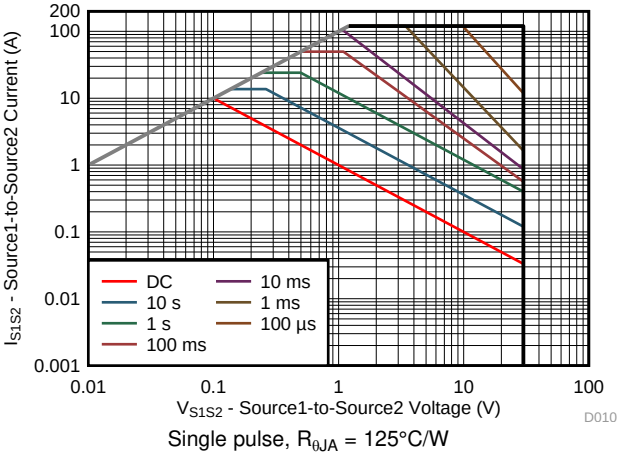


Figure 11. Maximum Safe Operating Area

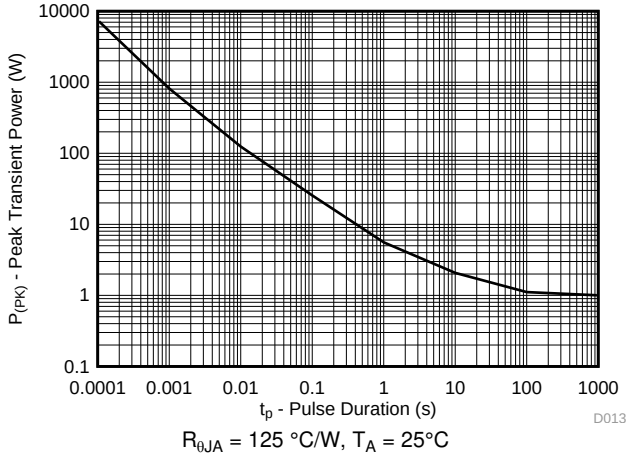


Figure 12. Single Pulse Maximum Power Dissipation

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

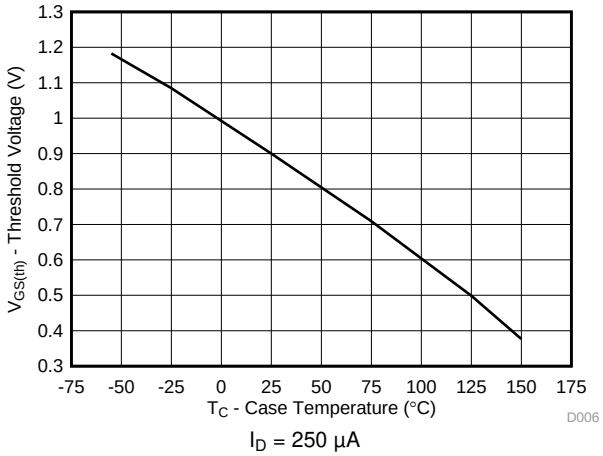


Figure 13. Threshold Voltage vs Temperature

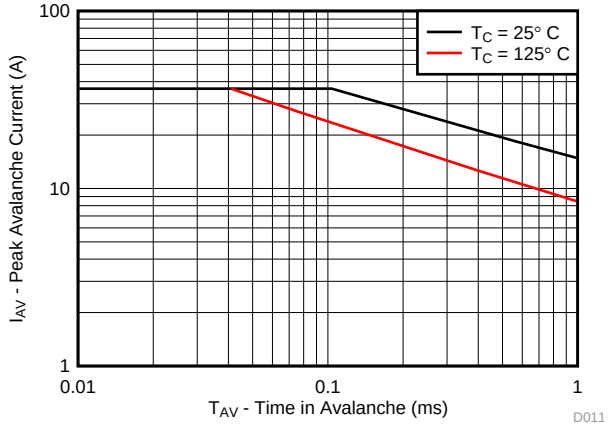


Figure 14. Single Pulse Unclamped Inductive Switching

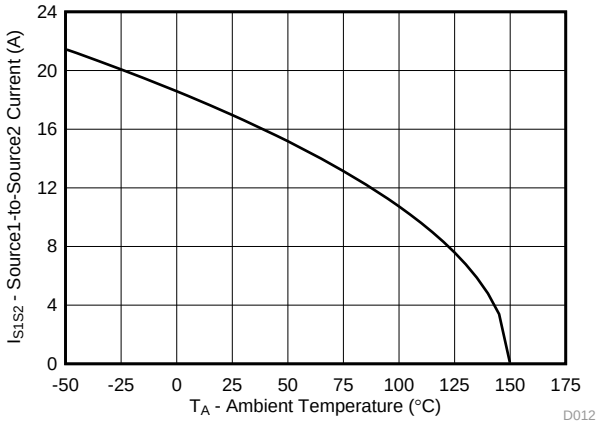


Figure 15. Maximum Source1-to-Source2 Current vs Temperature

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

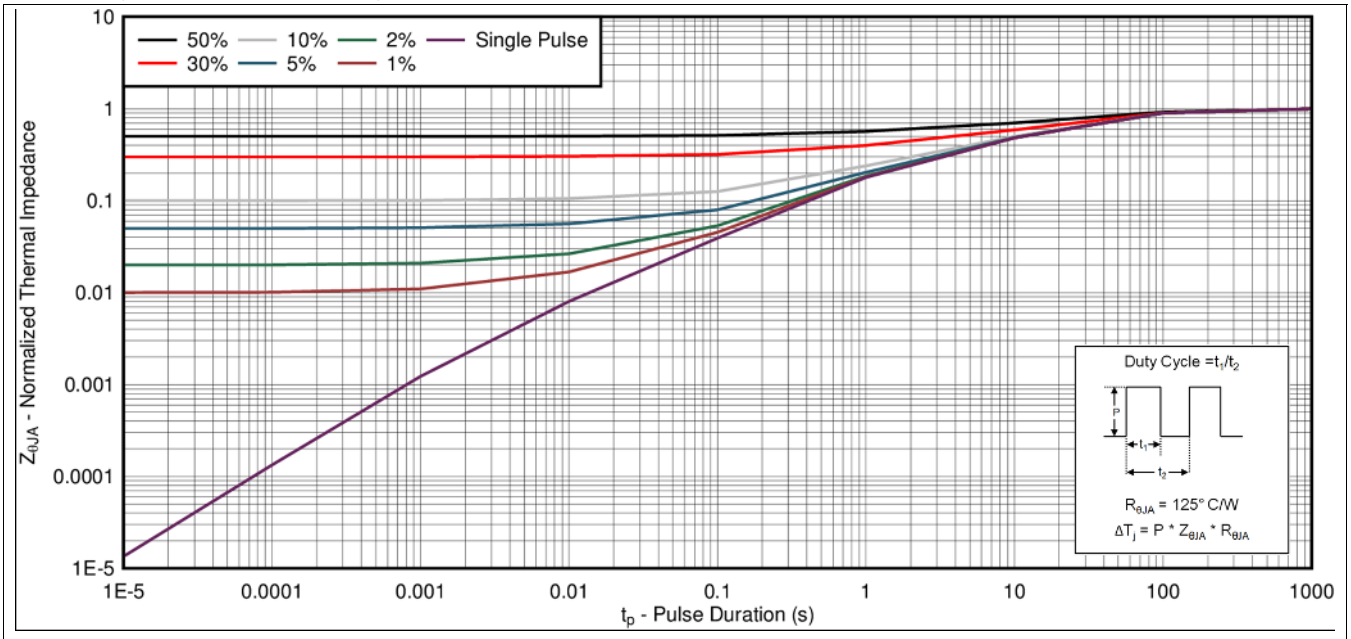


Figure 16. Transient Thermal Impedance

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

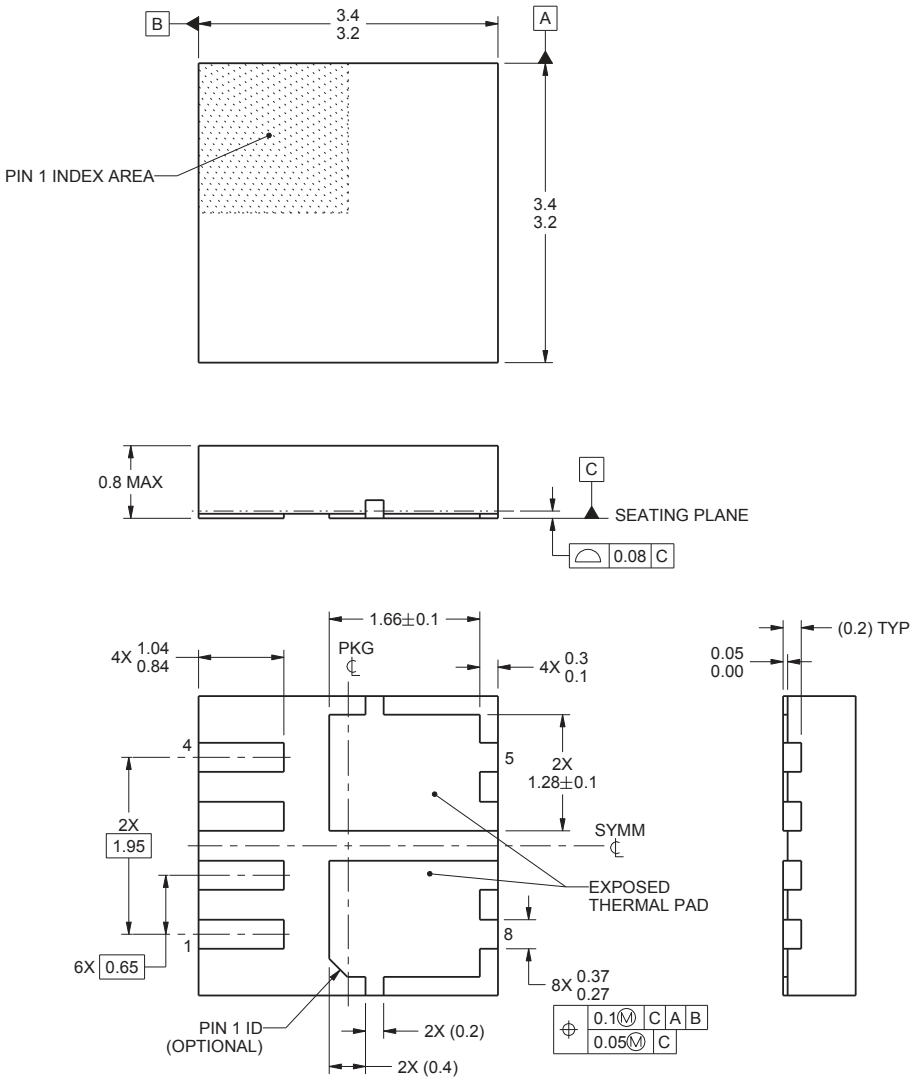
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 DMS Package Dimensions



4222980/A 05/2016

(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

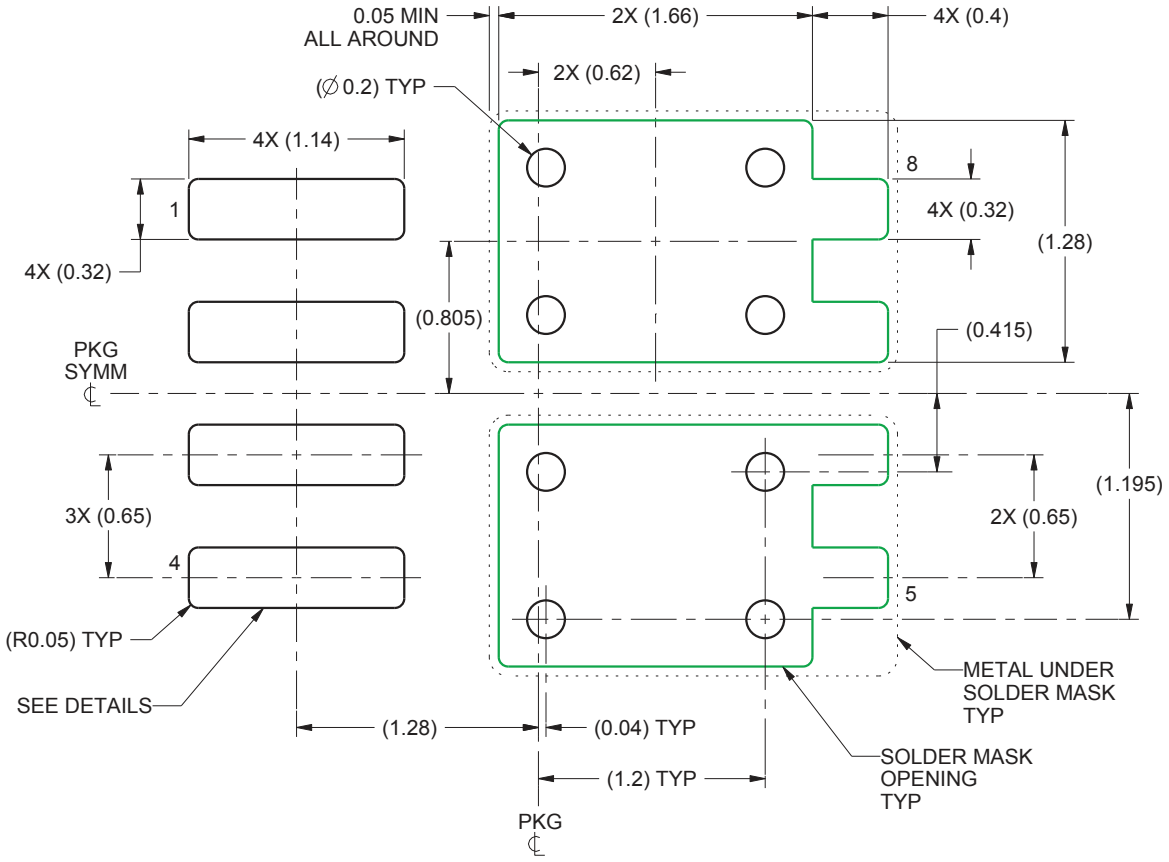
(2) This drawing is subject to change without notice.

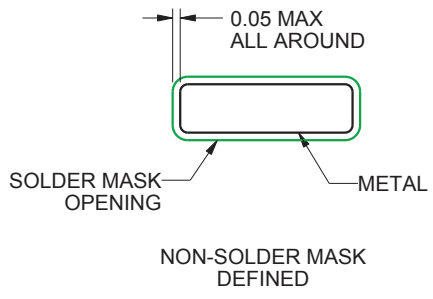
(3) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

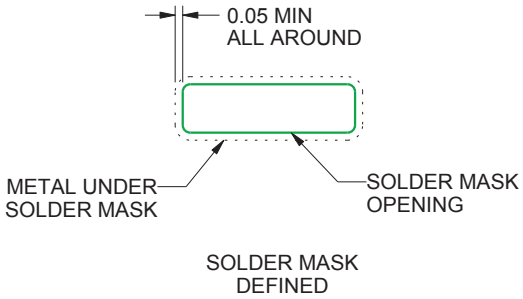
Table 1. Pin Configuration Table

POSITION	DESIGNATION	POSITION	DESIGNATION
1	Gate 1	5	Source 2
2	Drain	6	Source 2
3	Drain	7	Source 1
4	Gate 2	8	Source 1

7.2 Recommended PCB Pattern





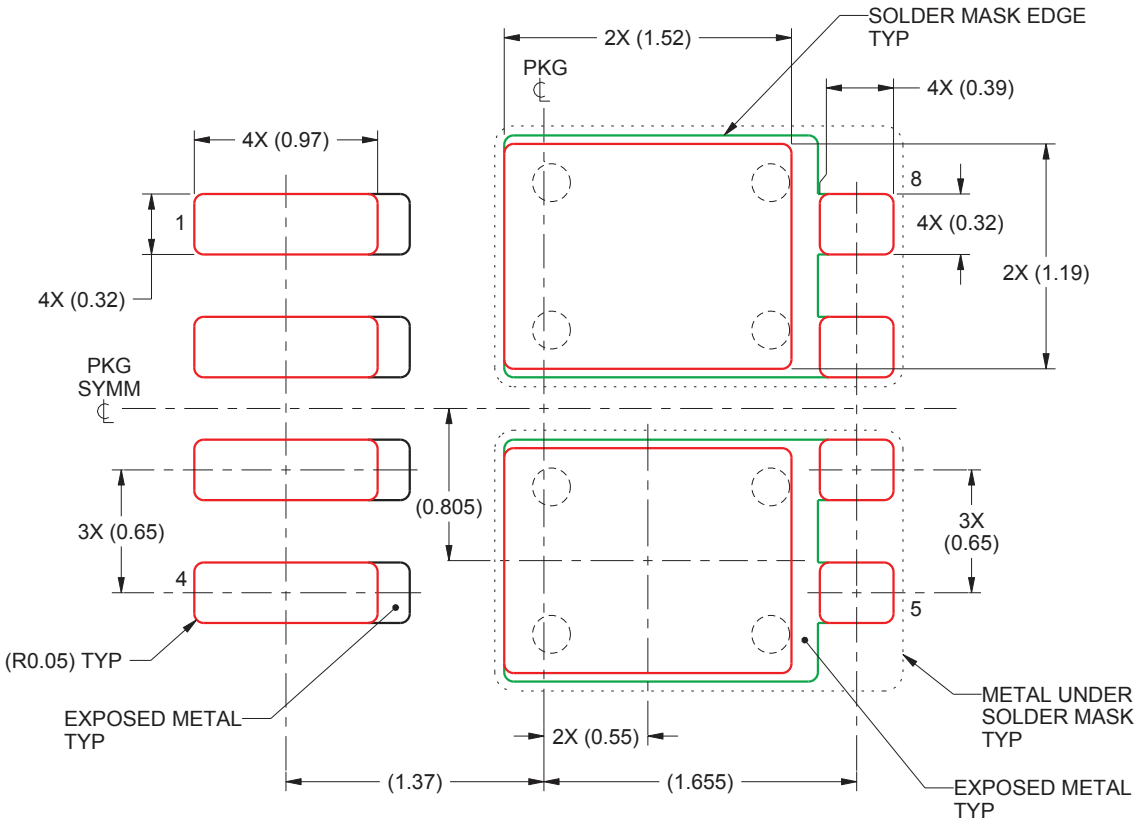


4222980/A 05/2016

(1) This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB Attachment (SLUA271).

(2) Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

7.3 Recommended Stencil Opening



(1) Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87313DMS	ACTIVE	WSON	DMS	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD87313	Samples
CSD87313DMST	ACTIVE	WSON	DMS	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD87313	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

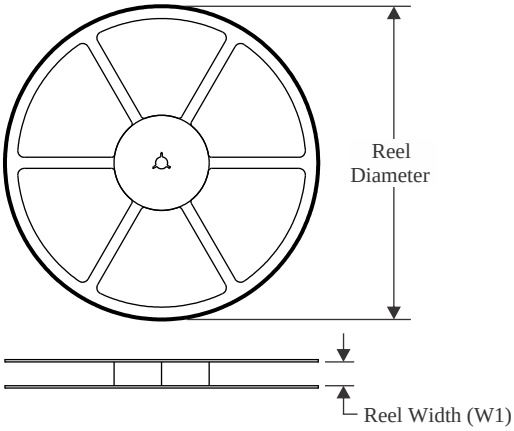
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

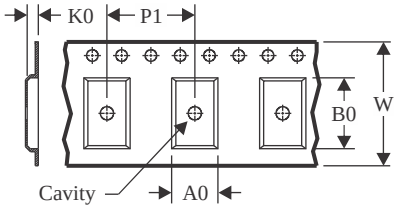
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

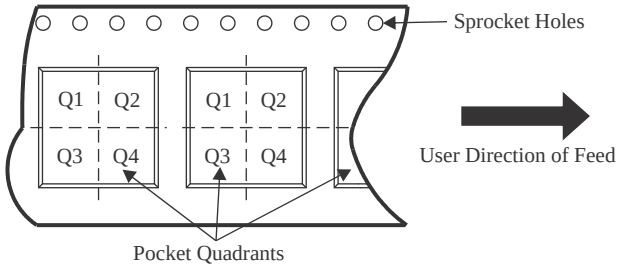


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

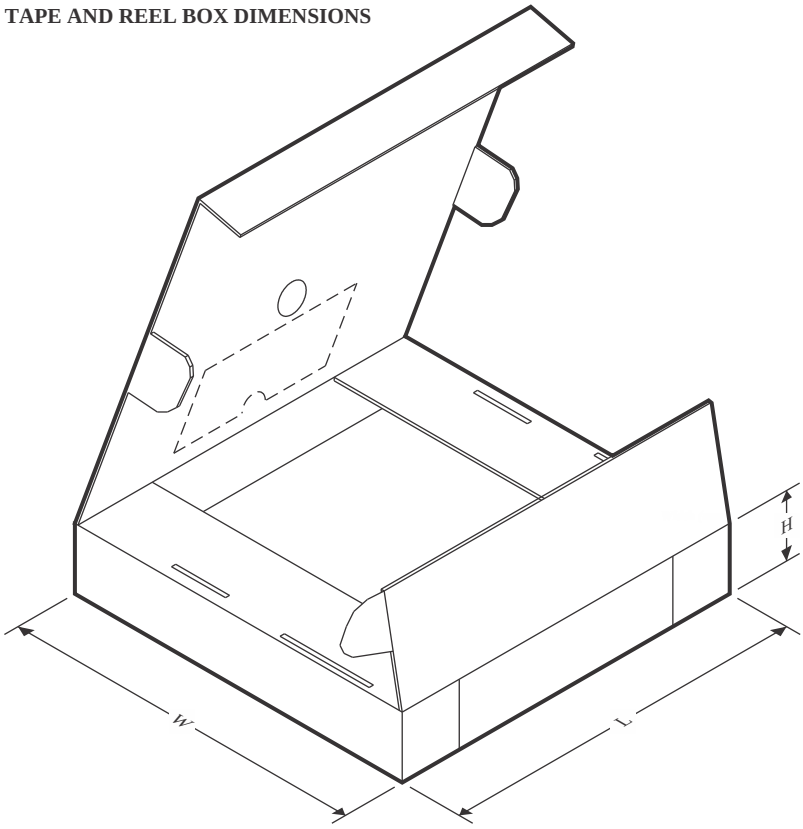
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87313DMST	WSON	DMS	8	250	178.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87313DMST	WSON	DMS	8	250	180.0	180.0	79.0

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