ANALOG DEVICES

Rail-to-Rail Output Audio Amplifiers

SSM2275/SSM2475

FEATURES

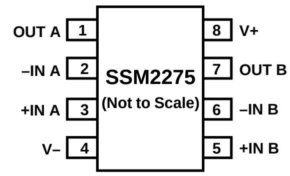
- Single or Dual-Supply Operation
- Excellent Sonic Characteristics
- Low Noise: 7 nV/√Hz
- Low THD: 0.0006%
- Rail-to-Rail Output
- High Output Current: ±50 mA
- Low Supply Current: 1.7 mA/amplifier
- Wide Bandwidth: 8 MHz
- High Slew Rate: 12 V/µs
- No Phase Reversal
- Unity Gain Stable
- Stable Parameters Over Temperature

APPLICATIONS

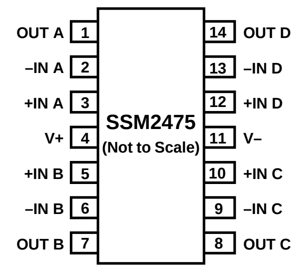
- Multimedia Audio
- Professional Audio Systems
- High Performance Consumer Audio
- Microphone Preamplifier
- MIDI Instruments

PIN CONFIGURATIONS

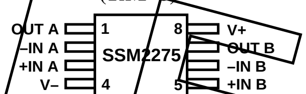
8-Lead Narrow Body SOIC (SO-8)



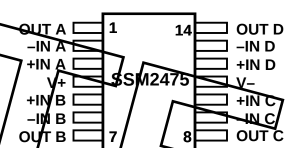
14-Lead Narrow Body SOIC (R-14)



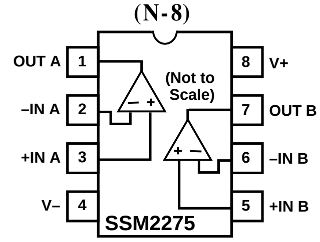
8-Lead microSOIC (RM-8)



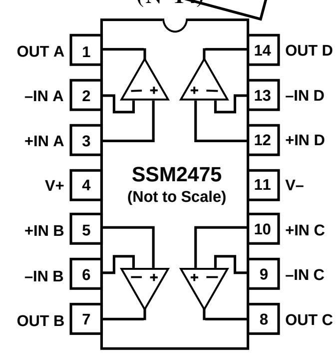
14-Lead TSSOP (RU-14)



8-Lead Plastic DIP (N-8)



14-Lead Plastic DIP (N-14)



GENERAL DESCRIPTION

The SSM2275 and SSM2475 use the Butler Amplifier front end, which combines both bipolar and FET transistors to offer the accuracy and low noise performance of bipolar transistors and the slew rates and sound quality of FETs. This product family includes dual and quad rail-to-rail output audio amplifiers that achieve lower production costs than the industry standard OP275 (the first Butler Amplifier offered by Analog Devices). This lower cost amplifier also offers operation from a single 5 V supply, in addition to conventional ±15 V supplies. The ac performance meets the needs of the most demanding audio applications, with 8 MHz bandwidth, 12 V/µs slew rate and extremely low distortion.

The SSM2275 and SSM2475 are ideal for application in high performance audio amplifiers, recording equipment, synthesizers, MIDI instruments and computer sound cards. Where cascaded stages demand low noise and predictable performance, SSM2275 and SSM2475 are a cost effective solution. Both are stable even when driving capacitive loads.

The ability to swing rail-to-rail at the outputs (see Applications section) and operate from low supply voltages enables designers to attain high quality audio performance, even in single supply systems. The SSM2275 and SSM2475 are specified over the extended industrial (–40°C to +85°C) temperature range and are available in 8-lead plastic DIPs, SOICs, and microSOIC surface mount packages. The SSM2475 is available in 14-lead plastic DIPs, narrow body SOICs, and thin shrink small outline (TSSOP) surface mount packages.

REV. 0

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SSM2275/SSM2475–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = +25°C$, $V_{CM} = 0$ V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	4	mV
		$-40°C \le T_A \le +85°C$		1	6	mV
Input Bias Current	I_B			250	400	nA
		$-40°C \le T_A \le +85°C$		300	500	nA
Input Offset Current	I_{OS}			5	75	nA
		$-40°C \le T_A \le +85°C$		15	125	nA
Input Voltage Range	V_{IN}	$V_S = \pm 15$ V	–14		+14	V
Common-Mode Rejection Ratio	CMRR	$-12.5\ V \le V_{CM} \le +12.5$ V	80	100		dB
		$-40°C \le T_A \le +85°C$, $-12.5\ V \le V_{CM} \le +12.5$ V	80	100		V/mV
A_{VO}		$R_L = 2$ kΩ, $-12\ V \le V_O \le +12$ V	100	240		V/mV
		$-40°C \le T_A \le +85°C$	80	120		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage, High	V_{OH}	$I_L \le 20$ mA	14	14.5		V
		$-40°C \le T_A \le +85°C$	14.5	14.7		V
Output Voltage, Low	V_{OL}	$I_L = 20$ mA		–14	–13.5	V
		$I_L = 10$ mA		–14.6	–14.4	V
		$I_L = 10$ mA, $-40°C \le T_A \le +85°C$		–14.3	–13.9	V
Output Short Circuit Current Limit	I_{SC}		±25	±50	±75	mA
		$-40°C \le T_A \le +85°C$	±17	±40	±80	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$\pm 2.5\ V \le V_S \le \pm 18$ V	85	110		dB
		$-40°C \le T_A \le +85°C$	80	105		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0$ V		1.7	2.9	mA
		$-40°C \le T_A \le +85°C$		1.75	3.0	mA
DYNAMIC PERFORMANCE						
Total Harmonic Distortion	THD	$R_L = 10$ kΩ, f = 1 kHz, $V_O = 1\ V_{RMS}$		0.0006		%
Slew Rate	SR	$R_L = 2$ kΩ‖50 pF	9	12		V/µs
Gain Bandwidth Product	GBW			8		MHz
Channel Separation	CS	$R_L = 2$ kΩ, f =1 kHz		128		dB
NOISE PERFORMANCE						
Voltage Noise Spectral Density	e_n	f > 1 kHz		8		nV/√Hz
Current Noise Spectral Density	i_n	f > 1 kHz		< 1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS ($V_S = +5$ V, $T_A = +25°C$, $V_{CM} = 2.5$ V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	4	mV
		$-40°C \le T_A \le +85°C$		1	6	mV
Input Bias Current	I_B			250	400	nA
		$-40°C \le T_A \le +85°C$		300	500	nA
Input Offset Current	I_{OS}			5	75	nA
		$-40°C \le T_A \le +85°C$		15	125	nA
Input Voltage Range	V_{IN}		0.3		4.7	V
Common-Mode Rejection Ratio	CMRR	$+0.8\ V \le V_{CM} \le +2\ V$		85		dB
		$-40°C \le T_A \le +85°C$		80		dB
A_{VO}		$R_L = 2\ k\Omega$, $-0.5\ V \le V_O \le +4.5\ V$	25	60		V/mV
		$-40°C \le T_A \le +85°C$	20	50		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage, High	V_{OH}	$I_L \le -15$ mA	4.2	4.5		V
		$I_L \le -10$ mA, $-40°C \le T_A \le +85°C$	4.5	4.8		V
Output Voltage, Low	V_{OL}	$I_L \le -15$ mA		0.6	1.0	V
		$I_L \le -10$ mA		0.3	0.5	V
		$I_L \le -10$ mA, $-40°C \le T_A \le +85°C$		0.7	1.1	V
Output Short Circuit Current Limit	I_{SC}	$-40°C \le T_A \le +85°C$		40		mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	$V_O = 0$ V		1.7	2.9	mA
		$-40°C \le T_A \le +85°C$		1.75	3.0	mA
DYNAMIC PERFORMANCE						
Total Harmonic Distortion	THD	$R_L = 10\ k\Omega$, f = 1 kHz, $V_O = 1\ V_{RMS}$		0.0006		%
Slew Rate	SR	$R_L = 2\ k\Omega \| 50$ pF		12		V/µs
Gain Bandwidth Product	GBW	$R_L = 2\ k\Omega \| 10$ pF		6		MHz
Channel Separation	CS	$R_L = 2\ k\Omega$, f = 1 kHz		128		dB
NOISE PERFORMANCE						
Voltage Noise Spectral Density	e_n	f > 1 kHz		8		$nV/\sqrt{Hz}$
Current Noise Spectral Density	i_n	f > 1 kHz		< 1		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage (V_S) . . . . ±18 V
Input Voltage (V_{IN}) . . . . ±15 V
Differential Input Voltage[2] . . . . ±15 V
Storage Temperature Range . . . . $-65°C < T_S < +150°C$
Operating Temperature Range . . . . $-40°C < T_A < +85°C$
Junction Temperature Range . . . . $-65°C < T_S < +150°C$
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C
ESD Susceptability . . . . 2,000 V

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supplies less than ±15 V, the input voltage and differential input voltage must be less than ±15 V.

Package Type	θ_{JA}*	θ_{JC}	Units
8-Lead Plastic DIP	103	43	°C/W
8-Lead SOIC	158	43	°C/W
8-Lead microSOIC	206	43	°C/W
14-Lead Plastic DIP	83	39	°C/W
14-Lead SOIC	120	36	°C/W
14-Lead TSSOP	180	35	°C/W

*θ_{JA} is specified for the worst case conditions, i.e., for device in socket for DIP packages and soldered onto a circuit board for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
SSM2275P	$-40°C < T_A < +85°C$	8-Lead PDIP	N-8
SSM2275S	$-40°C < T_A < +85°C$	8-Lead SOIC	SO-8
SSM2275RM	$-40°C < T_A < +85°C$	8-Lead microSOIC	RM-8
SSM2475P	$-40°C < T_A < +85°C$	14-Lead PDIP	N-14
SSM2475S	$-40°C < T_A < +85°C$	14-Lead SOIC	R-14
SSM2275RU	$-40°C < T_A < +85°C$	14-Lead TSSOP	RU-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2275/SSM2475 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

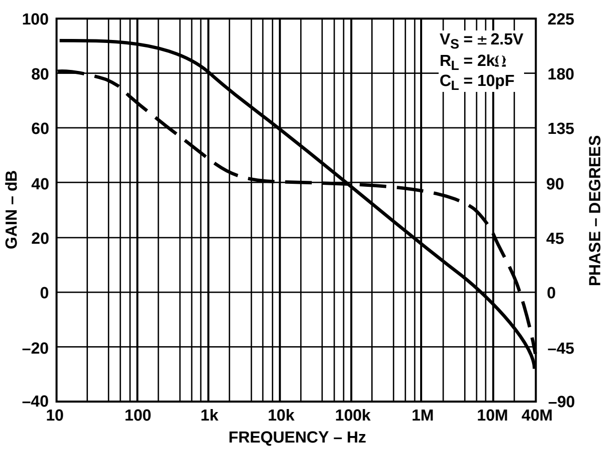


Figure 1. Phase/Gain vs. Frequency

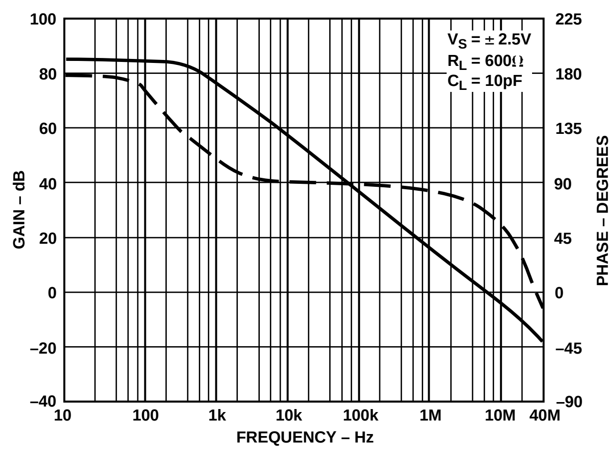


Figure 2. Phase/Gain vs. Frequency

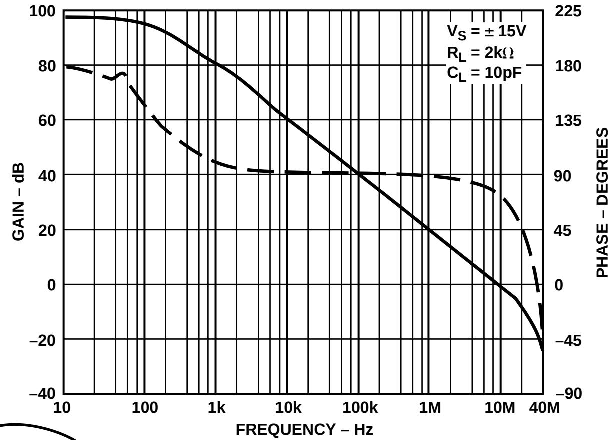


Figure 3. Phase/Gain vs. Frequency

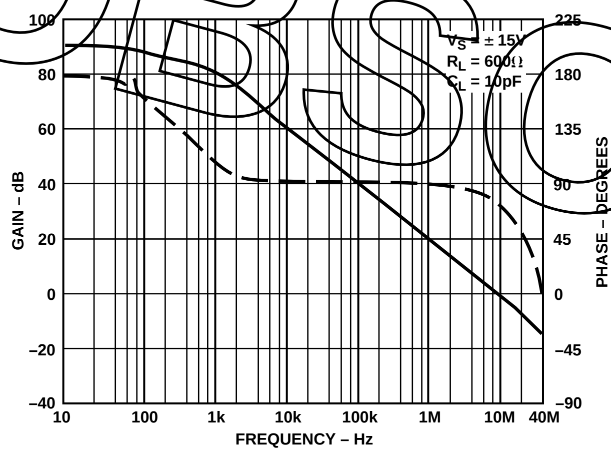


Figure 4. Phase/Gain vs. Frequency

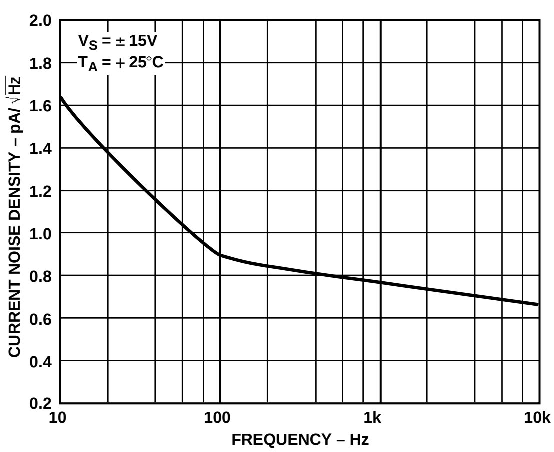


Figure 5. SSM2275 Current Noise Density vs. Frequency

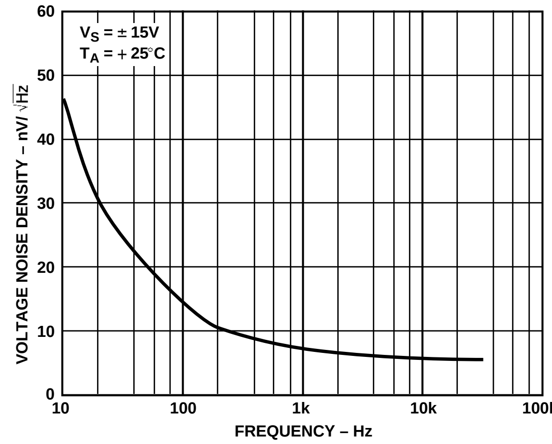


Figure 6. SSM2275 Voltage Noise Density (Typical)

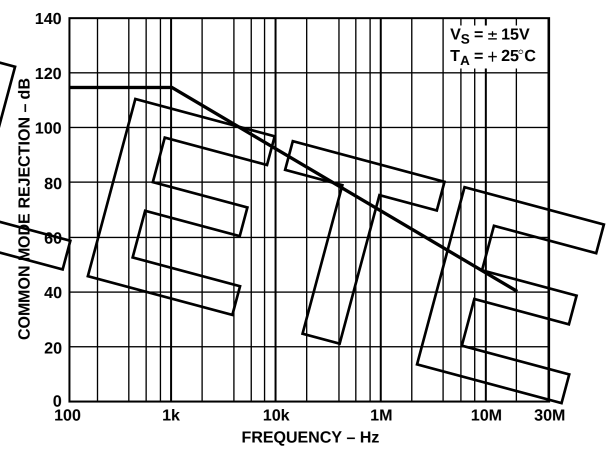


Figure 7. Common-Mode Rejection vs. Frequency

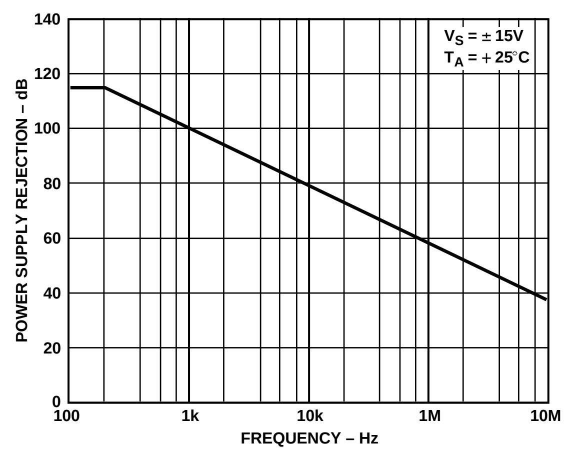


Figure 8. Power Supply Rejection vs. Frequency

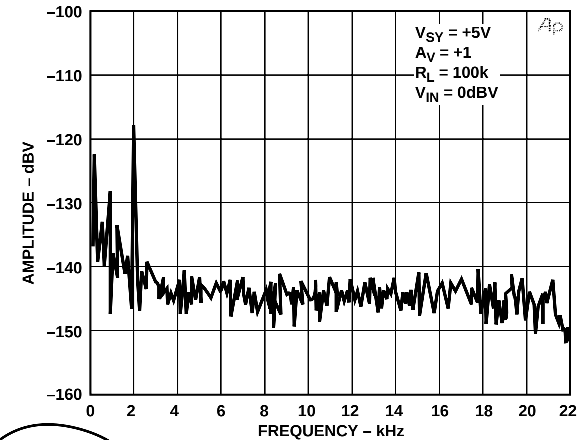


Figure 9. THD vs. Frequency (FFT)

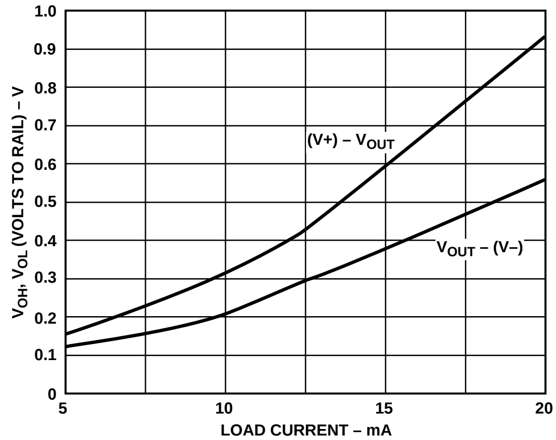


Figure 12. Headroom (V_{OH} and V_{OL}-to-Rails), T_A = +25°C

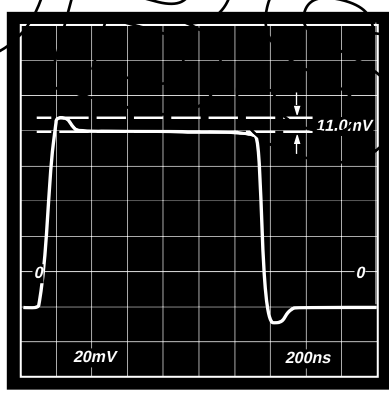


Figure 10. Small Signal Response; R_L = 600 Ω, C_L = 0 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

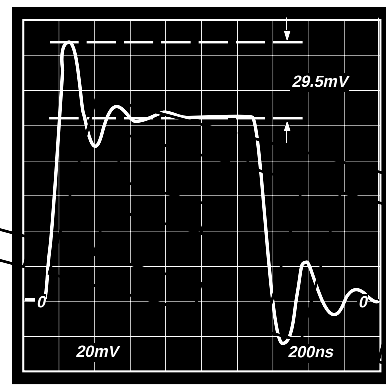


Figure 13. Small Signal Response; R_L = 600 Ω, C_L = 200 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

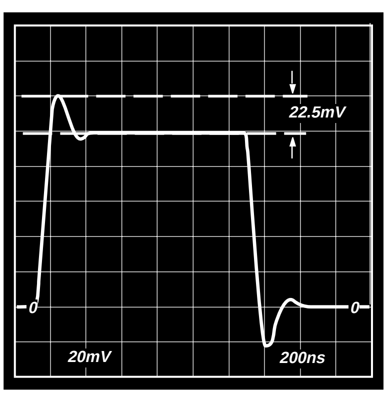


Figure 11. Small Signal Response; R_L = 600 Ω, C_L = 100 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

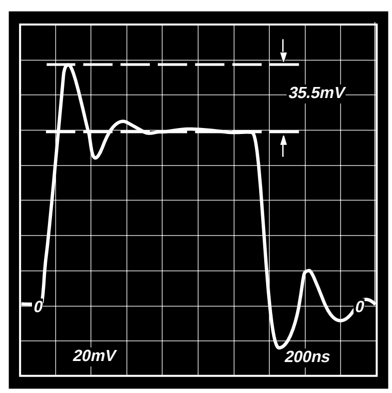


Figure 14. Small Signal Response; R_L = 600 Ω, C_L = 300 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

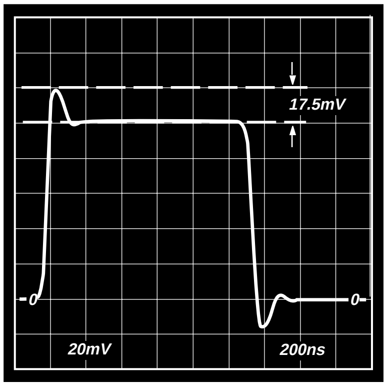


Figure 15. Small Signal Response; R_L = 2 kΩ, C_L = 0 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

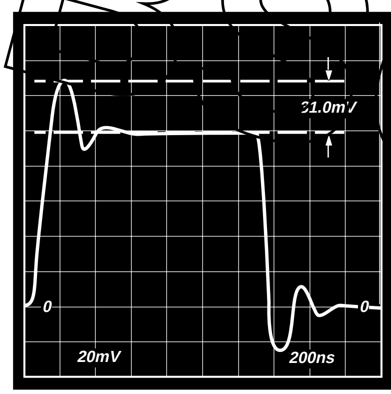


Figure 16. Small Signal Response; R_L = 2 kΩ, C_L = 100 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

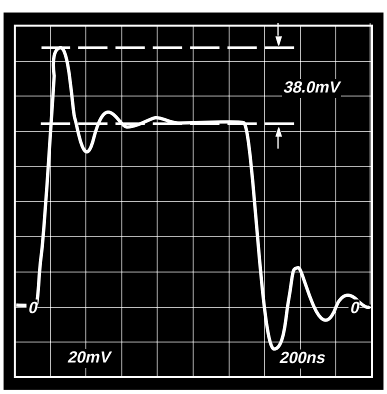


Figure 17. Small Signal Response; R_L = 2 kΩ, C_L = 200 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

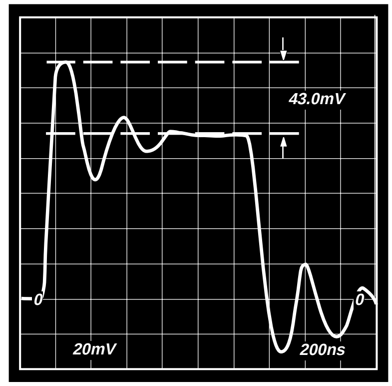


Figure 18. Small Signal Response; R_L = 2 kΩ, C_L = 300 pF, V_S = ±2.5 V, A_V = +1, V_{IN} = 100 mV p–p

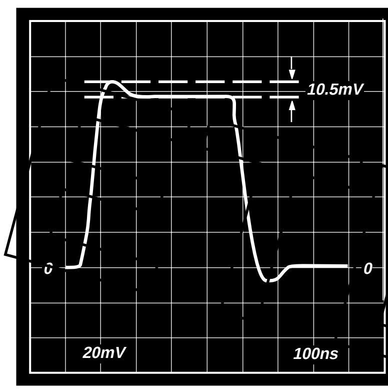


Figure 19. Small Signal Response; R_L = 600 Ω, C_L = 0 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

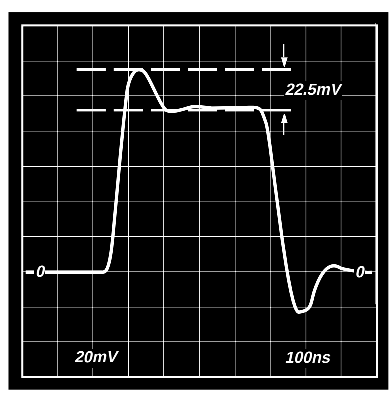


Figure 20. Small Signal Response; R_L = 600 Ω, C_L = 100 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

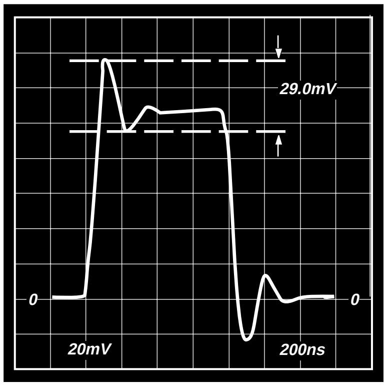


Figure 21. Small Signal Response; R_L = 600 Ω, C_L = 200 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

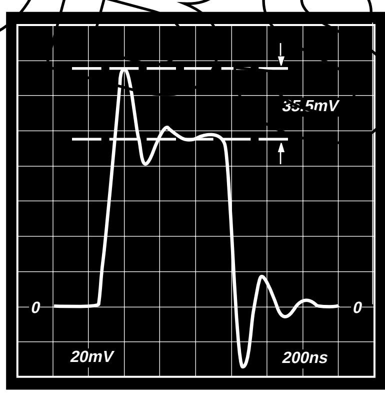


Figure 22. Small Signal Response; R_L = 600 Ω, C_L = 300 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

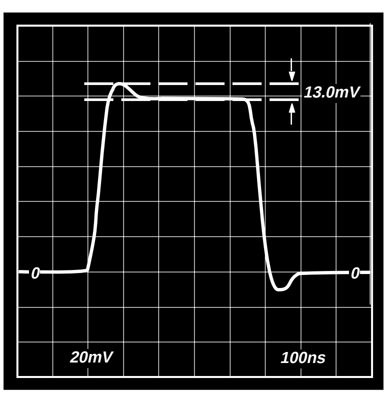


Figure 23. Small Signal Response; R_L = 2 kΩ, C_L = 0 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

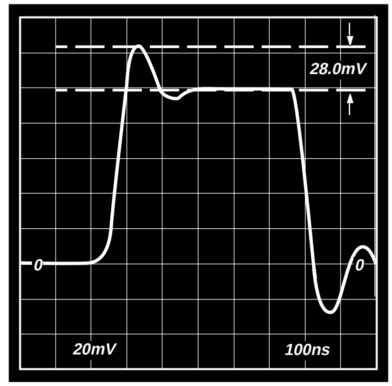


Figure 24. Small Signal Response; R_L = 2 kΩ, C_L = 100 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

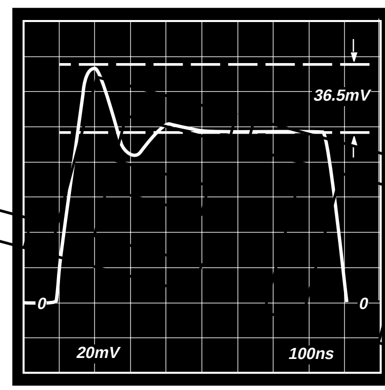


Figure 25. Small Signal Response; R_L = 2 kΩ, C_L = 200 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

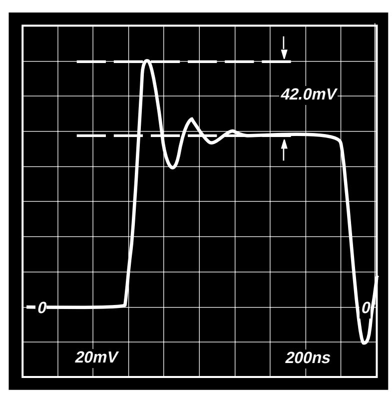


Figure 26. Small Signal Response; R_L = 2 kΩ, C_L = 300 pF, V_S = ±15 V, A_V = +1, V_{IN} = 100 mV p–p

THEORY OF OPERATION

The SSM2275 and SSM2475 are low noise and low distortion rail-to-rail output amplifiers that are excellent for audio applications. Based on the OP275 audiophile amplifier, the SSM2275/SSM2475 offers many similar performance characteristics with the advantage of a rail-to-rail output from a single supply source. Its low input voltage noise figure of 7 nV/√Hz allows the device to be used in applications requiring high gain, such as microphone preamplifiers. Its 11 V/µs slew rate also allows the SSM2275/SSM2475 to produce wide output voltage swings while maintaining low distortion. In addition, its low harmonic distortion figure of 0.0006% makes the SSM2275 and SSM2475 ideal for high quality audio applications.

Figure 27 shows the simplified schematic for a single amplifier. The amplifier contains a Butler Amplifier at the input. This front-end design uses both bipolar and MOSFET transistors in the differential input stage. The bipolar devices, Q1 and Q2, improve the offset voltage and achieve the low noise performance, while the MOS devices, M1 and M2, are used to obtain higher slew rates. The bipolar differential pair is biased with a proportional-to-absolute-temperature (PTAT) bias source, IB1, while the MOS differential pair is biased with a non-PTAT source, IB2. This results in the amplifier having a constant gain-bandwidth product and a constant slew rate over temperature.

The amplifier also contains a rail-to-rail output stage that can sink or source up to 50 mA of current. As with any rail-to-rail output amplifier the gain of the output stage, and consequently the open loop gain of the amplifier, is proportional to the load resistance. With a load resistance of 50 kΩ, the dc gain of the amplifier is over 110 dB. At load currents less than 1 mA, the output of the amplifier can swing to within 30 mV of either supply rail. As load current increases, the maximum voltage swing of the output will decrease. This is due to the collector to emitter saturation voltage of the output transistors increasing with an increasing collector current.

Input Overvoltage Protection

The maximum input differential voltage that can be applied to the SSM2275/SSM2475 is ±7 V. A pair of internal back-to-back Zener diodes are connected across the input terminals. This prevents emitter-base junction breakdown from occurring to the input transistors, Q1 and Q2, when very large differential voltages are applied. If the device's differential voltage could exceed ±7 V, then the input current should be limited to less than ±5 mA. This can be easily done by placing a resistor in series with both inputs. The minimum value of the resistor can be determined by:

$$R_{IN} = \frac{V_{DIFF,\,MAX} - 7}{0.01} \tag{1}$$

There are also ESD protection diodes that are connected from each input to each power supply rail. These diodes are normally reversed biased, but will turn on if either input voltage exceeds either supply rail by more than 0.6 V. Again, should this condition occur the input current should be limited to less than ±5 mA. The minimum resistor value should then be:

$$R_{IN} = \frac{V_{IN,\,MAX}}{5\,mA} \tag{2}$$

In practice, R_{IN} should be placed in series with both inputs to reduce offset voltages caused by input bias current. This is shown in Figure 28.

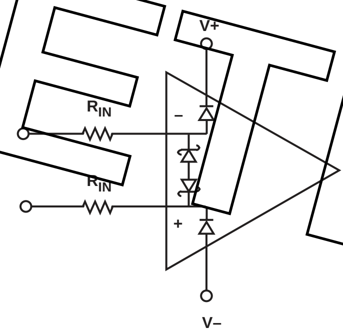


Figure 28. Using Resistors for Input Overcurrent Protection

Output Voltage Phase Reversal

The SSM2275/SSM2475 was designed to have a wide common-mode range and is immune to output voltage phase reversal with an input voltage within the supply voltages of the device. However, if either of the device's inputs exceeds 0.6 V above the posi-

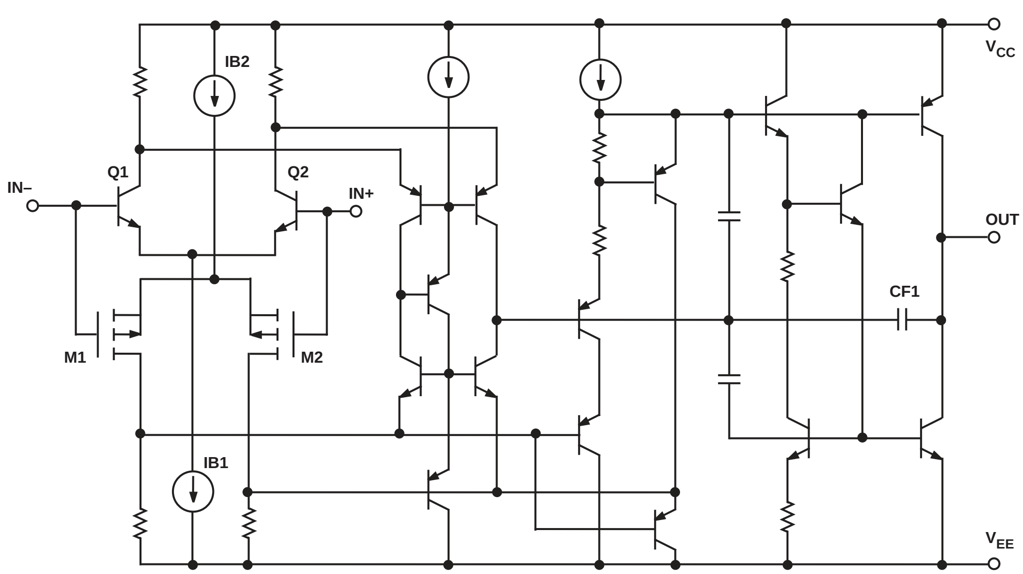


Figure 27. Simplified Schematic

tive voltage supply, the output could exhibit phase reversal. This is due to the input transistor's B–C junction becoming forward biased, causing the polarity of the input terminals of the device to switch.

This phase reversal can be prevented by limiting the input current to +1 mA. This can be done by placing a resistor in series with the input terminal that is expected to be overdriven. The series resistance should be at least:

$$R_{IN} = \frac{V_{IN,MAX} - 0.6}{1\ mA} \tag{3}$$

An equivalent resistor should be placed in series with both inputs to prevent offset voltages due to input bias currents, as shown in Figure 28.

Output Short Circuit Protection

To achieve high quality rail-to-rail performance, the output of the SSM2275/SSM2475 is not short-circuit protected. Shorting the output may damage or destroy the device when excessive voltages or currents are applied. To protect the output stage, the maximum output current should be limited to ±40 mA. Placing a resistor in series with the output of the amplifier as shown in Figure 29, the output current can be limited. The minimum value for R_X can be found from Equation 4.

$$R_X = \frac{V_{SY}}{40\,mA} \tag{4}$$

For a +5 V single supply application, R_X should be at least 125 Ω. Because R_X is inside the feedback loop, V_{OUT} is not affected. The trade off in using R_X is a slight reduction in output voltage swing under heavy output current loads. R_X will also increase the effective output impedance of the amplifier to $R_O + R_X$, where R_O is the output impedance of the device.

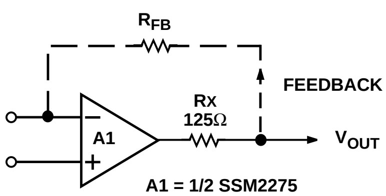


Figure 29. Output Short Circuit Protection Configuration

Power Dissipation Considerations

While many designers are constrained to use very small and low profile packages, reliable operation demands that the maximum junction temperatures not be exceeded. A simple calculation will ensure that your equipment will enjoy reliable operation over a long lifetime. Modern IC design allows dual and quad amplifiers to be packaged in SOIC and microSOIC packages, but it is the responsibility of the designer to determine what the actual junction temperature will be, and prevent it from exceeding the 150°C. Note that while the θ_{JC} is similar between package options, the θ_{JA} for the SOIC and TSSOP are nearly double the P-DIP. The calculation of maximum ambient temperature is relatively simple to make.

$$P_{MAX} = \frac{T_{I,MAX} - T_A}{\theta_{JA}} \tag{5}$$

For example, with the 8-lead SOIC, the calculation gives a maximum internal power dissipation (for all amplifiers, worst case) of P_{MAX} = (150°C – 85°C)/158°C/W = 0.41 W. For the DIP package, a similar calculation indicates that 0.63 W (approximately 50% more) can be safely dissipated. Note that ambient temperature is defined as the temperature of the PC board to which the device is connected (in the absence of radiated or convected heat loss). It is good practice to place higher power devices away from the more sensitive circuits. When in doubt, measure the temperature in the vicinity of the SSM2275 with a thermocouple thermometer.

Maximizing Low Distortion Performance

Because the SSM2275/SSM2475 is a very low distortion amplifier, careful attention should be given to the use of the device to prevent inadvertently introducing distortion. Source impedances seen by both inputs should be made equal, as shown in Figure 28, with $R_B = R1||R_F$ for minimum distortion. This eliminates any offset voltages due to varying bias currents. Proper power supply decoupling reduces distortion due to power supply variations.

Because the open loop gain of the amplifier is directly dependent on the load resistance, loads of less than 10 kΩ will increase the distortion of the amplifier. This is a trait of any rail-to-rail op amp. Increasing load capacitance will also increase distortion.

It is recommended that any unused amplifiers be configured as a unity gain follower with the noninverting input tied to ground. This minimizes the power dissipation and any potential crosstalk from the unused amplifier.

As with many FET-type amplifiers, the PMOS devices in the input stage exhibit a gate-to-source capacitance that varies with the common mode voltage. In an inverting configuration, the inverting input is held at a virtual ground and the common-mode voltage does not vary. This eliminates distortion due to input capacitance modulation. In noninverting applications, the gate-to-source voltage is not constant, and the resulting capacitance modulation can cause a slight increase in distortion.

Figure 30 shows a unity gain inverter and a unity gain follower configuration. Figure 31 shows an FFT of the outputs of these amplifiers with a 1 kHz sine wave. Notice how the largest harmonic amplitude (2nd harmonic) is –120 dB below the fundamental (0.0001%) in the inverting configuration.

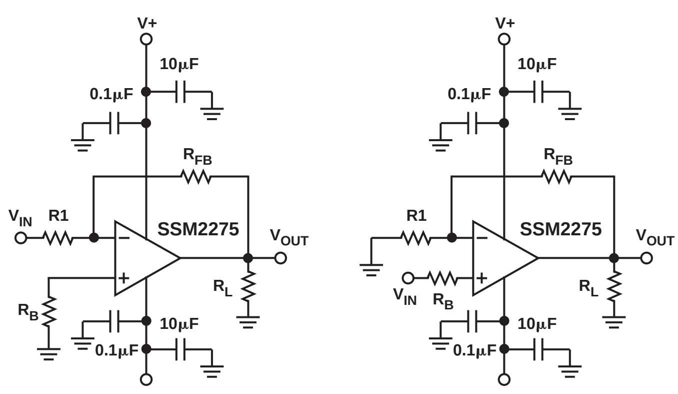


Figure 30. Basic Inverting and Noninverting Amplifiers

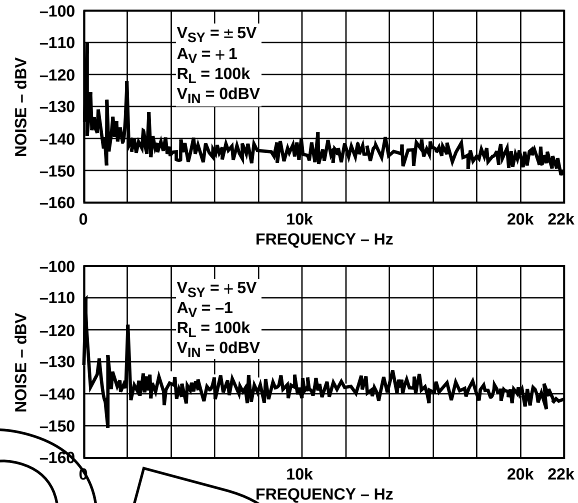


Figure 31. Spectral Graph of Amplifier Outputs

Settling Time

The high slew rate and wide gain-bandwidth product of the SSM2275 and SSM2475 amplifiers result in fast settling times (t_S < 1 µs) that are suitable for 16 and 20-bit applications. The test circuit used to measure the settling time of the SSM2275/SSM2475 is shown in Figure 32. This test method has advantages over false-sum node techniques of measuring settling times in that the actual output of the amplifier is measured, instead of an error voltage at the sum node. Common-mode settling effects are also taken into account in this circuit in addition to slew rate and bandwidth factors.

The output waveform of the device under test is clamped by Schottky diodes and buffered by the JFET source follower. The signal is amplified by a factor of ten by the OP260 current feedback amplifier and then Schottky-clamped at the output to the oscilloscope. The 2N2222 transistor sets up the bias current for the JFET and the OP41 is configured as a fast integrator, providing overall dc offset nulling at the output.

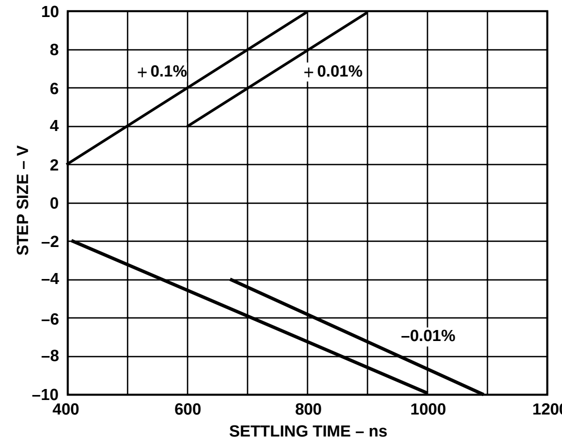


Figure 33. Settling Time vs. Step Size

Overdrive Recovery

The overdrive, or overload, recovery time of an amplifier is the time required for the output voltage to return to a rated output voltage from a saturated condition. This recovery time can be important in applications where the amplifier must recover quickly after a large transient event, or overload. The circuit in Figure 34 was used to evaluate the recovery time for the SSM2275/SSM2475. Also shown are the input and output voltages. It takes approximately 0.5 µs for the device to recover from output overload.

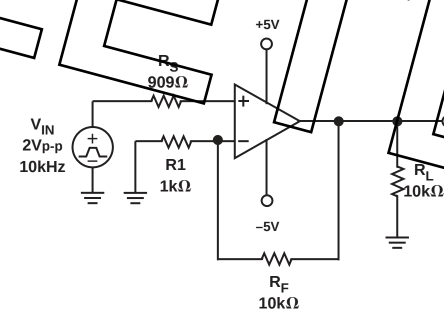


Figure 34. Overload Recovery Time Test Circuit

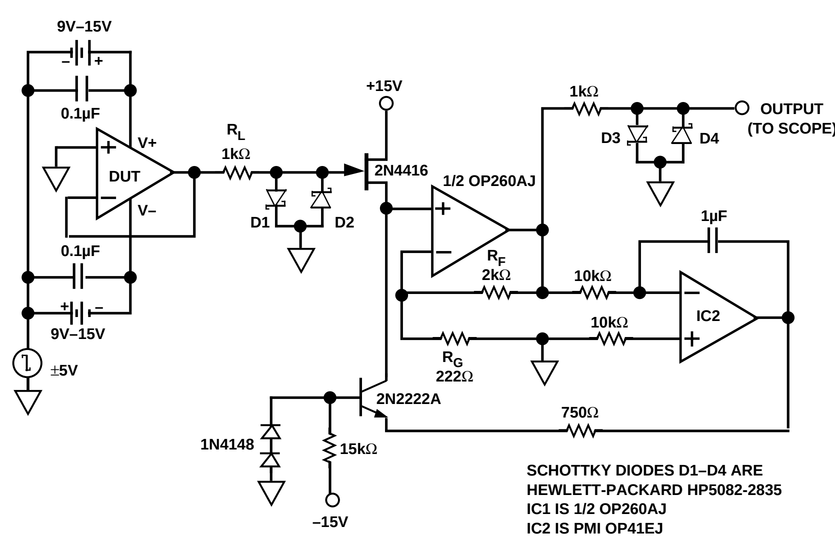


Figure 32. Settling Time Test Fixture

Capacitive Loading

The output of the SSM2275/SSM2475 can tolerate a degree of capacitive loading. However, under certain conditions, a heavy capacitive load could create excess phase shift at the output and put the device into oscillation. The degree of capacitive loading is dependent on the gain of the amplifier. At unity gain, the amplifier could become unstable at loads greater than 600 pF. At gain greater than unity, the amplifier can handle a higher degree of capacitive load without oscillating. Figure 35 shows how to configure the device to prevent oscillations from occurring.

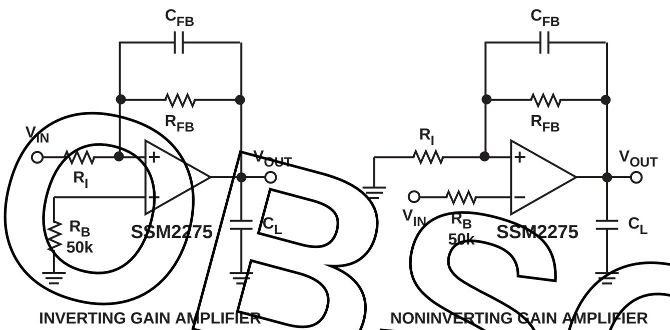


Figure 35. Configurations for Driving Heavy Capacitive Loads

R_B should be at least 50 kΩ. To minimize offset voltage, the parallel combination of R_{FB} and R_I should be equal to R_B. Setting a minimum C_F of 15 pF bandlimits the amplifier enough to eliminate any oscillation problems from any sized capacitive load. The low-pass frequency is determined by:

$$f_{-3dB} = \frac{1}{2\pi R_{FB} C_F} \tag{6}$$

With R_{FB} = 50 kΩ and C_F = 15 pF, this results in an amplifier with a 210 kHz bandwidth that can be used with any capacitive load. If the amplifier is being used in a non-inverting unity gain configuration and R_I is omitted, C_{FB} should be at least 100 pF. If the offset voltage can be tolerated at the output, R_{FB} can be replaced by a short and C_{FB} can be removed entirely. With the typical input bias current of 200 nA and R_B = 50 kΩ, the increase in offset voltage would be 10 mV. This configuration will stabilize the amplifier under all capacitive loads.

Single Supply Differential Line Driver

Figure 36 shows a single supply differential line driver circuit that can drive a 600 Ω load with less than 0.001% distortion. The design mimics the performance of a fully balanced transformer based solution. However, this design occupies much less board space while maintaining low distortion and can operate down to dc. Like the transformer based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1.

R13 and R14 set up the common-mode output voltage equal to half of the supply voltage. C1 is used to couple the input signal and can be omitted if the input's dc voltage is equal to half of the supply voltage. The minimum input impedance of the circuit as seen from V_{IN} is:

$$R_{IN} = (R1 + R5) \parallel (R3 + R7) \parallel R11 \tag{7}$$

For the values given in Figure 36, R_{IN} = 5 kΩ. With C1 omitted the circuit will provide a balanced output down to dc, otherwise the –3 dB corner for the input frequency is set by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_L} \tag{8}$$

The circuit can also be configured to provide additional gain if desired. The gain of the circuit is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{2(R2)}{R1} \tag{9}$$

where $V_{OUT} = V_{O1} - V_{O2}$, $R1 = R3 = R5 = R7$ and, $R2 = R4 = R6 = R8$

Figure 37 shows the THD+N versus frequency response of the circuit while driving a 600 Ω load at 1 V rms.

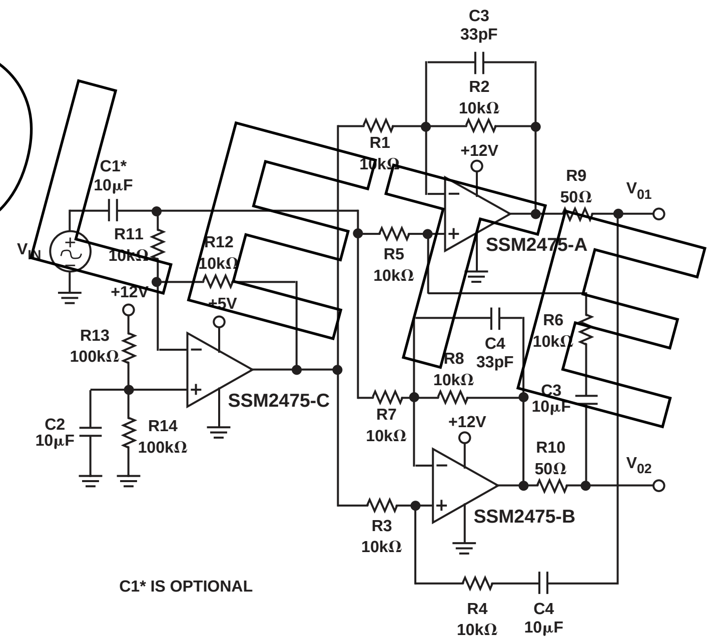


Figure 36. A Low Noise, Single Supply Differential Line Driver

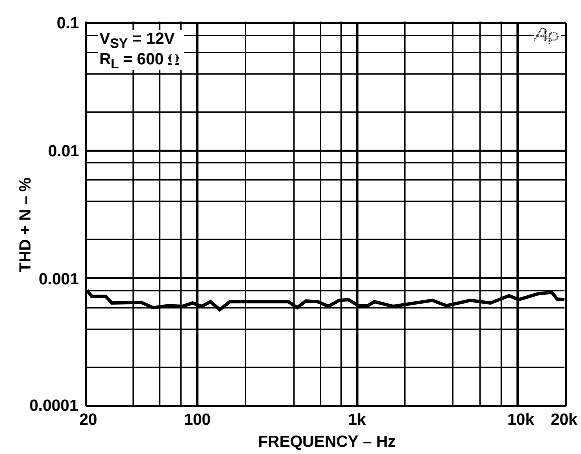


Figure 37. THD+N vs. Frequency of Differential Line Driver

Multimedia Soundcard Microphone Preamplifier

The low distortion and low noise figures of the SSM2275 make it an excellent device for amplifying low level audio signals. Figure 38 shows how the SSM2275 can be configured as a stereo microphone preamplifier driving the input to a multimedia sound codec, the AD1848. The SSM2275 can be powered from the same +5 V single supply as the AD1848. The V_{REF} pin on the AD1848 provides a bias voltage of 2.25 V for the SSM2275. This voltage can also be used to provide phantom power to a condenser microphone through a 2N4124 transistor buffer and 2 kΩ resistors. The phantom power circuitry can be omitted for dynamic microphones. The gain of SSM2275 amplifiers is set by R2/R1 which is 100 (40 dB) as shown. Figure 39 shows the device's THD+N performance with a 1 V_{RMS} output.

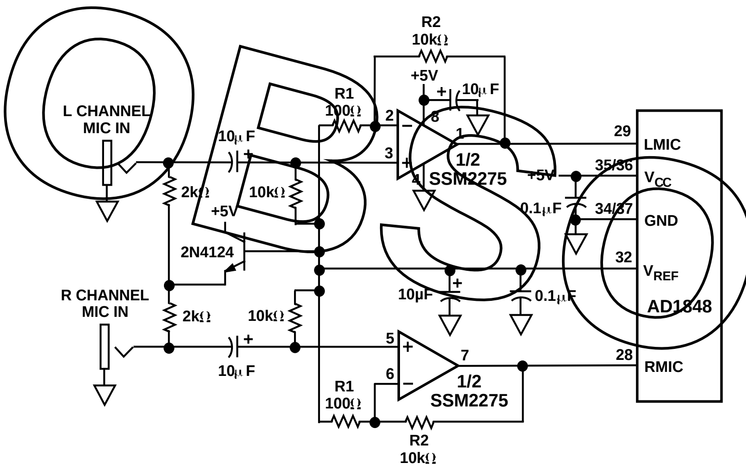


Figure 38. Low Noise Microphone Preamplifier for Multimedia Soundcard Codec

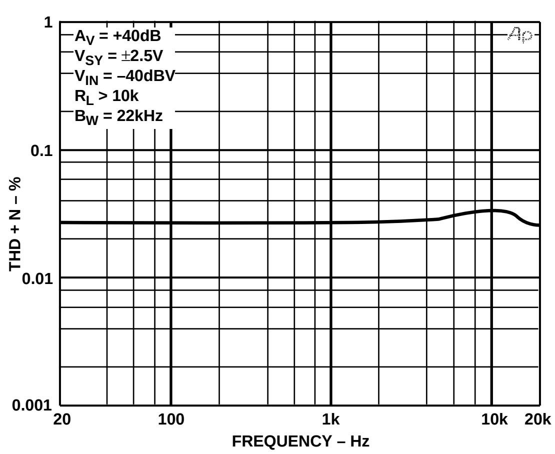


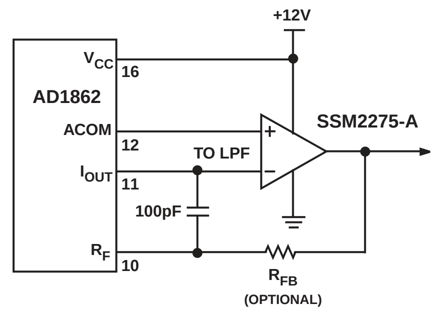
Figure 39. THD+N vs. Frequency (V_{SY} = +5 V, A_V = 40 dB, V_{OUT} = 1 V rms)

High Performance I-V Converters and Filters for 20-Bit DACs

Because of the increasing resolution and lower harmonic distortions required by more audio applications, the need for high quality amplifiers at the output of D/A converters becomes critical. The SSM2275 and SSM2475 can be used as current-to-voltage converters and smoothing filters for 18- and 20-bit DACs, achieving 0.0006% THD+N figures while running from the same +5 V or +12 V source used to power the D/A converter. Figure 40 shows how the SSM2275 can be used with the AD1862, a current output 20-bit DAC.

The AD1862 has a built in 3 kΩ resistor that is connected from the inverting input to the output of the amplifier. The full-scale output current of the AD1862 is ±1 mA, resulting in a maximum output voltage of ±3 V. Additional feedback resistance can be added in the feedback loop to increase the output voltage. With R_{FB} connected the maximum output voltage will be:

$$V_{OUT,MAX} = 1mA \times \left(3k\Omega + R_{FB}\right) \quad (10)$$

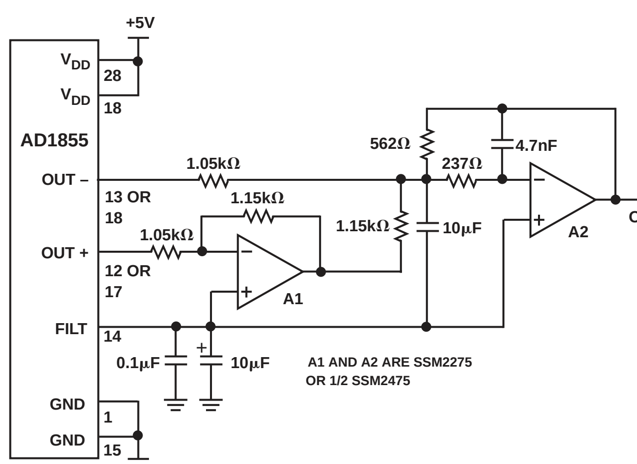


NOTE: ADDITIONAL PIN CONNECTIONS OMITTED FOR CLARITY

Figure 40. A High Performance I-V Converter for a 20-Bit DAC

In Figure 41, the SSM2275 is used as a low-pass filter for one channel of the AD1855, a 24-bit 96 kHz stereo sigma-delta DAC, which uses a complementary voltage output. The filter is configured as a second order low-pass Bessel filter with a cutoff frequency of 50 kHz. This provides a phase linear response from dc to 24 kHz, which is ideal for high quality audio applications. The SSM2275 can be connected to the same +5 V power supply source, that the AD1855 is connected to, eliminating the need for extra power circuitry. The FILT output (Pin 14) from the AD1855 provides a common reference voltage equal to half of the supply voltage for the SSM2275.

Amplifier A1 is used as a unity-gain inverter for the positive output of the AD1855. The output of A1 is combined with a negative output of the AD1855 into the active low pass filter around A2. The output impedance of each output of the AD1855 is 100 Ω which must be taken into account to achieve proper dc gain, which in Figure 41 is unity gain. In this configuration the SSM2275 can drive reasonable capacitive loads, making the device suitable for the RCA jack line outputs found in most consumer audio equipment.



NOTE: ADDITIONAL PIN CONNECTIONS OMITTED FOR CLARITY

Figure 41. Low-Pass Filter for a 24-Bit Stereo Sigma-Delta DAC

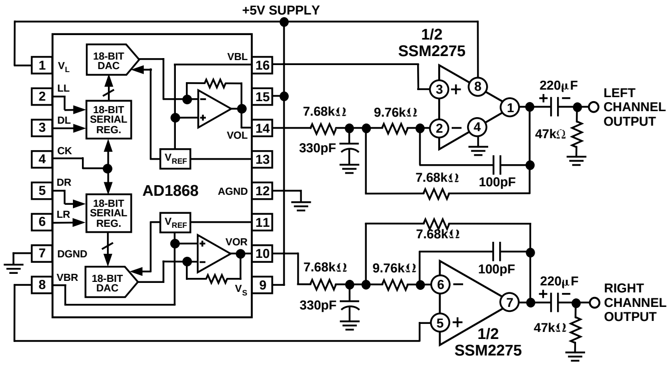


Figure 42. A Smoothing Filter for an 18-Bit Stereo DAC

SPICE Macro-model

The SPICE macro-model for the SSM2275 is shown in Listing 1 on the following page. This model is based on typical values for the device and can be downloaded from Analog Devices' Internet site at **www.analog.com**. The model uses a common emitter output stage to provide rail-to-rail performance. A resistor and dc voltage source, in series with the collector, accurately portray output dropout voltage versus output current. The VCMH and VCML sources set the upper and lower limits of the input common mode voltage range. Both are set up as a function of the supply voltage to mimic the varying common mode range with supply voltage. The EOS voltage source establishes the offset voltage and is also used to create the common-mode rejection and power supply rejection characteristics for the model.

A secondary pole section is also set up to vary the gain bandwidth product and phase margin of the model based on the supply voltage. The H1 and VR1 sources set up an equivalent resistor that is linearly varied with supply voltage. This equivalent resistance, in parallel with C2, creates the secondary pole. G2 is also linearly varied to increase the GBW at higher supply voltages. With a supply voltage of 5 V, the gain bandwidth product is 6.3 MHz with a 47 degree phase margin. At a 30 V supply voltage, the GBW product moves out to 7.5 MHz with 48° phase margin.

The broadband input referred voltage noise for the model is 6.8 nV/$\sqrt{\text{Hz}}$. Flicker noise characteristics are also accurately modeled with the 1/f corner frequency set through the KF and AF terms in the input stage transistors. Finally, a voltage-controlled current source, GSY, is used to model the amplifier's supply current versus supply voltage characteristics.

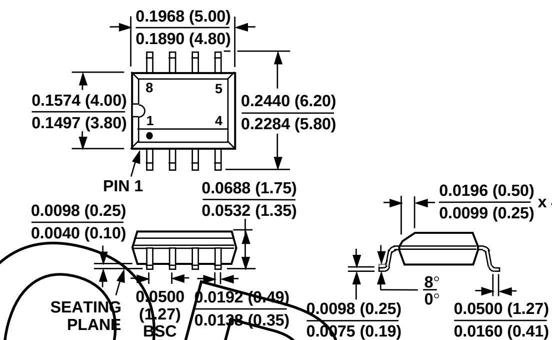
Listing 1: SSM2275 SPICE Macro-Model

```
* SSM2275 SPICE Macro-Model Typical Values
* 8/97, Ver. 1
* TAM / ADSC
*
* Node assignments
*                      non-inverting input
*                      |    inverting input
*                      |    |     positive supply
*                      |    |     |     negative supply
*                      |    |     |     |    output
*                      |    |     |     |    |
*                      |    |     |     |    |
.SUBCKT SSM2275        1    2     99    50   45
*
* INPUT STAGE
*
Q1  4  3  5 QNIX
Q2  6  2  7 QNIX
RC1   99 11 15E3
RC2   99 12 15E3
RE1    5  8 1E3
RE2    7  8 1E3
EOS   3  1 POLY(2) (61,98) (73,98) 1.5E-3 1.78E-5 1
IOS    1  2 5E-9
ECMH1  4 11 POLY(1) (99,50) 0.9 -30E-3
ECMH2  6 12 POLY(1) (99,50) 0.9 -30E-3
ECML1  9 50 POLY(1) (99,50) 0.1 30E-3
ECML2 10 50 POLY(1) (99,50) 0.1 30E-3
D1     9  5 DX
D2    10  7 DX
D3    13  1 DZ
D4     2 13 DZ
IBIAS  8 50 200E-6
*
* CMRR=115 dB, ZERO AT 1kHz, POLE AT 10kHz
*
ECM1 60 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 60 61 159.2E3
RCM2 61 98 17.66E3
CCM1 60 61 1E-9
*
* PSRR=120dB, ZERO AT 1kHz
*
RPS1 70  0 1E6
RPS2 71  0 1E6
CPS1 99 70 1E-5
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 1.59E6
CPS3 72 73 1E-10
RPS4 73 98 1.59
*
* INTERNAL VOLTAGE REFERENCE
*
RSY1 99 91 100E3
RSY2 50 90 100E3
VSN1 91 90 DC 0
EREF 98  0 (90,0) 1
GSY  99 50 POLY(1) (99,50) 0.97E-3 -7E-6
*
* ADAPTIVE POLE AND GAIN STAGE
* AT Vsy= 5, fp=12.50MHz,Av=1
* AT Vsy=30, fp=18.75MHz,Av=1.16
*
G2  98 20 POLY(2) (4,6) (99,50) 0 80.3E-6 0 0 2.79E-6
VR1 20 21 DC 0
H1  21 98 POLY(2) VR1 VSN1 0 11.317E3 0 0 -28.29E6
C2  20 98 1.2E-12
*
* POLE AT 90MHz
*
G3 98 23 (20,98) 565.5E-6
R5 23 98 1.768E3
C3 23 98 1E-12
*
* GAIN STAGE
*
G1 98 30 (23,98) 733.3E-6
R1 30 98 9.993E3
CF 30 45 200E-12
D5 31 99 DX
D6 50 32 DX
V1 31 30 0.6
V2 30 32 0.6
*
* OUTPUT STAGE
*
Q3  46 42 99 QPOX
Q4  47 44 50 QNOX
RO1 46 48 30
RO2 47 49 30
VO1 45 48 15E-3
VO2 49 45 10E-3
RB1 41 42 200
RB2 43 44 200
EO1 99 41 POLY(1) (98,30) 0.7528 1
EO2 43 50 POLY(1) (30,98) 0.7528 1
*
* MODELS
*
.MODEL QNIX NPN(IS=1E-16,BF=400,KF=1.96E-14,AF=1)
.MODEL QNOX NPN(IS=1E-16,BF=100,VAF=130)
.MODEL QPOX PNP(IS=1E-16,BF=100,VAF=130)
.MODEL DX D(IS=1E-16)
.MODEL DZ D(IS=1E-14,BV=6.6)
.ENDS SSM2275
```

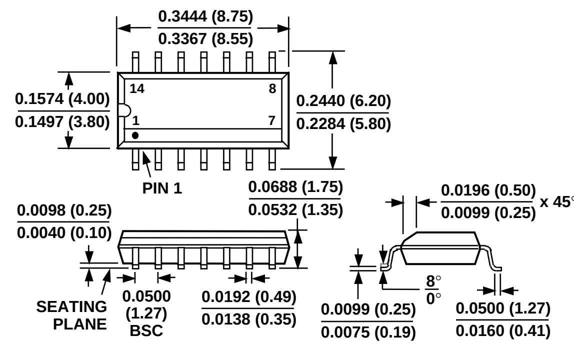
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

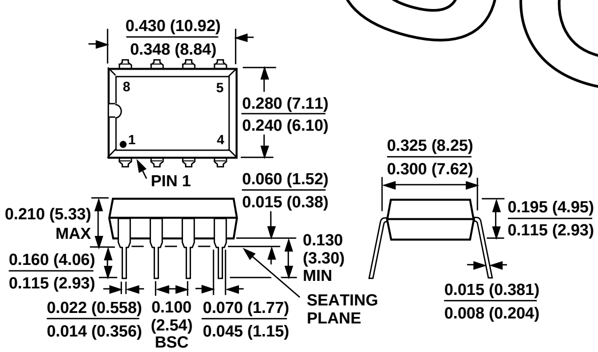
8-Lead SOIC (SO-8)



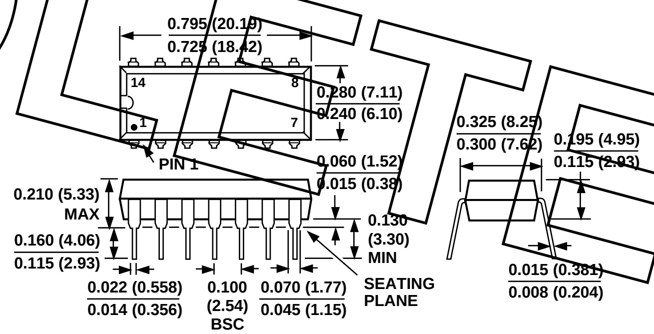
14-Lead SOIC (R-14)



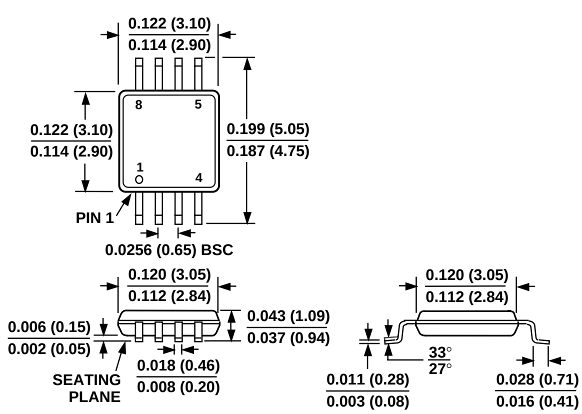
8-Lead Plastic DIP (N-8)



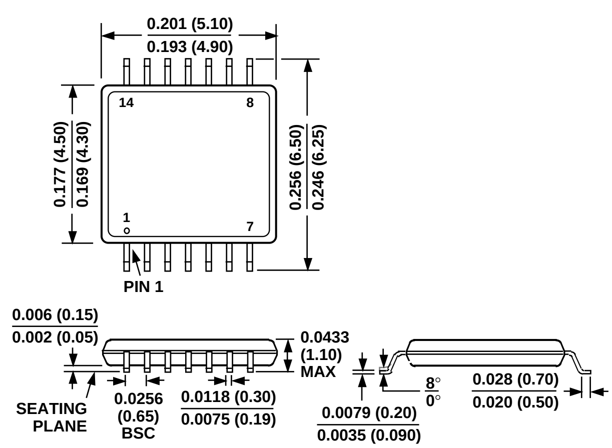
14-Lead Plastic DIP (N-14)



8-Lead micro SOIC (RM-8)



14-Lead TSSOP (RU-14)



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PRINTED IN U.S.A.