DS40MB200 Dual 4-Gbps 2:1/1:2 CML MUX/Buffer With Transmit Pre-Emphasis and Receive Equalization

1 Features

- 1-Gbps to 4-Gbps Low Jitter Operation
- Fixed Input Equalization
- Programmable Output Pre-Emphasis
- Independent Switch and Line Side Pre-Emphasis Controls
- Programmable Switch-Side Loopback Mode
- On-Chip Terminations
- 3.3-V Supply
- ESD Rating of 6-kV HBM
- 48-leadless WQFN Package (7 mm × 7 mm)
- 0°C to +85°C Operating Temperature Range

2 Applications

- Backplane or Cable Driver
- Redundancy and Signal Conditioning Applications
- XAUI

3 Description

The DS40MB200 device is a dual signal conditioning 2:1 multiplexer (MUX) and 1:2 fan-out buffer designed for use in backplane-redundancy applications. Signal conditioning features include continuous time linear equalization (CTLE) and programmable output pre-emphasis, extending data communication in FR4 backplanes at rates up to 4 Gbps. Each input stage has a fixed equalizer to reduce intersymbol interference distortion from board traces.

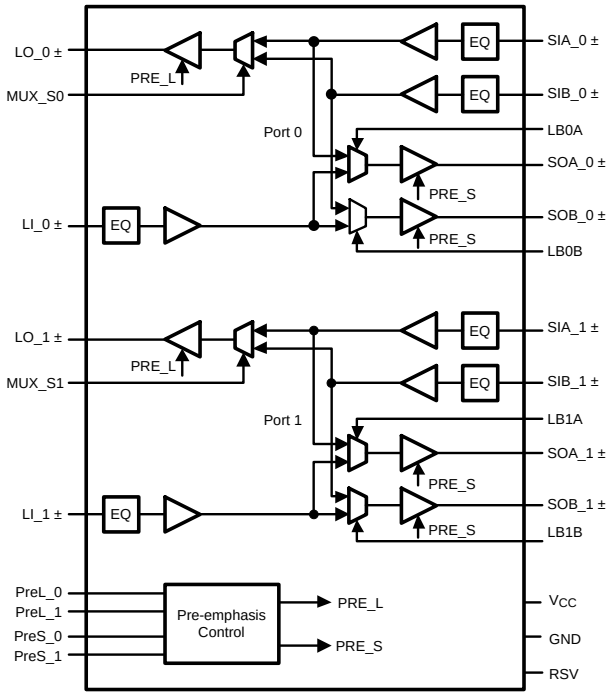
All output drivers have four selectable steps of pre-emphasis to compensate for transmission losses from long FR4 backplanes and reduce deterministic jitter. The pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs are internally terminated with 100-Ω differential terminating resistors. All drivers are internally terminated with 50 Ω to V_{CC}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS40MB200	WQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



All CML inputs and outputs must be AC coupled for optimal performance.

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4 Revision History

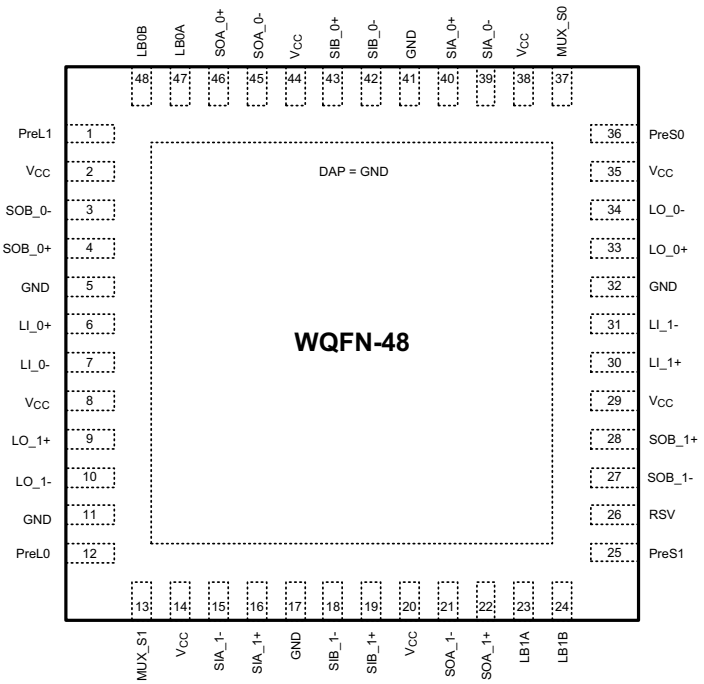
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (March 2013) to Revision J **Page**

- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Thermal Information* table, *Parameter Measurement Information* section, *Feature Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed thermal information per latest modeling results ... 5
- Changed board trace attenuation estimate, per recent measurement ... 15

5 Pin Configuration and Functions

NJU Package
48-Pin WQFN
Top View



Pin Functions

PIN		I/O[1]	DESCRIPTION[2]
NAME	NO.		
LINE-SIDE HIGH-SPEED DIFFERENTIAL I/Os			
LI_0+ LI_0−	6 7	I	Inverting and noninverting differential inputs of port_0 at the line side. LI_0+ and LI_0− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
LI_1+ LI_1−	30 31	I	Inverting and noninverting differential inputs of port_1 at the line side. LI_1+ and LI_1− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
LO_0+ LO_0−	33 34	O	Inverting and noninverting differential outputs of port_0 at the line side. LO_0+ and LO_0− have an internal 50 Ω connected to V_{CC}.
LO_1+ LO_1−	9 10	O	Inverting and noninverting differential outputs of port_1 at the line side. LO_1+ and LO_1− have an internal 50 Ω connected to V_{CC}.
SWITCH-SIDE HIGH SPEED-DIFFERENTIAL I/Os			
SIA_0+ SIA_0−	40 39	I	Inverting and noninverting differential inputs to the mux_0 at the switch_A side. SIA_0+ and SIA_0− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
SIA_1+ SIA_1−	16 15	I	Inverting and noninverting differential inputs to the mux_1 at the switch_A side. SIA_1+ and SIA_1− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
SIB_0+ SIB_0−	43 42	I	Inverting and noninverting differential inputs to the mux_0 at the switch_B side. SIB_0+ and SIB_0− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
SIB_1+ SIB_1−	19 18	I	Inverting and noninverting differential inputs to the mux_1 at the switch_B side. SIB_1+ and SIB_1− have an internal 50 Ω connected to an internal reference voltage. See Figure 7.
SOA_0+ SOA_0−	46 45	O	Inverting and noninverting differential outputs of mux_0 at the switch_A side. SOA_0+ and SOA_0− have an internal 50 Ω connected to V_{CC}.
SOA_1+ SOA_1−	22 21	O	Inverting and noninverting differential outputs of mux_1 at the switch_A side. SOA_1+ and SOA_1− have an internal 50 Ω connected to V_{CC}.

(1) I = Input, O = Output, P = Power
(2) All CML Inputs or Outputs must be AC coupled.

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION[2]
NAME	NO.		
SOB_0+ SOB_0−	4 3	O	Inverting and noninverting differential outputs of mux_0 at the switch_B side. SOB_0+ and SOB_0− have an internal 50 Ω connected to V_{CC}.
SOB_1+ SOB_1−	28 27	O	Inverting and noninverting differential outputs of mux_1 at the switch_B side. SOB_1+ and SOB_1− have an internal 50 Ω connected to V_{CC}.
CONTROL (3.3-V LVCMOS)			
LB0A	47	I	A logic low at LB0A enables the internal loopback path from SIA_0± to SOA_0±. LB0A is internally pulled high.
LB0B	48	I	A logic low at LB0B enables the internal loopback path from SIB_0± to SOB_0±. LB0B is internally pulled high.
LB1A	23	I	A logic low at LB1A enables the internal loopback path from SIA_1± to SOA_1±. LB1A is internally pulled high.
LB1B	24	I	A logic low at LB1B enables the internal loopback path from SIB_1± to SOB_1±. LB1B is internally pulled high.
MUX_S0	37	I	A logic low at MUX_S0 selects mux_0 to switch B. MUX_S0 is internally pulled high. Default state for mux_0 is switch A.
MUX_S1	13	I	A logic low at MUX_S1 selects mux_1 to switch B. MUX_S1 is internally pulled high. Default state for mux_1 is switch A.
PREL_0 PREL_1	12 1	I	PREL_0 and PREL_1 select the output pre-emphasis of the line side drivers (LO_0± and LO_1±). PREL_0 and PREL_1 are internally pulled high. See Table 3 for line side pre-emphasis levels.
PRES_0 PRES_1	36 25	I	PRES_0 and PRES_1 select the output pre-emphasis of the switch side drivers (SOA_0±, SOB_0±, SOA_1± and SOB_1±). PRES_0 and PRES_1 are internally pulled high. See Table 4 for switch side pre-emphasis levels.
RSV	26	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.
POWER			
GND	5, 11, 17, 32, 41	P	Ground reference. Each ground pin must be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	Die Attach Pad (DAP) is the metal contact at the bottom side, located at the center of the WQFN-48 package. It must be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.
V_{CC}	2, 8, 14, 20, 29, 35, 38, 44	P	V_{CC} = 3.3 V ± 5%. Each V_{CC} pin must be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin. TI recommends to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)(2)

	MIN	MAX	UNIT
Supply voltage (V_{CC})	−0.3	4	V
CMOS/TTL input voltage	−0.3	V_{CC} + 0.3	V
CML input/output voltage	−0.3	V_{CC} + 0.3	V
Junction temperature		125	°C
Lead temperature (soldering, 4 sec)		260	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), 1.5 kΩ, 100 pF, per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Machine model (MM), per JEDEC specification JESD22-A115-A	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} – GND)	3.135	3.3	3.465	V
Supply noise amplitude (10 Hz to 2 GHz)			20	mV_{PP}
Ambient temperature	0		85	°C
Case temperature			100	°C

6.4 Thermal Information

THERMAL METRIC(1)		DS40MB200 NJU (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
LVCMOS DC SPECIFICATIONS							
V_{IH}	High level input voltage			2		V_{CC} + 0.3	V
V_{IL}	Low level input voltage			−0.3		0.8	V
I_{IH}	High level input current	V_{IN} = V_{CC}		−10		10	µA
I_{IL}	Low level input current	V_{IN} = GND		75	94	124	µA
R_{PU}	Pull-high resistance				35		kΩ
RECEIVER SPECIFICATIONS							
V_{ID}	Differential input voltage range	AC-coupled differential signal. This parameter is not production tested.	Below 1.25 Gbps	100		1750	mV_{P-P}
			At 1.25 Gbps–3.125 Gbps	100		1560	
			Above 3.125 Gbps	100		1200	
V_{ICM}	Common mode voltage at receiver inputs	Measured at receiver inputs reference to ground.			1.3		V
R_{ITD}	Input differential termination	On-chip differential termination between IN+ or IN−.		84	100	116	Ω
DRIVER SPECIFICATIONS							
VODB	Output differential voltage swing without pre-emphasis	R_L = 100 Ω ±1% PRES_1 = PRES_0 = 0 PREL_1 = PREL_0 = 0 Driver pre-emphasis disabled. Running K28.7 pattern at 4 Gbps. See Figure 6 for test circuit.		1000	1200	1400	mV_{P-P}
V_{PE}	Output pre-emphasis voltage ratio 20 × log (VODPE / VODB)	R_L = 100 Ω ±1% Running K28.7 pattern at 4 Gbps(2) x = S for switch side pre-emphasis control x = L for line side pre-emphasis control See Figure 8 on waveform. See Figure 6 for test circuit.	PREx_[1:0] = 00		0		dB
			PREx_[1:0] = 01		−3		
			PREx_[1:0] = 10		−6		
			PREx_[1:0] = 11		−9		
t_{PE}	Pre-emphasis width(3)	Tested at −9-dB pre-emphasis level, PREx[1:0] = 11 x = S for switch side pre-emphasis control x = L for line side pre-emphasis control See Figure 3 on measurement condition.		125	200	250	ps
R_{OTSE}	Output termination	On-chip termination from OUT+ or OUT− to V_{CC}(4)		42	50	58	Ω
R_{OTD}	Output differential termination	On-chip differential termination between OUT+ and OUT−(4)			100		Ω
ΔR_{OTSE}	Mismatch in output termination resistors	Mismatch in output terminations at OUT+ and OUT−(4)				5%	
V_{OCM}	Output common mode voltage				2.7		V
POWER DISSIPATION							
P_D	Power dissipation	V_{DD} = 3.465 V All outputs terminated by 100 Ω ±1%. PREL_[1:0] = 0, PRES_[1:0] = 0 Running PRBS 2^7–1 pattern at 4 Gbps				1	W

(1) Typical parameters measured at V_{CC} = 3.3 V, T_A = 25°C. They are for reference purposes and are not production-tested.
(2) K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000} K28.5 pattern is a 20-bit repeating pattern of +K28.5 and –K28.5 code groups {110000 0101 001111 1010}
(3) Specified by design and characterization using statistical analysis.
(4) IN+ and IN− are generic names refer to one of the many pairs of complementary inputs of the DS40MB200. OUT+ and OUT− are generic names refer to one of the many pairs of the complimentary outputs of the DS40MB200. Differential input voltage V_{ID} is defined as |IN+–IN−|. Differential output voltage V_{OD} is defined as |OUT+–OUT−|.

Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
AC CHARACTERISTICS							
RJ	Device random jitter(5)(6)	See Figure 6 for test circuit. Alternating-1-0 pattern. Pre-emphasis disabled.	At 1.25 Gbps			2	ps_{rms}
			At 4 Gbps			2	
DJ	Device deterministic jitter(7)(6)	See Figure 6 for test circuit. Pre-emphasis disabled.	At 4 Gbps, PRBS7 pattern			30	ps_{p-p}
DR_{MAX}	Maximum data rate(6)	Tested with alternating-1-0 pattern		4			Gbps

(5) Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation sqrt ($RJ_{OUT}^2 - RJ_{IN}^2$), where RJ_{OUT} is the random jitter measured at the output of the device in ps_{rms}, RJ_{IN} is the random jitter of the pattern generator driving the device.
(6) Specified by design and characterization using statistical analysis.
(7) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{OUT} - DJ_{IN}$), where DJ_{OUT} is the peak-to-peak deterministic jitter measured at the output of the device in ps_{p-p}, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_R	Differential low-to-high transition time	Measured with a clock-like pattern at 100 MHz, between 20% and 80% of the differential output voltage. Pre-emphasis disabled. Transition time is measured with fixture as shown in Figure 6, adjusted to reflect the transition time at the output pins.		80		ps
t_F	Differential high-to-low transition time			80		ps
t_{PLH}	Differential low-to-high propagation delay	Measured at 50% differential voltage from input to output.		0.5	2	ns
t_{PHL}	Differential high-to-low propagation delay			0.5	2	ns
t_{SKP}	Pulse skew(2)	$\lvert t_{PHL} - t_{PLH} \rvert$			20	ps
t_{SKO}	Output skew(3)(2)	Difference in propagation delay among data paths in the same device.			200	ps
t_{SKPP}	Part-to-part skew(2)	Difference in propagation delay between the same output from devices operating under identical condition.			500	ps
t_{SM}	MUX switch time	Measured from V_{IH} or V_{IL} of the mux-control or loopback control to 50% of the valid differential output.		1.8	6	ns

(1) Typical parameters measured at V_{CC} = 3.3 V, T_A = 25°C. They are for reference purposes and are not production-tested.
(2) Specified by design and characterization using statistical analysis.
(3) t_{SKO} is the magnitude difference in the propagation delays among data paths between switch A and switch B of the same port and similar data paths between port 0 and port 1. An example is the output skew among data paths from SIA_0± to LO_0±, SIB_0± to LO_0±, SIA_1± to LO_1± and SIB_1± to LO_1±. Another example is the output skew among data paths from LI_0± to SOA_0±, LI_0± to SOB_0±, LI_1± to SOA_1± and LI_1± to SOB_1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths between port 0 and port 1. An example is the output skew among data paths SIA_0± to SOA_0±, SIB_0± to SOB_0±, SIA_1± to SOA_1± and SIB_1± to SOB_1±.

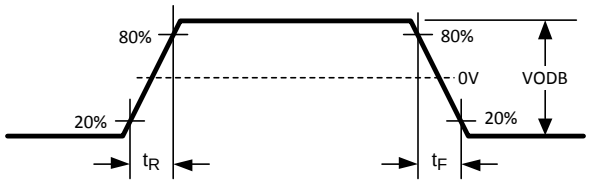


Figure 1. Driver Output Transition Time

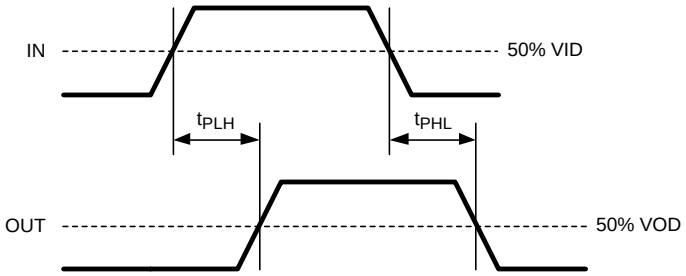


Figure 2. Propagation Delay From Input to Output

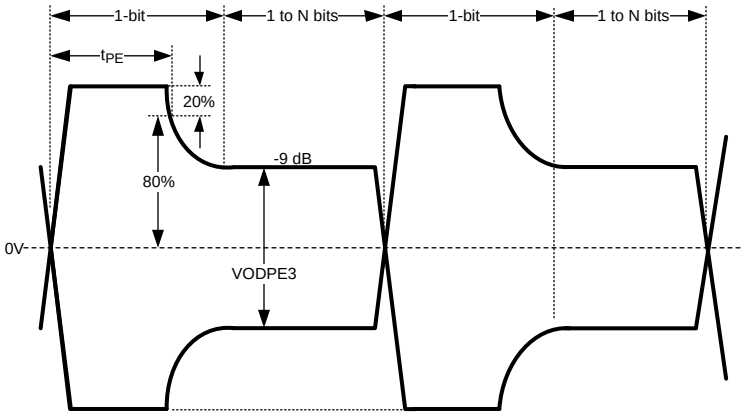


Figure 3. Test Condition for Output Pre-Emphasis Duration

6.7 Typical Characteristics

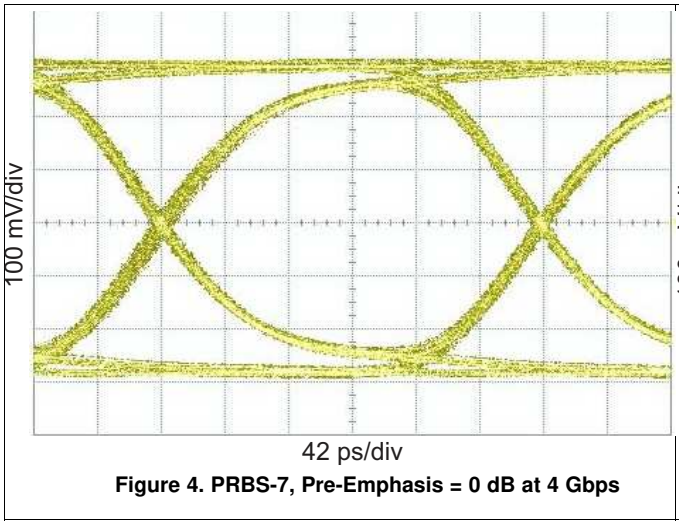


Figure 4. PRBS-7, Pre-Emphasis = 0 dB at 4 Gbps

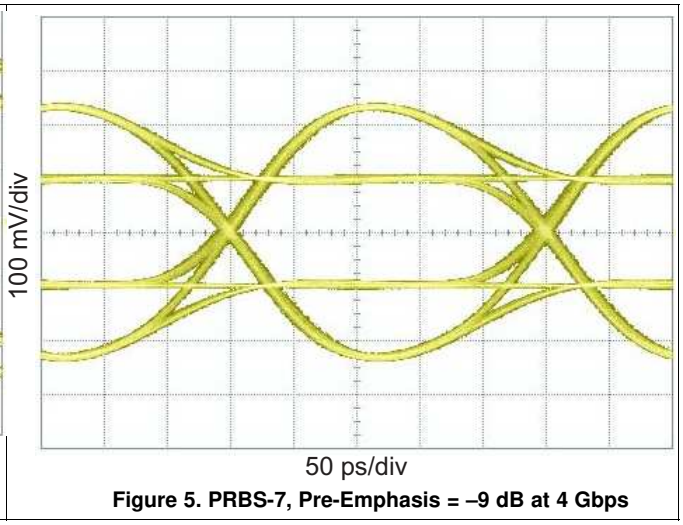


Figure 5. PRBS-7, Pre-Emphasis = –9 dB at 4 Gbps

7 Parameter Measurement Information

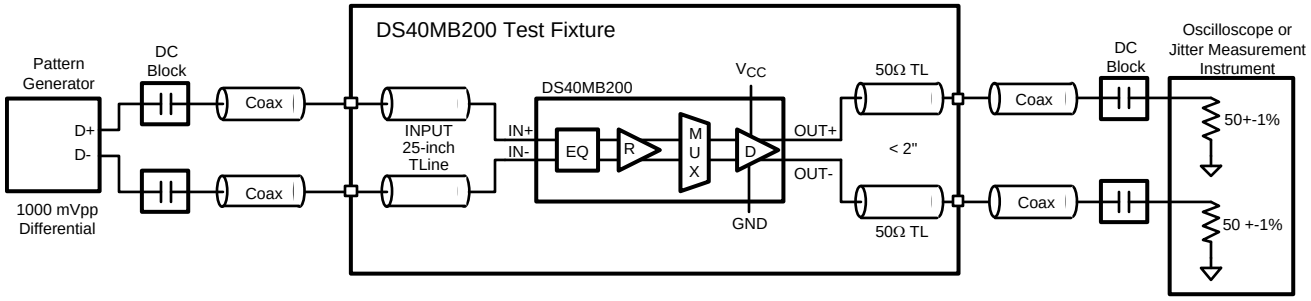


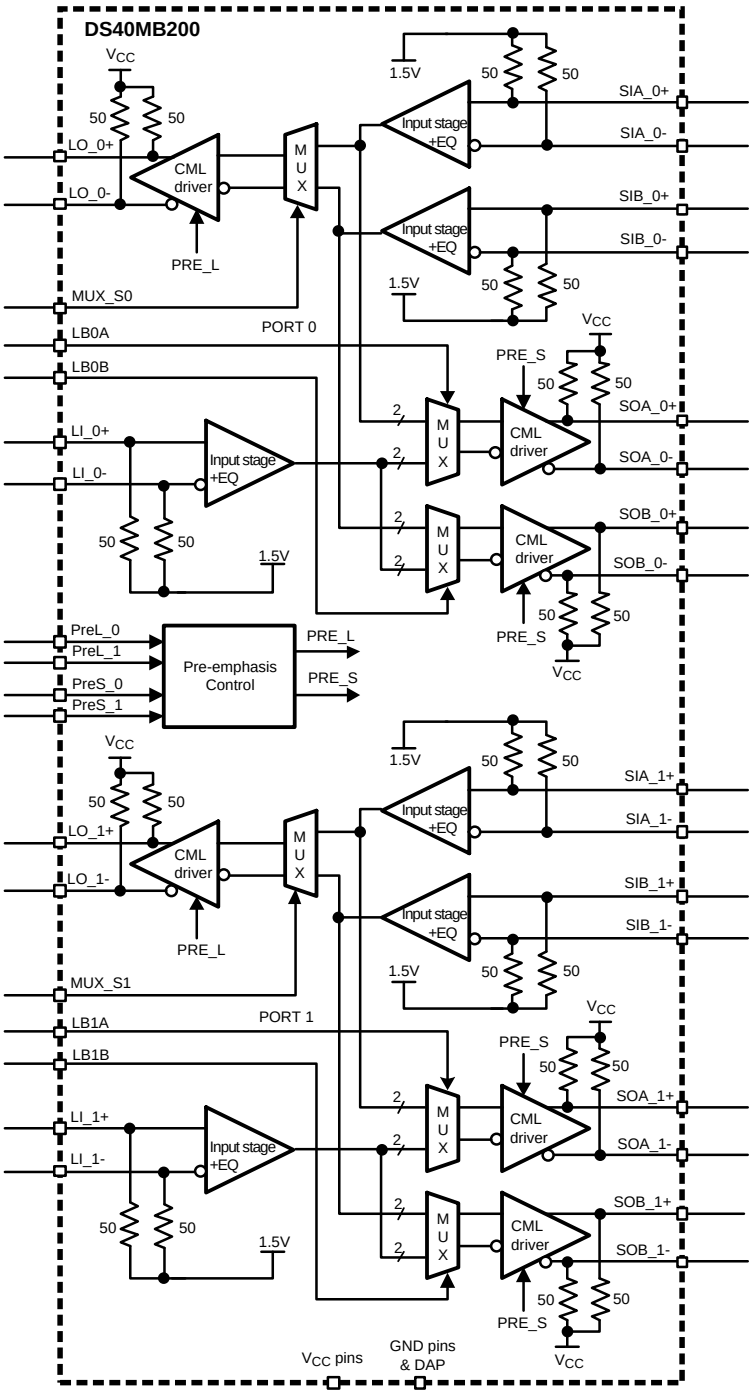
Figure 6. AC Test Circuit

8 Detailed Description

8.1 Overview

The DS40MB200 is a signal conditioning 2:1 multiplexer and 1:2 buffer designed to support port redundancy with encoded or scrambled data rates between 1 and 4 Gbps. The DS40MB200 provides fixed equalization at the receive input and pre-emphasis control on the output in order to support signal reach extension.

8.2 Functional Block Diagram



8.3 Feature Description

The DS40MB200 MUX buffer consists of several key blocks:

- CML Inputs and EQ
- Multiplexer and Loopback Control
- CML Drivers and Pre-Emphasis Control

8.3.1 CML Inputs and EQ

The high-speed inputs are self-biased to about 1.3 V at IN+ and IN- and are designed for AC coupling. See Figure 7 for details about the internal receiver input termination and bias circuit.

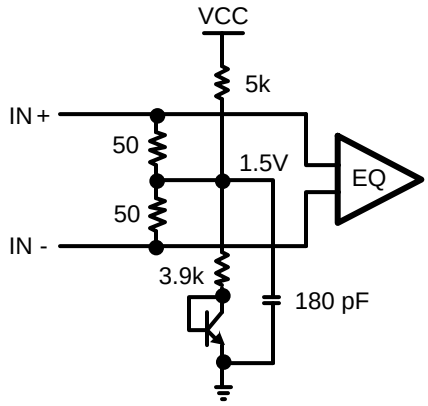


Figure 7. Receiver Input Termination and Bias Circuit

The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL, and CML. The DS40MB200 is not designed to operate with data rates below 1000 Mbps or with a DC bias applied to the CML inputs or outputs. Most high-speed links are encoded for DC balance and have been defined to include AC coupling capacitors, allowing the DS40MB200 to be inserted directly into the datapath without any limitation. The ideal AC-coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC-coupling capacitor value ranges between 100 and 1000 nF. Some specifications with scrambled data may require a larger capacitor for optimal performance. To reduce unwanted parasitic effects around and within the AC-coupling capacitor, a body size of 0402 is recommended. Figure 6 shows the AC-coupling capacitor placement in an AC test circuit.

Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB (at 2 GHz) of transmission loss from a short backplane trace (about 10 inches backplane).

8.3.2 Multiplexer and Loopback Control

Table 1 and Table 2 provide details about how to configure the DS40MB200 multiplexer and loopback settings.

Table 1. Logic Table for Multiplex Controls

PIN	PIN VALUE	MUX FUNCTION
MUX_S0	0	MUX_0 select switch_B input, SIB_0±.
	1 (default)	MUX_0 select switch_A input, SIA_0±.
MUX_S1	0	MUX_1 select switch_B input, SIB_1±.
	1 (default)	MUX_1 select switch_A input, SIA_0±.

Table 2. Logic Table for Loopback Controls

PIN	PIN VALUE	LOOPBACK FUNCTION
LB0A	0	Enable loopback from SIA_0± to SOA_0±.
	1 (default)	Normal mode. Loopback disabled.

Table 2. Logic Table for Loopback Controls (continued)

PIN	PIN VALUE	LOOPBACK FUNCTION
LB0B	0	Enable loopback from SIB_0± to SOB_0±.
	1 (default)	Normal mode. Loopback disabled.
LB1A	0	Enable loopback from SIA_1± to SOA_1±.
	1 (default)	Normal mode. Loopback disabled.
LB1B	0	Enable loopback from SIB_1± to SOB_1±.
	1 (default)	Normal mode. Loopback disabled.

8.3.3 CML Drivers and Pre-Emphasis Control

The output driver has pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane and minimize the deterministic jitter caused by the amplitude disparity. The DS40MB200 provides four steps of user-selectable pre-emphasis ranging from 0, –3, –6 and –9 dB to handle different lengths of backplane. Figure 8 shows a driver pre-emphasis waveform. The pre-emphasis duration is 200 ps nominal, corresponding to 0.8 unit intervals (UI) at 4Gbps. The pre-emphasis levels of switch-side and line-side can be individually programmed.

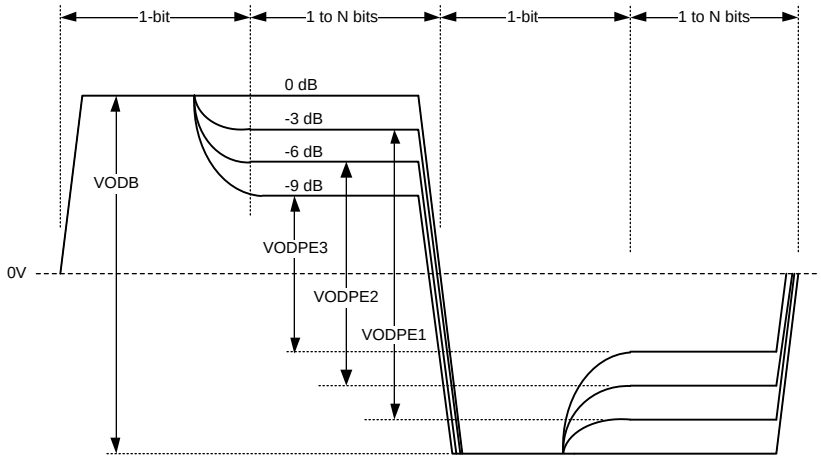


Figure 8. Driver Pre-Emphasis Differential Waveform (Showing All 4 Pre-Emphasis Steps)

Table 3. Line-Side Pre-Emphasis Controls

PreL_[1:0]	PRE-EMPHASIS LEVEL IN mV_{PP} (VODB)	DE-EMPHASIS LEVEL IN mV_{PP} (VODPE)	PRE-EMPHASIS IN dB (VODPE/VODB)	TYPICAL FR4 BOARD TRACE
0 0	1200	1200	0	10 inches
0 1	1200	850	−3	20 inches
1 0	1200	600	−6	30 inches
1 1 (default)	1200	426	−9	40 inches

Table 4. Switch-Side Pre-Emphasis Controls

PreS_[1:0]	PRE-EMPHASIS LEVEL IN mV_{PP} (VODB)	DE-EMPHASIS LEVEL IN mV_{PP} (VODPE)	PRE-EMPHASIS IN dB (VODPE/VODB)	TYPICAL FR4 BOARD TRACE
0 0	1200	1200	0	10 inches
0 1	1200	850	−3	20 inches
1 0	1200	600	−6	30 inches
1 1 (default)	1200	426	−9	40 inches

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS40MB200 is a 2:1 MUX and 1:2 buffer that equalizes input data up to 4 Gbps and provides transmit pre-emphasis controls to improve overall signal reach. As a MUX buffer, the DS40MB200 is ideal for designs where there is a need for port sharing or redundancy as well as on-the-fly reorganization of routes and data connections.

9.2 Typical Application

A typical application for the DS40MB200 is shown in Figure 9 and Figure 10.

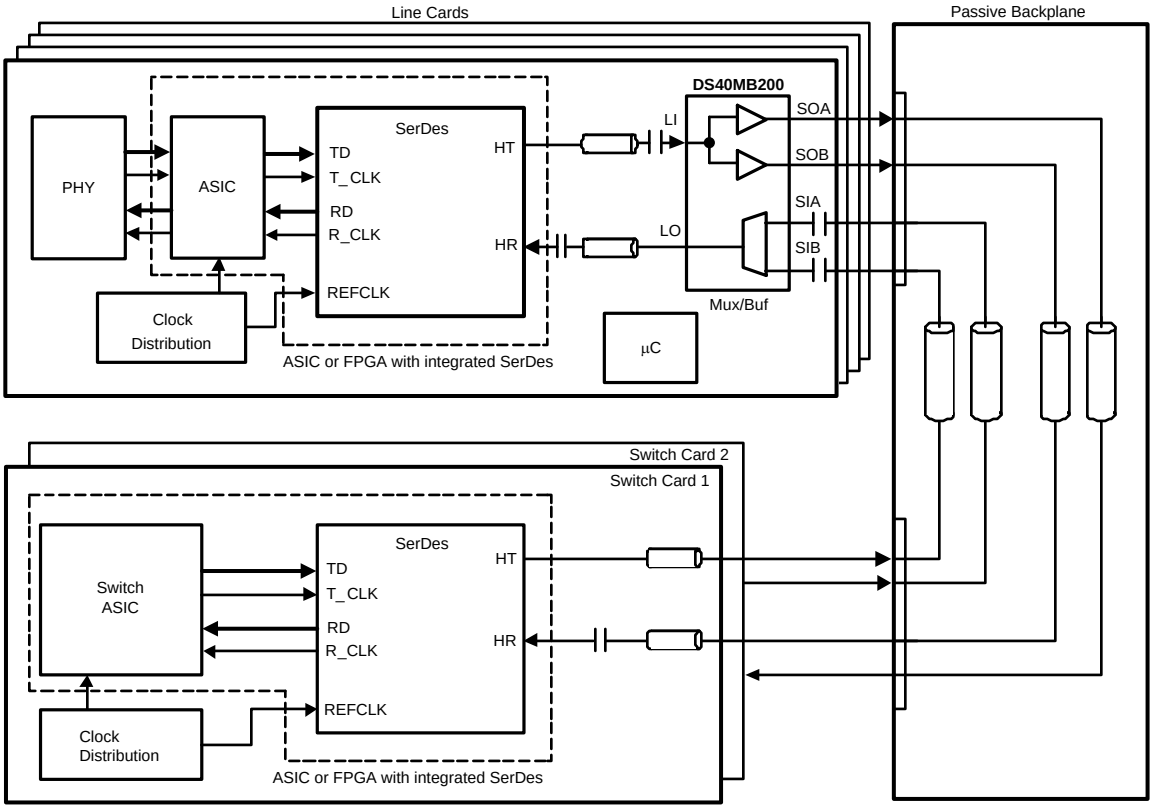


Figure 9. System Diagram (Showing Data Paths of Port 0)

Typical Application (continued)

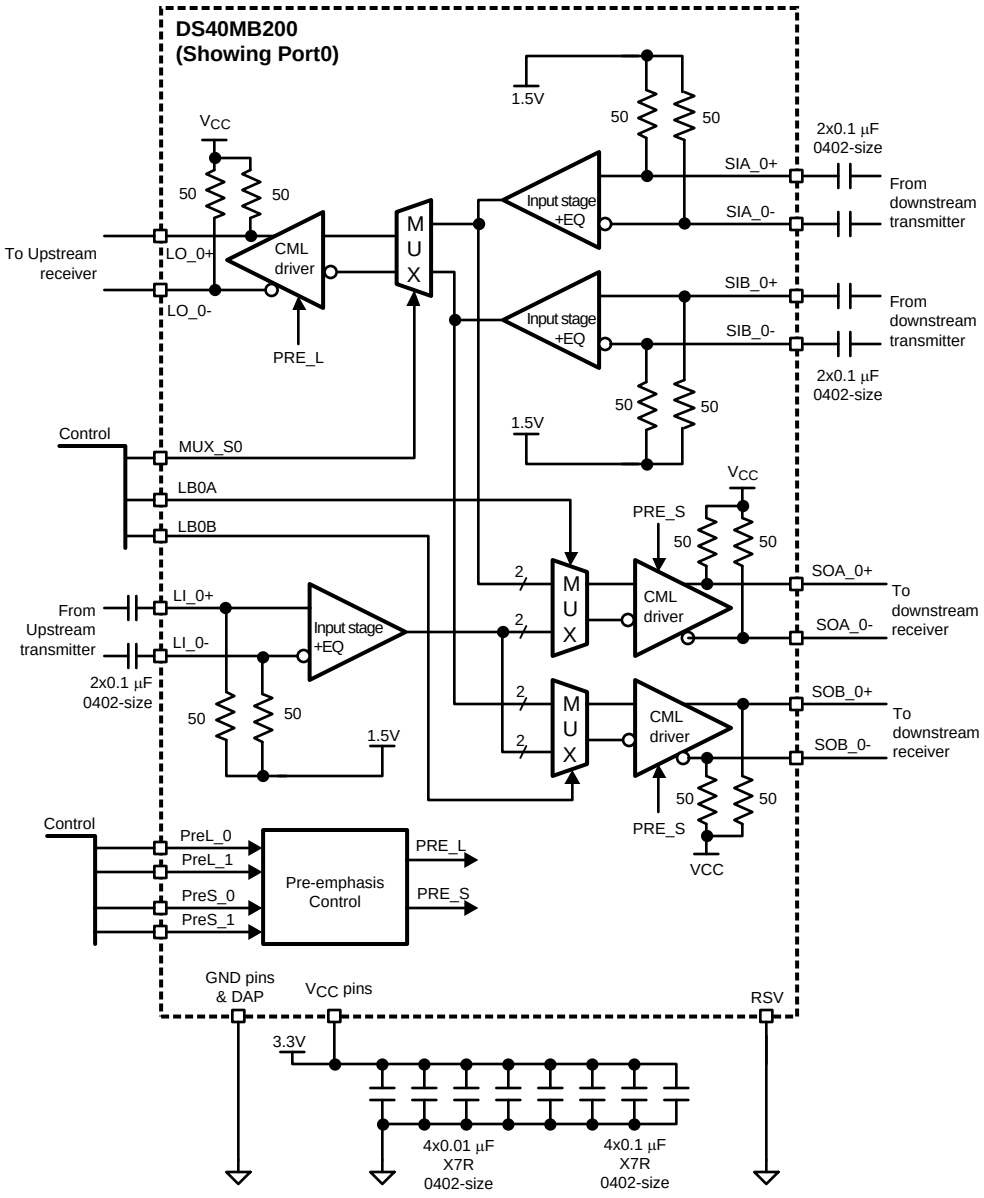


Figure 10. DS40MB200 Connection Block Diagram (Showing Data Paths of Port 0)

9.2.1 Design Requirements

In a typical design, the DS40MB200 equalizes a short backplane trace on its input, followed by a longer trace at the DS40MB200 output. In this application example, a 25-inch FR4 coupled micro-strip board trace is used in place of the short backplane link. A block diagram of this example is shown in Figure 11.

Typical Application (continued)

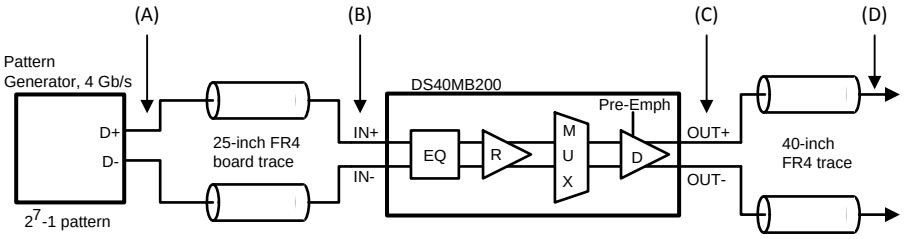


Figure 11. Block Diagram of DS40MB200 Application Example

The 25-inch microstrip board trace has approximately 6 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the transmission loss of the short backplane transmission line. The 25-inch microstrip is connected between the pattern generator and the differential inputs of the DS40MB200 for AC measurements.

Table 5. Input Trace Parameters

TRACE LENGTH	FINISHED TRACE WIDTH W	SEPARATION BETWEEN TRACES	DIELECTRIC HEIGHT H	DIELECTRIC CONSTANT ε_R	LOSS TANGENT
25 inches	8.5 mil	11.5 mil	6 mil	3.8	0.022

The length of the output trace may vary based on system requirements. In this example, a 40-inch FR4 trace with similar trace width, separation, and dielectric characteristics is placed at the DS40MB200 output.

As with any high-speed design, there are many factors which influence the overall performance. Following is a list of critical areas for consideration and study during design.

- Use 100-Ω impedance traces. Generally, these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

9.2.2 Detailed Design Procedure

For optimal design, the DS40MB200 must be configured to route incoming data correctly as well as to provide the best signal quality. The following design procedures must be observed:

1. The DS40MB200 must be configured to provide the correct multiplexer and buffer routes in order to satisfy system requirements. In order to set the appropriate multiplexer control settings, refer to Table 1. To configure the buffer control settings, refer to Table 2. For example, consider the case where the designer wishes to route the input from Switch Card A (SIA0_0±) to the output for the line card (LO_0±). To accomplish this, set MUX_S0 = 1 (select SIA0_0±). For the other direction from line card output to switch card, set LB0A = 1 and LB0B = 1 so that the input from the line-card is buffered to both Switch Card A (SOA_0±) and Switch Card B (SOB_0±).
2. The DS40MB200 is designed to be placed at an offset location with respect to the overall channel attenuation. To optimize performance, the multiplexer buffer transmit pre-emphasis can be tuned to extend the trace length reach while also recovering a solid eye opening. To tune transmit pre-emphasis on either the line card side or switch card side, refer to Table 3 and Table 4 for recommended pre-emphasis control settings according to the length of FR4 board trace connected at the DS40MB200 output. For example, if 40 inches of FR4 trace is connected to the switch card output, set PreS_[1:0] = (1, 1) for VOD = 1200 mVpp and –9 dB of transmit pre-emphasis.

9.2.3 Application Curves

Figure 12 through Figure 17 show how the signal integrity varies at different places in the data path. These measured locations can be referenced back to the labeled points provided in Figure 11.

- Point (A): Output signal of source pattern generator
- Point (B): Input to DS40MB200 after 25 inches of FR4 trace from source
- Point (C): Output of DS40MB200 driver
- Point (D): Signal after 40 inches of FR4 trace from DS40MB200 driver

The source signal is a PRBS-7 pattern at 4 Gbps. For the long output traces, the eye after 40 inches of output FR4 trace is significantly improved by adding –9 dB of pre-emphasis.

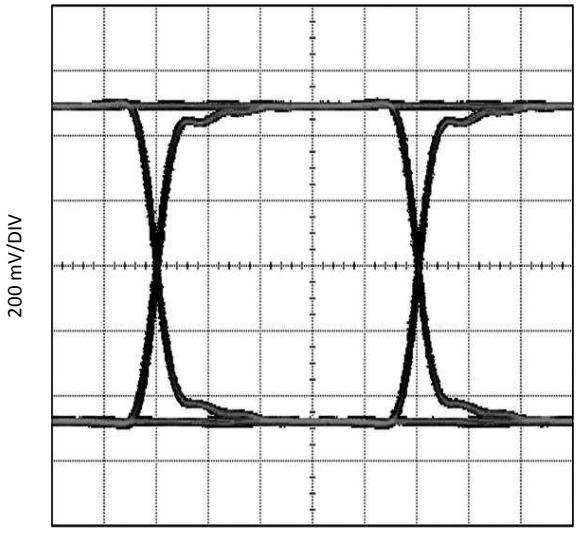


Figure 12. Eye Measured at Point (A)

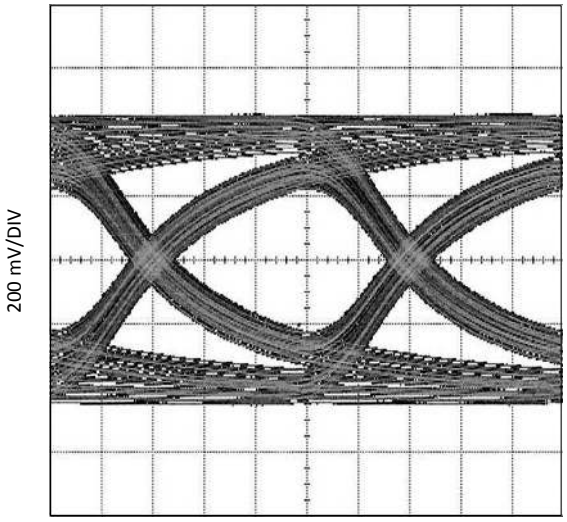


Figure 13. Eye Measured at Point (B)

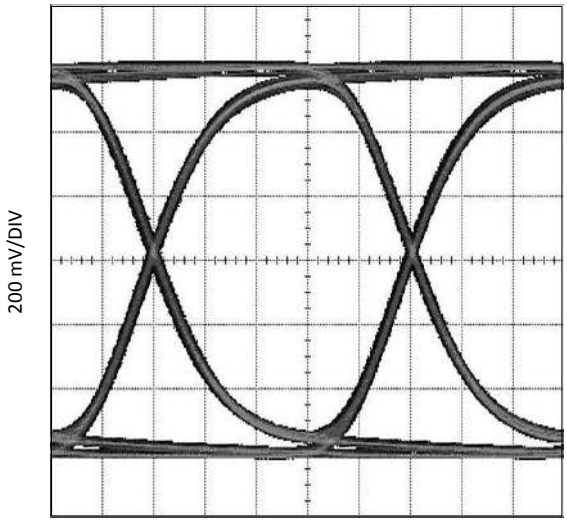


Figure 14. Eye Measured at Point (C), Pre-Emph = 0 dB

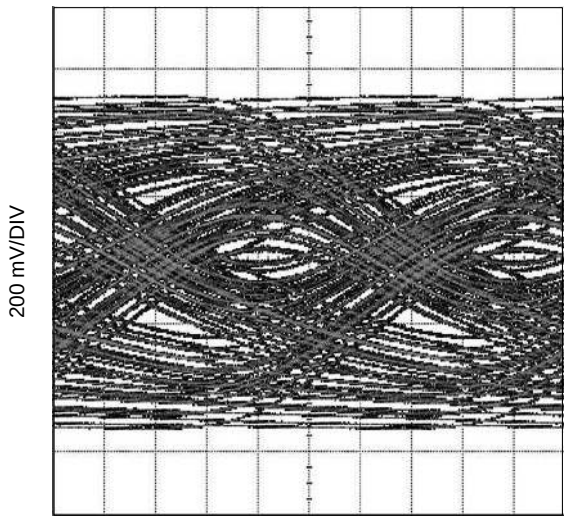


Figure 15. Eye Measured at Point (D), Pre-Emph = 0 dB

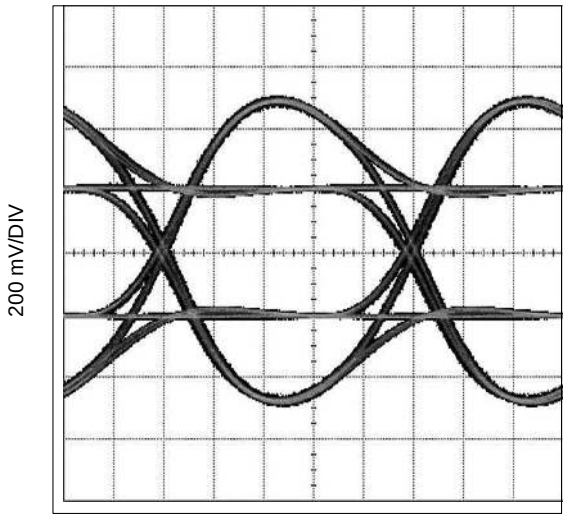


Figure 16. Eye Measured at Point (C), Pre-Emph = –9 dB

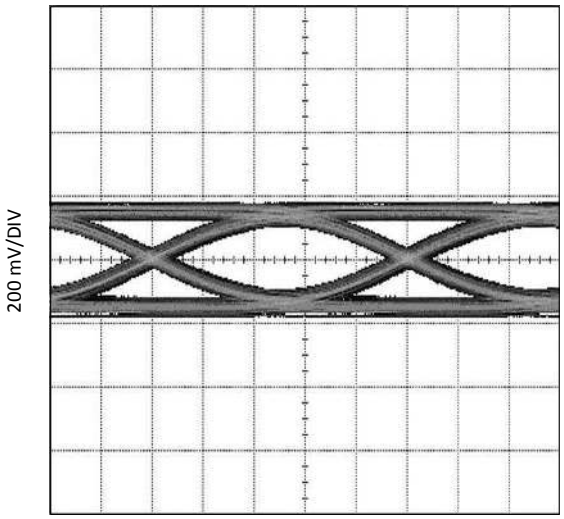


Figure 17. Eye Measured at Point (D), Pre-Emph = –9 dB

10 Power Supply Recommendations

The supply (V_{CC}) and ground (GND) pins must be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric must be minimized so that the V_{CC} and GND planes create a low inductance supply with distributed capacitance. Careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01-µF or 0.1-µF bypass capacitor must be connected to each V_{CC} pin such that the capacitor is placed as close to the V_{CC} pins as possible. Smaller body-size capacitors, such as 0402 body size, can help facilitate proper component placement. Refer to the V_{CC} pin connections in Figure 10 for further details.

11 Layout

11.1 Layout Guidelines

Use at least a four-layer board with a power and ground plane. Closely coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus will be rejected by the receivers. Information on the WQFN style package is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

11.2 Layout Examples

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Figure 18. A layout example for the DS40MB200 DAP is shown in Figure 19, where 16 stencil openings are used for the DAP alongside nine vias to GND.

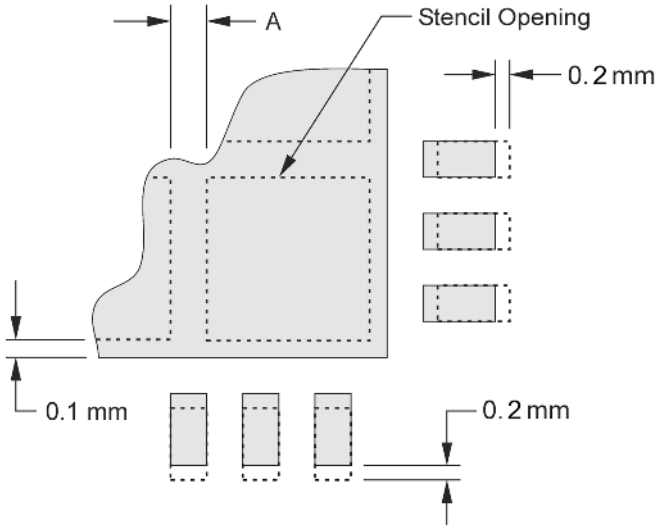


Figure 18. No Pullback WQFN, Single Row Reference Diagram

Table 6. No Pullback WQFN Stencil Aperture Summary for DS40MB200

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS40MB200	48	SQA48A	0.25 × 0.6	0.5	5.1 × 5.1	0.25 × 0.7	1.1 × 1.1	16	0.2

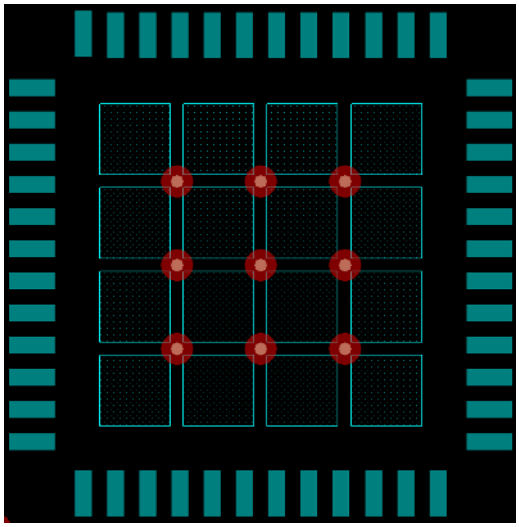


Figure 19. 48-Pin WQFN Stencil Example of Via and Opening Placement

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

AN-1187 Leadless Leadframe Package (LLP), SNOA401

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS40MB200SQ/NOPB	ACTIVE	WQFN	NJU	48	250	RoHS & Green	SN	Level-3-260C-168 HR	0 to 85	40MB200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

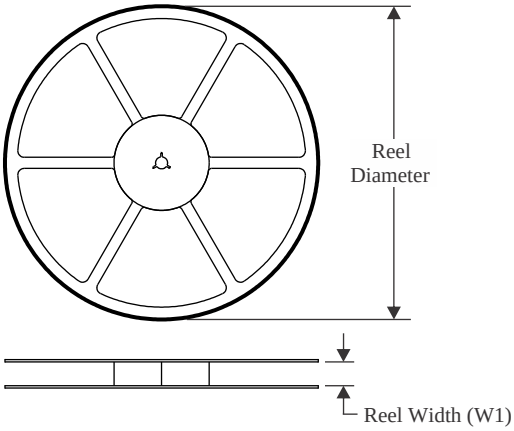
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

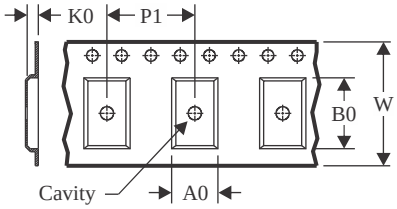
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

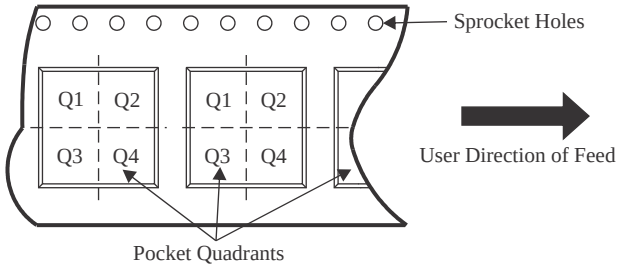


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

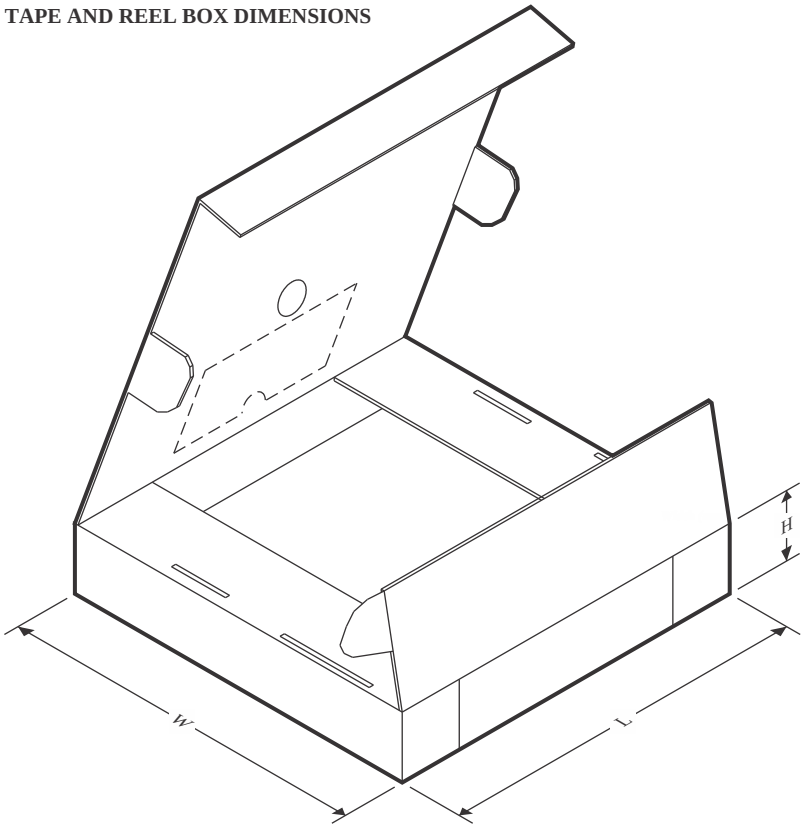
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS40MB200SQ/NOPB	WQFN	NJU	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

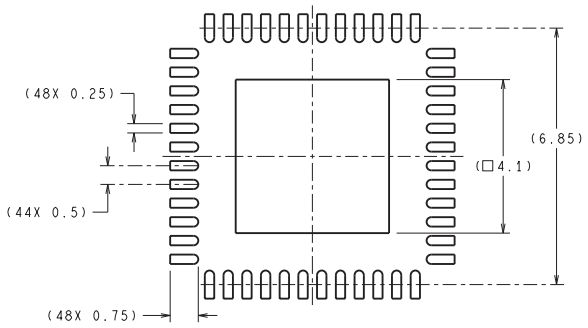
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

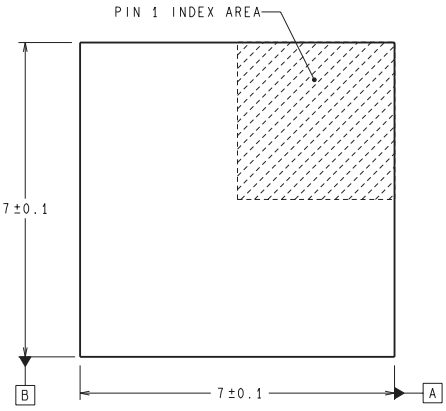
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS40MB200SQ/NOPB	WQFN	NJU	48	250	208.0	191.0	35.0

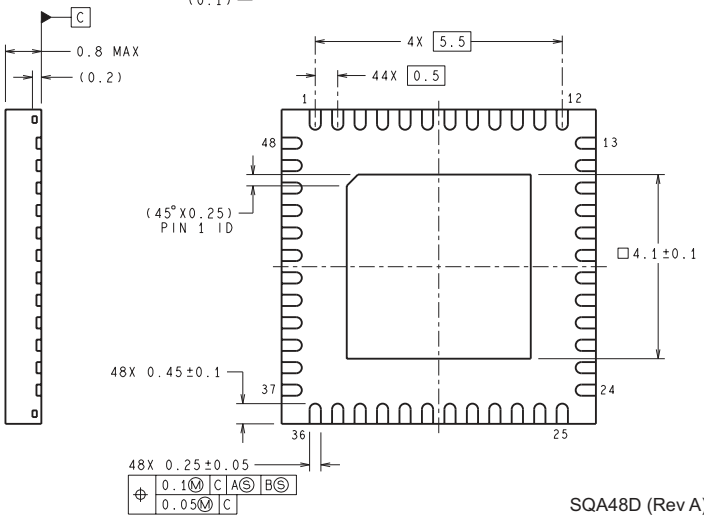
NJU0048D



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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