



SLPS241A – DECEMBER 2009 – REVISED JANUARY 2010

DualCool[™] N-Channel NexFET[™] Power MOSFETs

Check for Samples: CSD16322Q5C

FEATURES

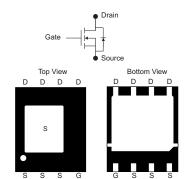
- DualCool[™] Package SON 5×6mm
- Optimized for Two Sided Cooling
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant and Halogen Free

APPLICATIONS

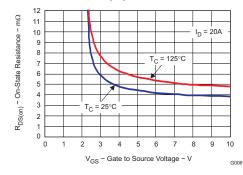
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous or Control FET Applications

DESCRIPTION

The NexFET[™] power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.







PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	25		V
Qg	Gate Charge Total (4.5V)	6.8		nC
Q _{gd}	Gate Charge Gate to Drain	1.3		nC
	Drain to Source On Resistance	$V_{GS} = 3V$	5.4	mΩ
R _{DS(on)}		$V_{GS} = 4.5V$	4.6	mΩ
		$V_{GS} = 8V$	3.9	mΩ
V _{GS(th)}	Threshold Voltage	1.1		V

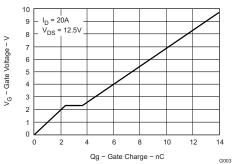
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16322Q5C	SON 5x6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 2$	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage		V
	Continuous Drain Current, T _C = 25°C	97	А
ID	Continuous Drain Current ⁽¹⁾	21	А
I _{DM}	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$		А
PD	Power Dissipation ⁽¹⁾	3.1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse $I_D = 50A$, L = 0.1mH, $R_G = 25\Omega$	125	mJ

- (1) $R_{\theta JA} = 39^{\circ} \text{C/W}$ on 1-inch^2 Cu, (2-oz.) on a 0.06" thick FR4 PCB.
- (2) Pulse duration $\leq 300 \mu s$, duty cycle $\leq 2\%$



Gate Charge

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT
Static Cl	haracteristics		i		
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250 \mu A$	25		V
I _{DSS}	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = 20V$		1	μΑ
I _{GSS}	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = +10/-8V$		100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.9 1.1	1.4	V
		$V_{GS} = 3V, I_{DS} = 20A$	5.4	7	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _{DS} = 20A	4.6	5.8	mΩ
		V _{GS} = 8V, I _{DS} = 20A	3.9	5	mΩ
9 _{fs}	Transconductance	V _{DS} = 15V, I _{DS} = 20A	106		S
Dynamic	C Characteristics		•	•	
C _{iss}	Input Capacitance		1050	1365	pF
C _{oss}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V,$ f = 1MHz	740	950	pF
C _{rss}	Reverse Transfer Capacitance		55	70	pF
R_G	Series Gate Resistance		1.1	2.2	Ω
Qg	Gate Charge Total (4.5V)		6.8	9.7	nC
Q _{gd}	Gate Charge – Gate to Drain	V _{DS} = 12.5V,	1.3		nC
Q _{gs}	Gate Charge – Gate to Source	$I_{DS} = 20A$	2.4		nC
Q _{g(th)}	Gate Charge at Vth		1.3		nC
Q _{oss}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$	17		nC
t _{d(on)}	Turn On Delay Time		6.1		ns
t _r	Rise Time	$V_{DS} = 12.5V, V_{GS} = 4.5V,$	10.7		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 20A, R_G = 2\Omega$	12.3		ns
t _f	Fall Time		3.7		ns
Diode C	haracteristics		·		
V _{SD}	Diode Forward Voltage	$I_{DS} = 20A, V_{GS} = 0V$	0.8	1	V
Q _{rr}	Reverse Recovery Charge		19		nC
t _{rr}	Reverse Recovery Time	$V_{DD} = 13V, I_F = 20A, di/dt = 300A/\mu s$	21		ns

THERMAL CHARACTERISTICS

($T_A = 25^{\circ}C$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) ⁽¹⁾			3.5	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom drain) ⁽¹⁾			2.4	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	°C/W

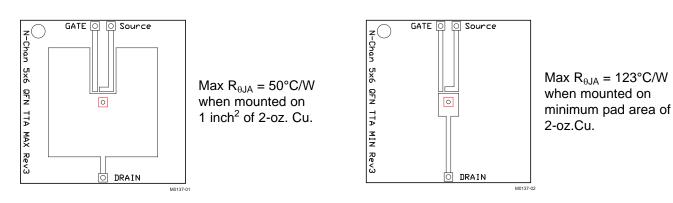
 $R_{\theta JC}$ is determined with the device mounted on a 1-inch² 2-oz. Cu pad on a 1.5 x 1.5-inch 0.06-inch thick FR4 board. $R_{\theta JC}$ is specified (1) by design, whereas $R_{\theta CA}$ is determined by the user's board design. Device mounted on FR4 material with 1-inch² of 2-oz. Cu.

(2)



CSD16322Q5C

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TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

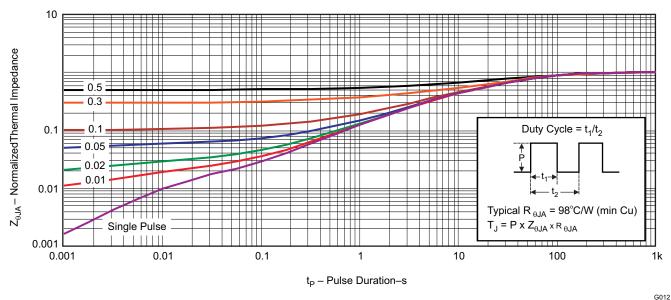


Figure 1. Transient Thermal Impedance

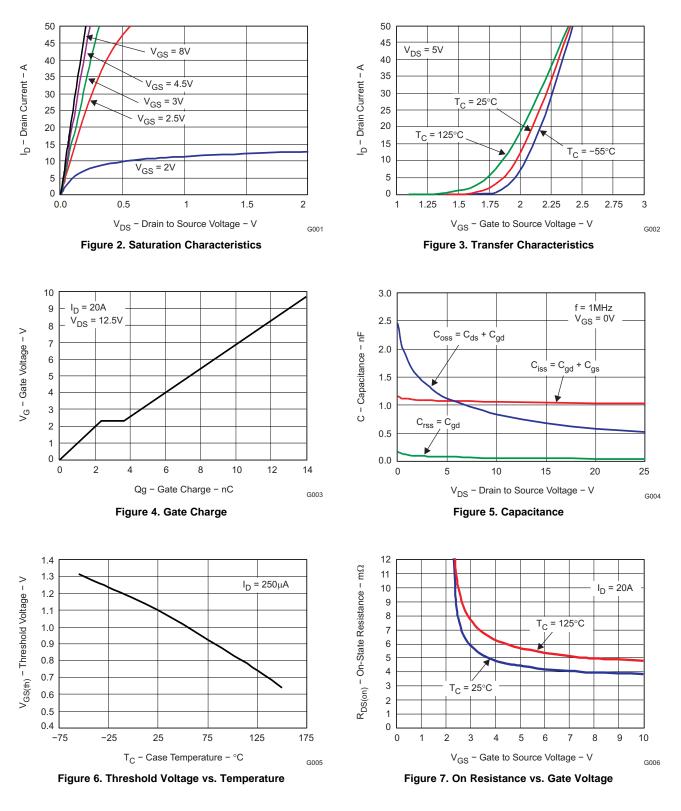
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TEXAS INSTRUMENTS

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TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$

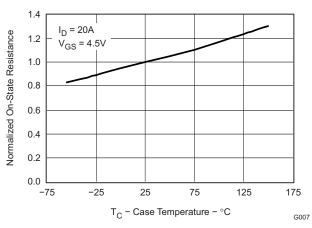




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TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$





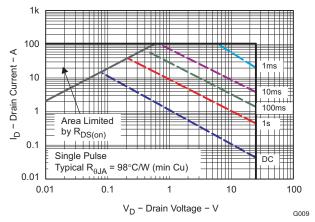


Figure 10. Maximum Safe Operating Area

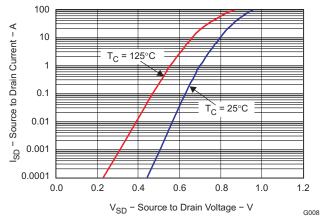


Figure 9. Typical Diode Forward Voltage

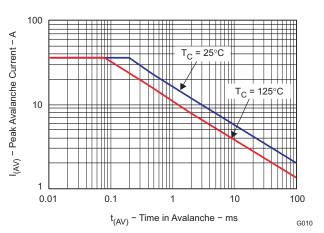
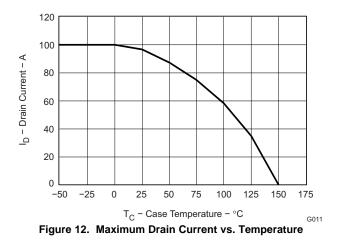


Figure 11. Single Pulse Unclamped Inductive Switching



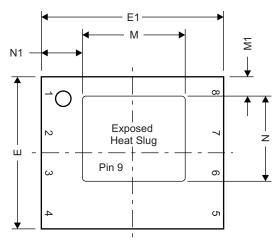
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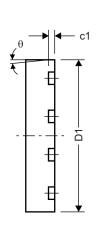
Q5C Package Dimensions

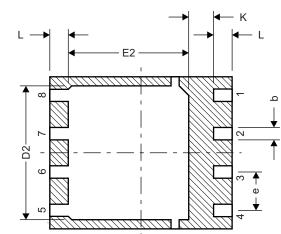


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MECHANICAL DATA



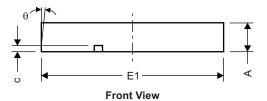




Top View

Side View

Bottom View



DualCool [™] Pinout			
Pin# Label			
1, 2, 3, 9 Source			
4	Gate		
5, 6, 7, 8	Drain		

M0162-01

DIM	MILLIN	IETERS	INC	HES
DIW	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
С	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
е	1.27	TYP	0.0)50
L	0.510	0.710	0.020	0.028
θ	-	-	-	-
К	0.760	-	0.030	-
М	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
Ν	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056

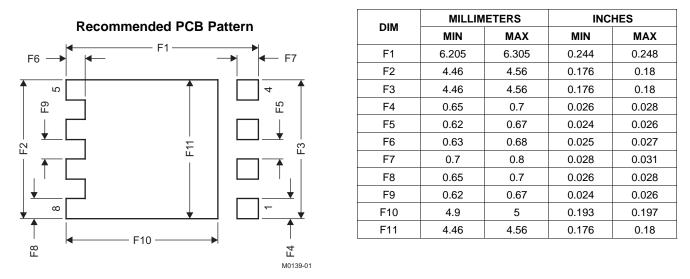
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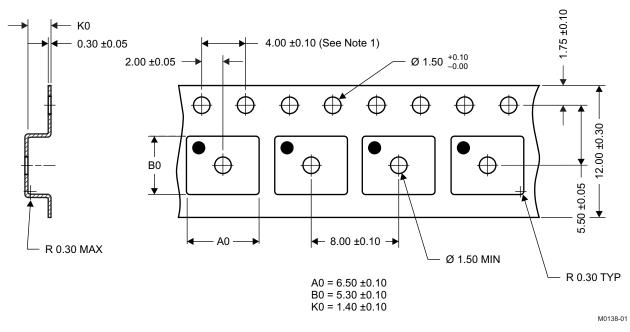


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For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q5C Tape and Reel Information



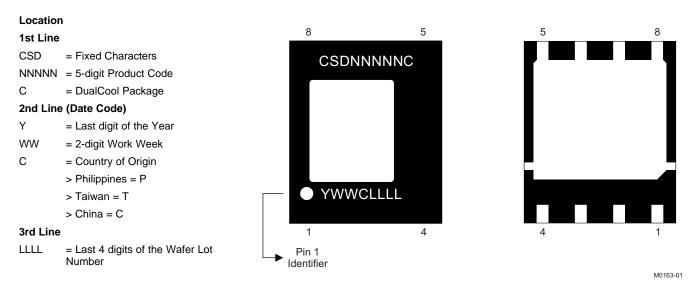
Notes:

- 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm, unless otherwise specified.
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- 6. MSL1 260°C (IR and convection) PbF reflow compatible

TEXAS INSTRUMENTS

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Package Marking Information

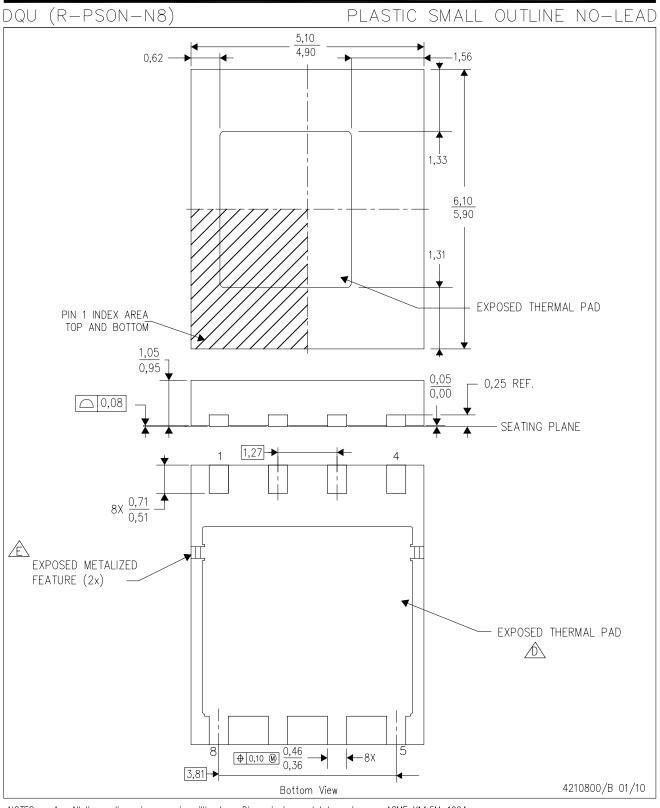


REVISION HISTORY

Changes from Original (December 2009) to Revision A				
•	Changed the labels on the Bottom View pinout image	. 1		
•	Changed the Mechanical Data dimensions table. Added dimensions for M, M1, N and N1	. 6		

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MECHANICAL DATA



NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. Α.

- B. This drawing is subject to change without notice.
- C. Dual Cool No-Lead (SON) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance.

Â Metalized features are supplier options and may not be on the package.



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