

4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY
Product Summary

V_{BR} (min)	I_{PP} (max)	C_{I/O} (typ)
6.2V	6A	0.65pF

Description

This new generation TVS is designed to protect sensitive electronics from the damage due to ESD. The combination of low capacitance and high ESD surge capability makes it ideal for use in high speed ports such as USB 2.0, IEEE1394, HDMI, Laptop and Personal Computers, Flat Panel Displays, Video Graphics Displays, SIM Ports.

Applications

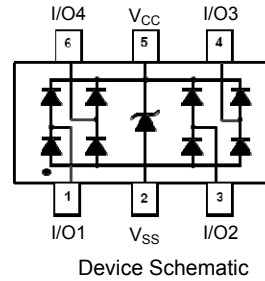
- USB 2.0
- IEEE1394
- SIM Ports
- Portable Electronics
- Computers and Peripheral

Features

- Low Clamping Voltage, I/O to V_{SS}
Typical 9V at 10A 100ns, TLP
Typical 7.7V at 6A 8μs/20μs
- IEC 61000-4-2 (ESD): Air – +27/-19kV, Contact – ±16kV
- IEC 61000-4-4 (EFT): Level-4
- 4 Channels of ESD Protection
- TLP Dynamic Resistance: 0.25Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**

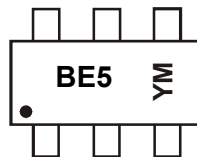
Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Copper leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 ③
- Weight: 0.013 grams (approximate)


Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT1042-04TS-7	Standard	BE5	7	8	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
 3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


BE5= Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2013	2014	2015	2016	2017	2018
Code	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	$I_{PP_I/O}$	± 6	A	I/O to V_{SS} , 8/20 μs
Peak Pulse Power, per IEC 61000-4-5	$P_{PP_I/O}$	55	W	I/O to V_{SS} , 8/20 μs
Operating Voltage (DC)	V_{DC}	5.5	V	I/O to V_{SS}
ESD Protection – Contact Discharge, per IEC 61000-4-2	$V_{ESD_I/O}$	± 16	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	$V_{ESD_I/O}$	+27/-19	kV	I/O to V_{SS}
Operating Temperature	T_{OP}	-55 to +85	$^\circ\text{C}$	–
Storage Temperature	T_{STG}	-55 to +150	$^\circ\text{C}$	–

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	417	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	–	–	5.0	V	V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_R(V_{CC}$ to $V_{SS})$	–	–	1.0	μA	$V_R = V_{RWM} = 5\text{V}$, V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_R(I/O$ to $V_{SS})$	–	–	0.5	μA	$V_R = V_{RWM} = 5\text{V}$, any I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	6.2	–	–	V	$I_R = 1\text{mA}$, V_{CC} to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.8	–	V	$I_F = -15\text{mA}$, V_{CC} to V_{SS}
Reverse Clamping Voltage(Note 7)	$V_{C_V_{CC}}$	–	6.3	–	V	$I_{PP} = 9\text{A}$, V_{CC} to V_{SS} , 8/20 μs
	$V_{C_I/O}$	–	7.7	9	V	$I_{PP} = 6\text{A}$, I/O to V_{SS} , 8/20 μs
ESD Clamping Voltage	$V_{ESD_V_{CC}}$	–	6.8	–	V	TLP, 10A, $t_p = 100\text{ ns}$, V_{CC} to V_{SS} , per Fig. 8
	$V_{ESD_I/O}$	–	9	–	V	TLP, 10A, $t_p = 100\text{ ns}$, I/O to V_{SS} , per Fig. 8
Dynamic Resistance	$R_{DIF_V_{CC}}$	–	0.1	–	Ω	TLP, 10A, $t_p = 100\text{ ns}$, V_{CC} to V_{SS}
	$R_{DIF_I/O}$	–	0.25	–	Ω	TLP, 10A, $t_p = 100\text{ ns}$, I/O to V_{SS}
Channel Input Capacitance	$C_{I/O}$ to V_{SS}	–	0.65	0.8	pF	$V_R = 2.5\text{V}$, $V_{CC} = 5\text{V}$, $f = 1\text{MHz}$
Variation of Channel Input Capacitance	$\Delta C_{I/O}$	–	0.02	–	pF	$V_{CC} = 5\text{V}$, $V_{SS} = 0\text{V}$, I/O = 2.5V, $f = 1\text{MHz}$, $T = +25^\circ\text{C}$, I/O_x to V_{SS} – I/O_y to V_{SS}

- Notes:
- Device mounted on Polyimide PCB pad layout (2oz copper) as shown on Diodes Inc. suggested pad layout AP02001, which can be found on our website at <http://www.diodes.com>.
 - Short duration pulse test used to minimize self-heating effect.
 - Clamping voltage value is based on an 8x20 μs peak pulse current (I_{pp}) waveform.

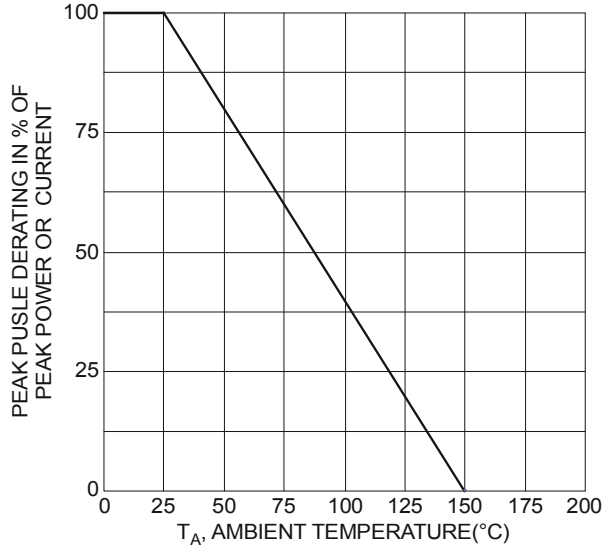


Figure 1 Pulse Derating Curve

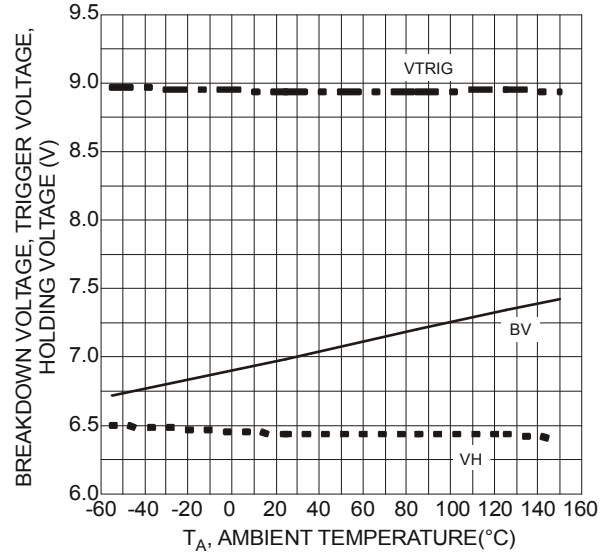


Figure 2 Breakdown Voltage, Trigger Voltage, Holding Voltage vs. Ambient Temperature

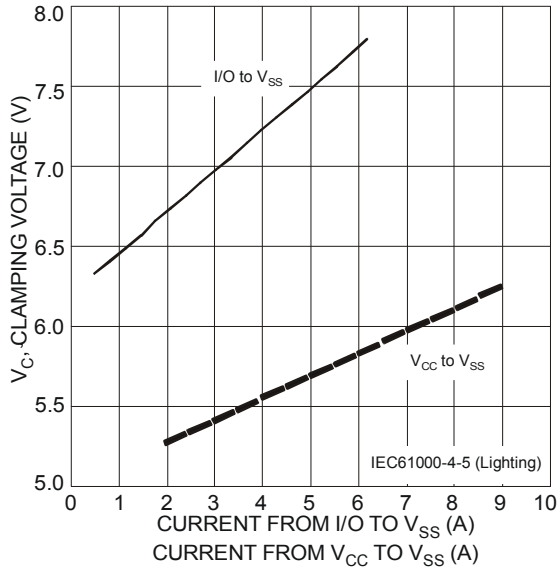


Figure 3 Clamping Voltage Characteristics

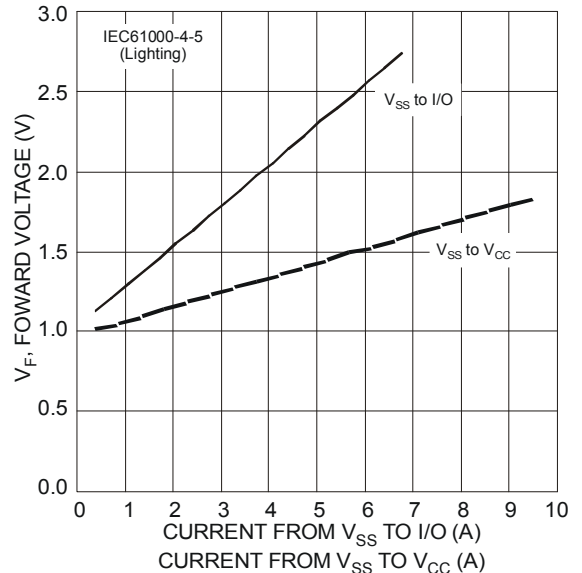


Figure 4 Forward Voltage Characteristics

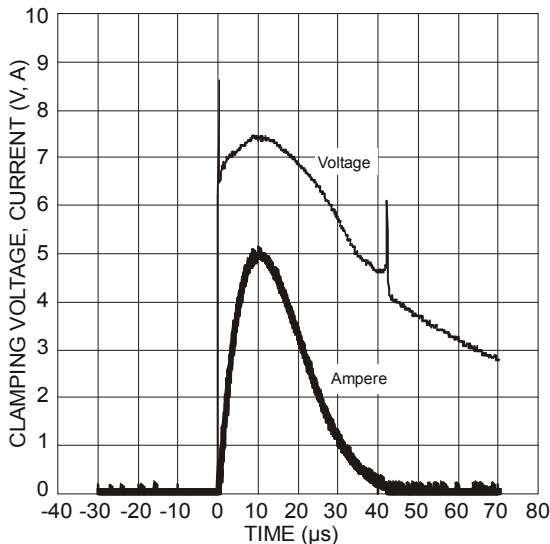


Figure 5 Waveform of Clamping Voltage, Current vs. Time (8/20µs, I/O to VSS)

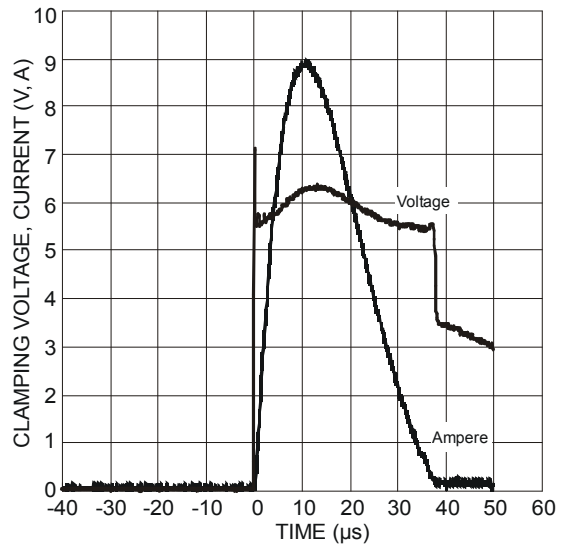


Figure 6 Waveform of Clamping Voltage, Current vs. Time (8/20µs, VCC to VSS)

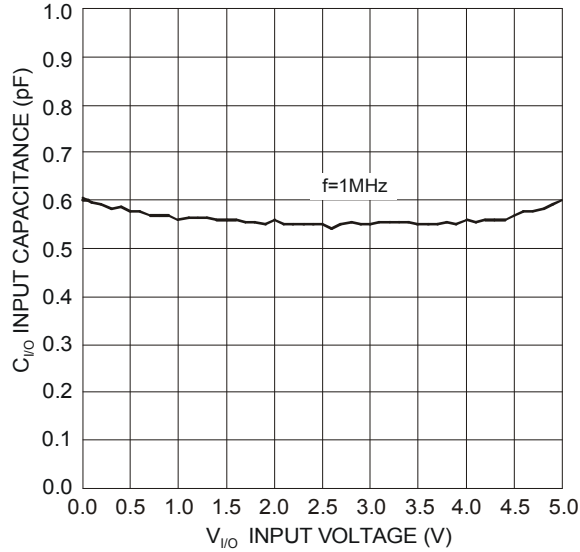


Figure 7 Input Capacitance vs. Input Voltage

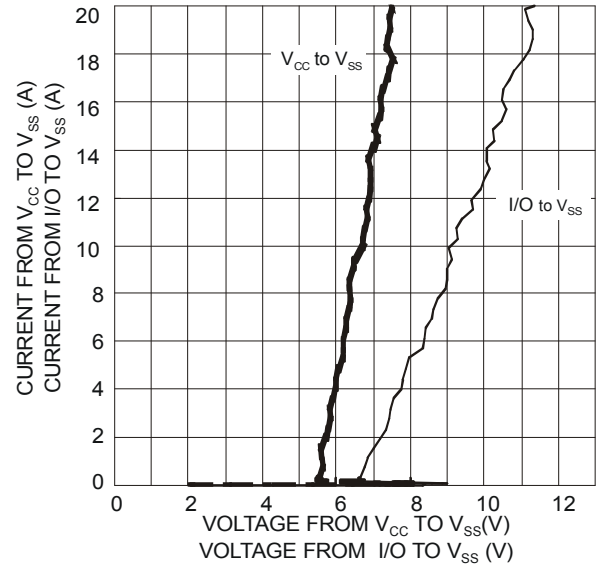
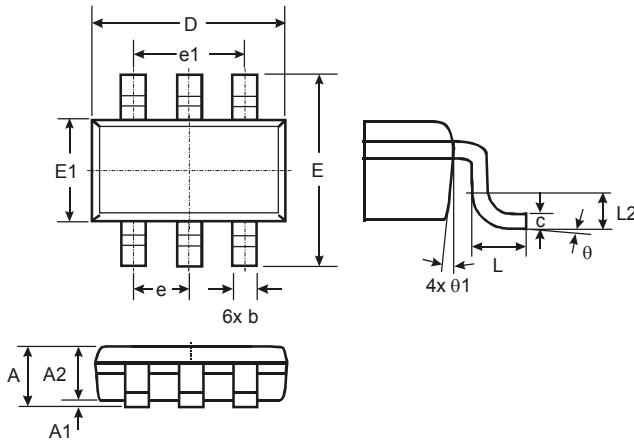


Figure 8. Current vs. Voltage

Package Outline Dimensions

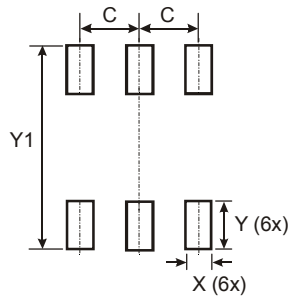
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



TSOT26			
Dim	Min	Max	Typ
A	–	1.00	–
A1	0.01	0.10	–
A2	0.84	0.90	–
D	–	–	2.90
E	–	–	2.80
E1	–	–	1.60
b	0.30	0.45	–
c	0.12	0.20	–
e	–	–	0.95
e1	–	–	1.90
L	0.30	0.50	–
L2	–	–	0.25
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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