

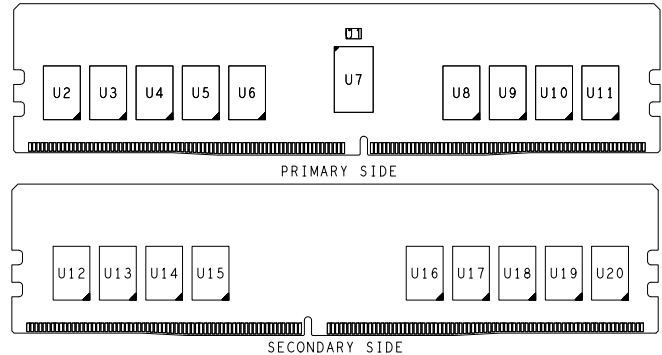
DDR4 SDRAM RDIMM Addendum

MTA18ASF2G72PDBZ – 16GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 RDIMM core data sheet
- 288-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC4-3200
- Extended Temperature Range ($-40^{\circ}\text{C} \leq T_{\text{OPER}} \leq 105^{\circ}\text{C}$)
- 16GB (2 Gig × 72)
- Data bus inversion (DBI) for data bus
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin RDIMM (R/C-G1)



Options

- Operating temperature
 - Extended ($-40^{\circ}\text{C} \leq T_{\text{OPER}} \leq 105^{\circ}\text{C}$)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)

Marking

B
Z
-3G2

Table 1: Addressing

Parameter	16GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig × 8), 16 banks
Module rank address	2 CS _n [1:0]

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT40A1G8,¹ 8Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL _{-n} RCD _{-n} RP)
MTA18ASF2G72PDBZ-3G2__	16GB	2 Gig × 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

- Notes: 1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ASF2G72PDBZ-3G2E1.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	3	157	U3	0	11	168
	1	0	5		1	8	16
	2	2	12		2	10	23
	3	1	150		3	9	161
	4	7	155		4	15	166
	5	4	3		5	12	14
	6	6	10		6	14	21
	7	5	148		7	13	159
U4	0	19	179	U5	0	27	190
	1	16	27		1	24	38
	2	18	34		2	26	45
	3	17	172		3	25	183
	4	23	177		4	31	188
	5	20	25		5	28	36
	6	22	32		6	30	43
	7	21	170		7	29	181
U6	0	CB3	201	U8	0	35	249
	1	CB0	49		1	32	97
	2	CB2	56		2	34	104
	3	CB1	194		3	33	242
	4	CB7	199		4	39	247
	5	CB4	47		5	36	95
	6	CB6	54		6	38	102
	7	CB5	192		7	37	240
U9	0	43	260	U10	0	51	271
	1	40	108		1	48	119
	2	42	115		2	50	126
	3	41	253		3	49	264
	4	47	258		4	55	269
	5	44	106		5	52	117
	6	46	113		6	54	124
	7	45	251		7	53	262
U11	0	59	282	U12	0	56	130
	1	56	130		1	59	282
	2	58	137		2	57	275
	3	57	275		3	58	137
	4	63	280		4	60	128
	5	60	128		5	63	280
	6	62	135		6	61	273
	7	61	273		7	62	135

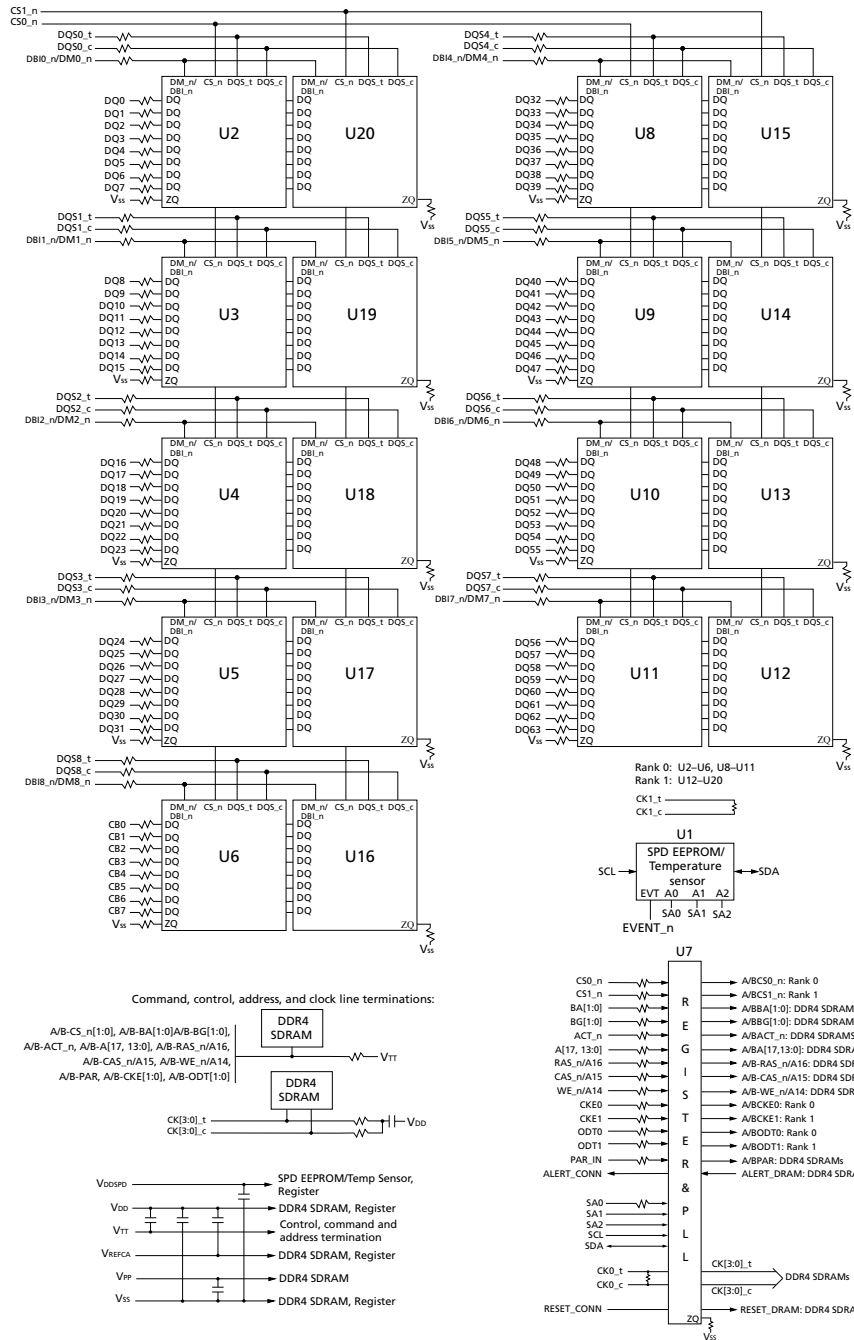


Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U13	0	48	119	U14	0	40	108
	1	51	271		1	43	260
	2	49	264		2	41	253
	3	50	126		3	42	115
	4	52	117		4	44	106
	5	55	269		5	47	258
	6	53	262		6	45	251
	7	54	124		7	46	113
U15	0	32	97	U16	0	CB0	49
	1	35	249		1	CB3	201
	2	33	242		2	CB1	194
	3	34	104		3	CB2	56
	4	36	95		4	CB4	47
	5	39	247		5	CB7	199
	6	37	240		6	CB5	192
	7	38	102		7	CB6	54
U17	0	24	38	U18	0	16	27
	1	27	190		1	19	179
	2	25	183		2	17	172
	3	26	45		3	18	34
	4	28	36		4	20	25
	5	31	188		5	23	177
	6	29	181		6	21	170
	7	30	43		7	22	32
U19	0	8	16	U20	0	0	5
	1	11	168		1	3	157
	2	9	161		2	1	150
	3	10	23		3	2	12
	4	12	14		4	4	3
	5	15	166		5	7	155
	6	13	159		6	5	148
	7	14	21		7	6	10

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions (-40° ≤ T_C ≤ 105°) – 16GB (Die Revision E)

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig × 8) component data sheet.

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	693	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{pp} current	I _{PP0} ¹	54	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1} ¹	837	mA
Precharge standby current	I _{DD2N} ²	648	mA
Precharge standby ODT current	I _{DD2NT} ¹	666	mA
Precharge power-down current	I _{DD2P} ²	468	mA
Precharge quiet standby current	I _{DD2Q} ²	522	mA
Active standby current	I _{DD3N} ²	846	mA
Active standby I _{pp} current	I _{PP3N} ²	54	mA
Active power-down current	I _{DD3P} ²	666	mA
Burst read current	I _{DD4R} ¹	1935	mA
Burst write current	I _{DD4W} ¹	1674	mA
Burst refresh current (1x REF)	I _{DD5R} ¹	1134	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R} ¹	72	mA
Self refresh current: Normal temperature range (-40°C to 85°C)	I _{DD6N} ²	612	mA
Self refresh current: Extended temperature range (-40°C to 105°C)	I _{DD6E} ²	1710	mA
Self refresh current: Reduced temperature range (-40°C to 45°C)	I _{DD6R} ²	378	mA
Auto self refresh current (25°C)	I _{DD6A} ²	155	mA
Auto self refresh current (45°C)	I _{DD6A} ²	378	mA
Auto self refresh current (75°C)	I _{DD6A} ²	558	mA
Auto self refresh current (105°C)	I _{DD6A} ²	1710	mA
Auto self refresh I _{pp} current	I _{PP6X} ²	108	mA
Bank interleave read current	I _{DD7} ¹	1989	mA
Bank interleave read I _{pp} current	I _{PP7} ¹	144	mA
Maximum power-down current	I _{DD8} ²	360	mA

- Notes: 1. One module rank in the active I_{DD/PP}, the other rank in I_{DD2P/PP3N}.
2. All ranks in this I_{DD/PP} condition.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.