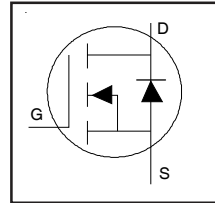


HEXFET® Power MOSFET



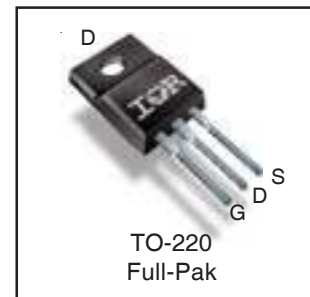
$V_{DSS}$	<b>60V</b>
$R_{DS(on)}$ <b>typ. max.</b>	<b>2.7mΩ</b>
	<b>3.4mΩ</b>
$I_D$ (Silicon Limited)	<b>86A</b>

### Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

### Benefits

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

### Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	86	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	73	
$I_{DM}$	Pulsed Drain Current ①	820	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

### Avalanche Characteristics

$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	738	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦⑧	—	2.87	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)	—	65	

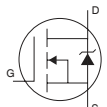
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	29	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.7	3.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
g <sub>fs</sub>	Forward Transconductance	88	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 75A
R <sub>G</sub>	Internal Gate Resistance	—	0.79	—	Ω	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

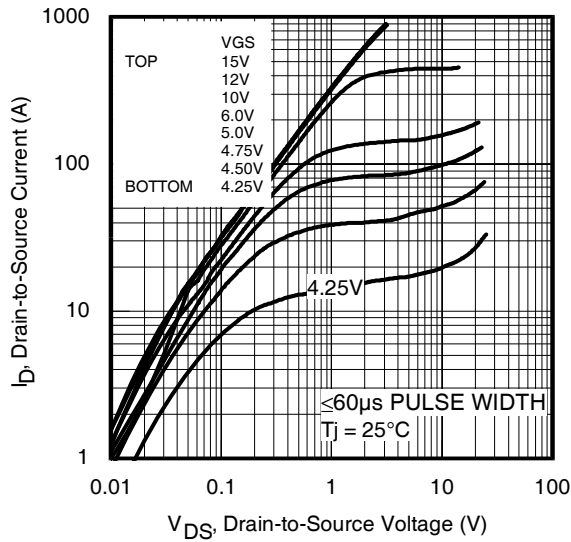
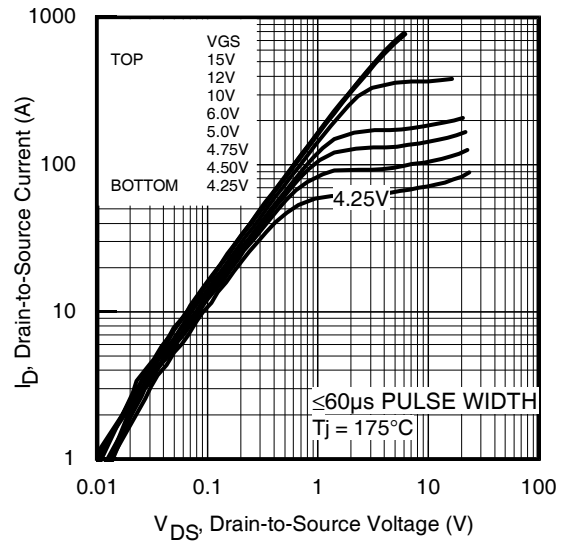
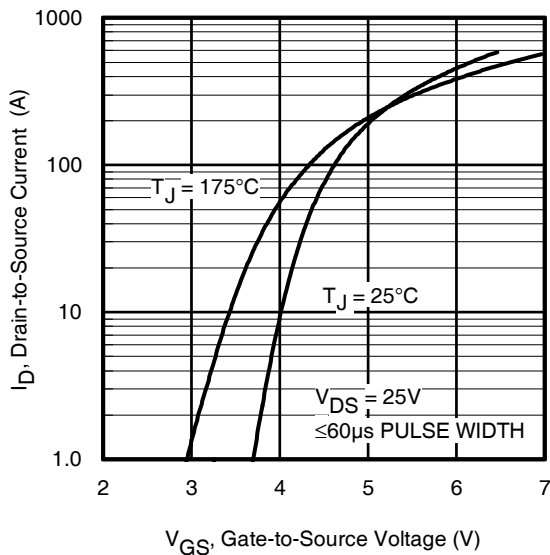
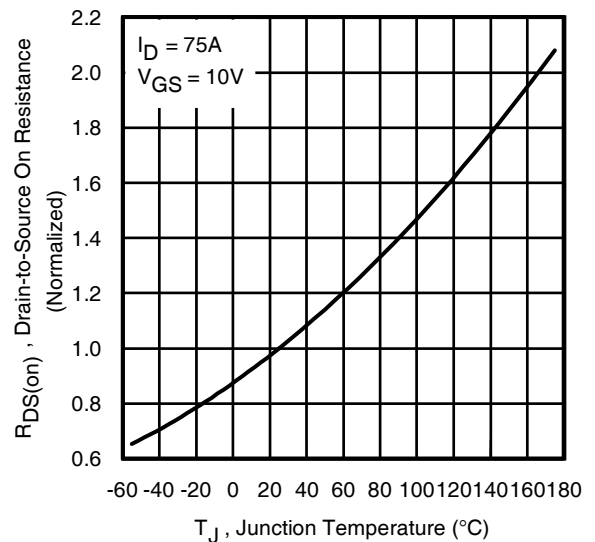
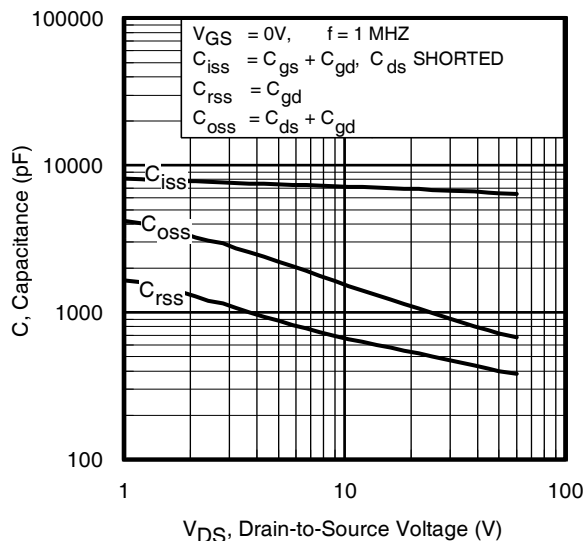
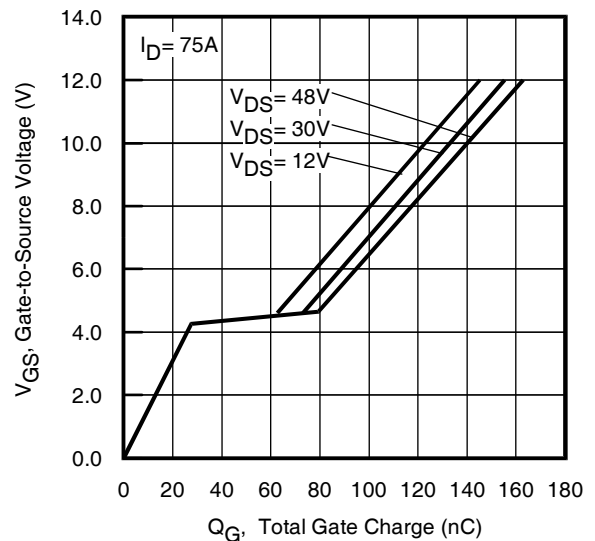
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q <sub>g</sub>	Total Gate Charge	—	130	195	nC	I <sub>D</sub> = 75A V <sub>DS</sub> = 30V V <sub>GS</sub> = 10V <sup>④</sup> I <sub>D</sub> = 75A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	31	—		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	42	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	88	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	22	—	ns	V <sub>DD</sub> = 39V I <sub>D</sub> = 75A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V <sup>④</sup>
t <sub>r</sub>	Rise Time	—	77	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	55	—		
t <sub>f</sub>	Fall Time	—	64	—		
C <sub>iss</sub>	Input Capacitance	—	6600	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 48V f = 1.0 MHz, See Fig. 5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑤</sup> , See Fig. 11 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑤</sup>
C <sub>oss</sub>	Output Capacitance	—	720	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	400	—		
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related)	—	1080	—		
C <sub>oss eff. (TR)</sub>	Effective Output Capacitance (Time Related)	—	1400	—		

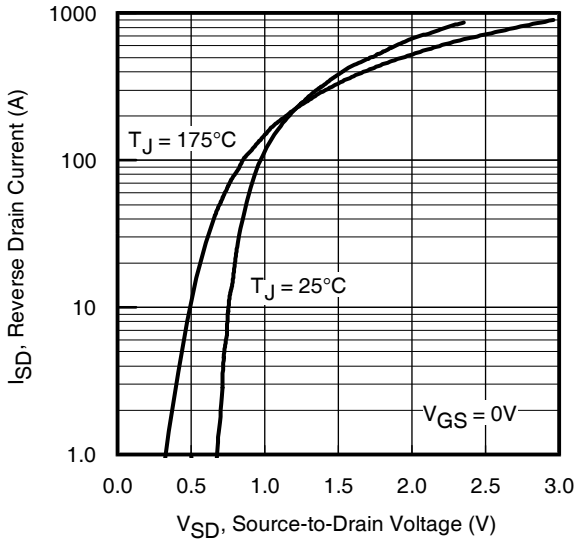
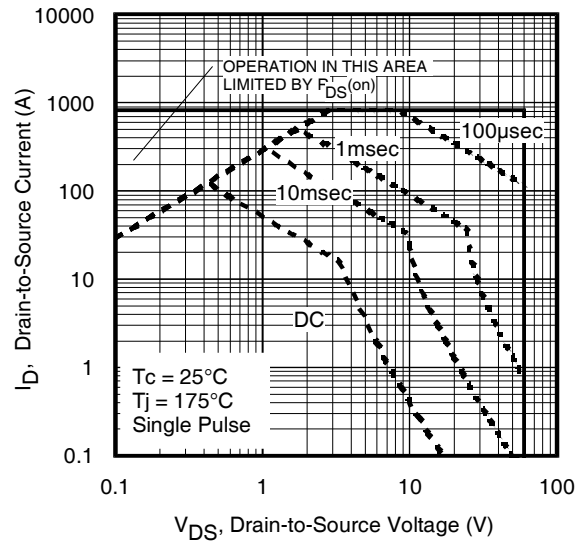
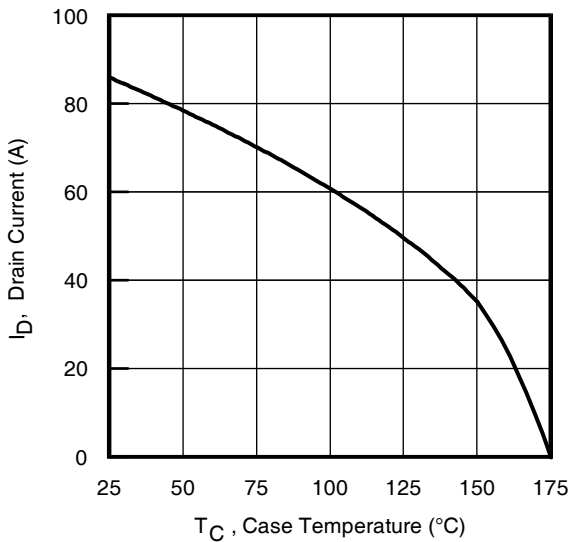
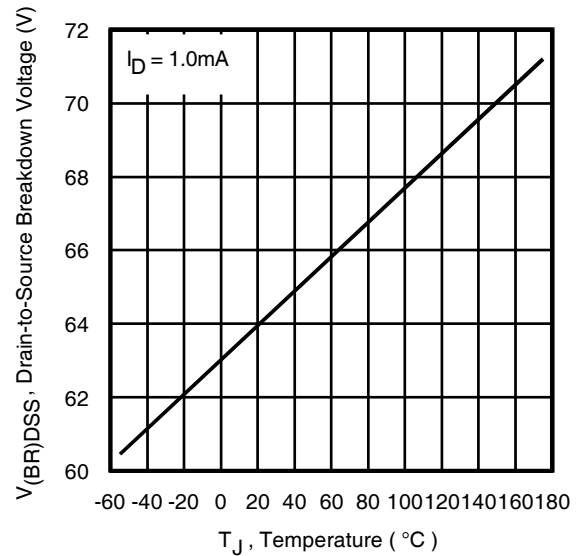
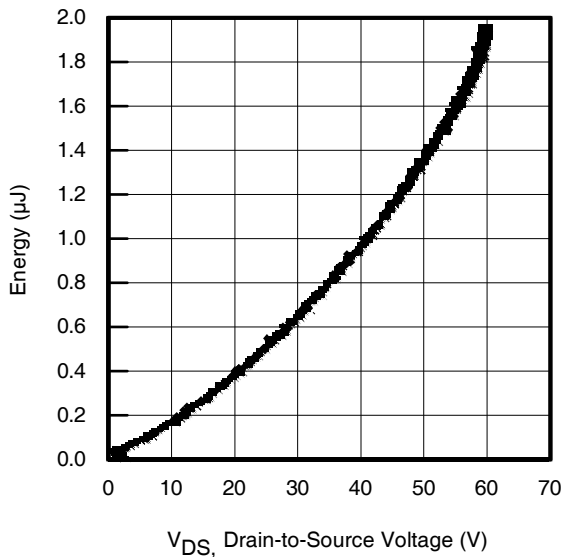
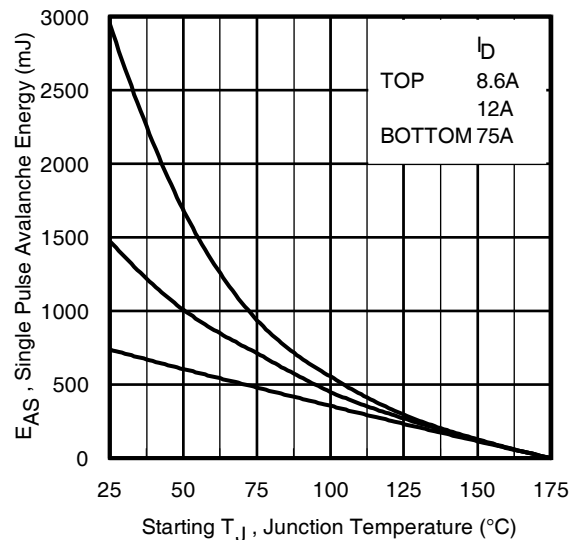
**Diode Characteristics**

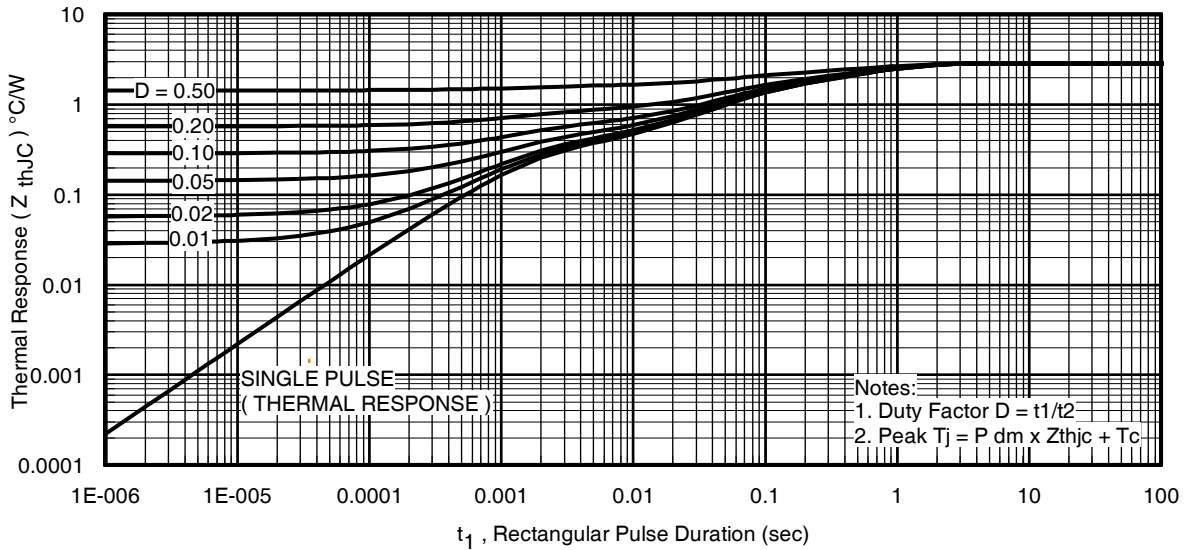
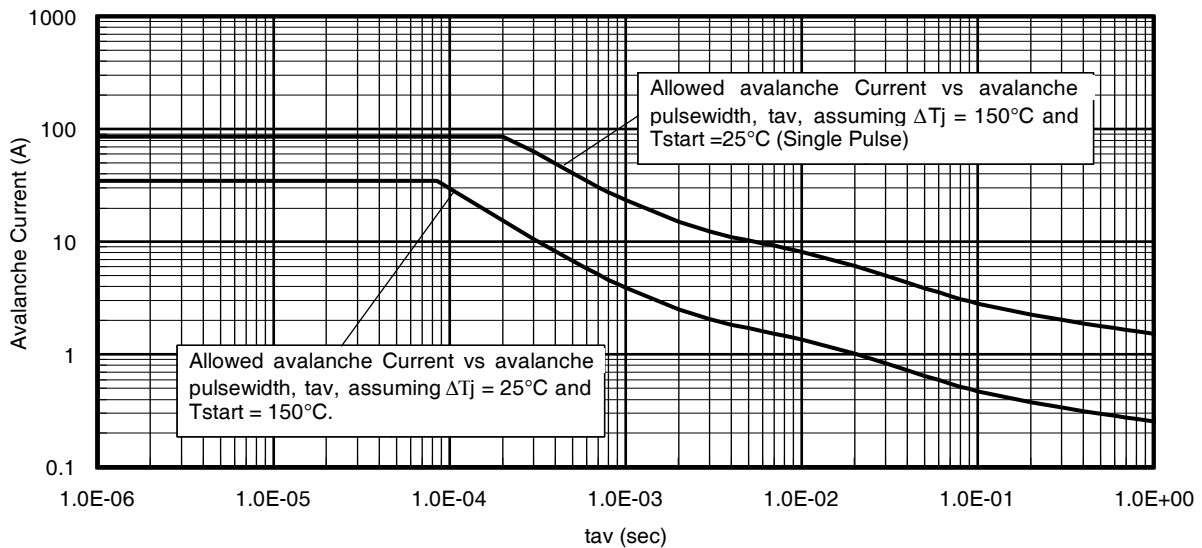
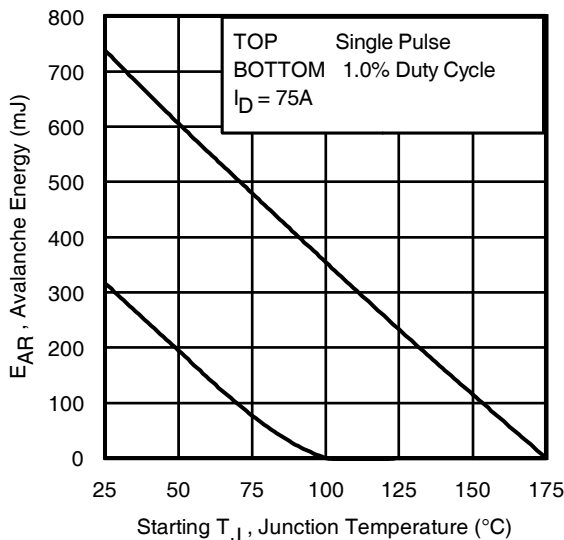
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	86	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	820	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>GS</sub> = 0V <sup>④</sup>
dv/dt	Peak Diode Recovery <sup>③</sup>	—	3.3	—	V/ns	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>DS</sub> = 60V
t <sub>rr</sub>	Reverse Recovery Time	—	43	—	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 51V, T <sub>J</sub> = 125°C I <sub>F</sub> = 75A
Q <sub>rr</sub>	Reverse Recovery Charge	—	58	—	nC	
		—	65	—		T <sub>J</sub> = 125°C
I <sub>RPM</sub>	Reverse Recovery Current	—	2.4	—	A	T <sub>J</sub> = 25°C

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.26mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 75A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 75A, di/dt ≤ 890A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- ⑧ R<sub>θJC</sub> value shown is at time zero.


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical  $C_{OSS}$  Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width**

**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
**(For further info, see AN-1005 at www.irf.com)**

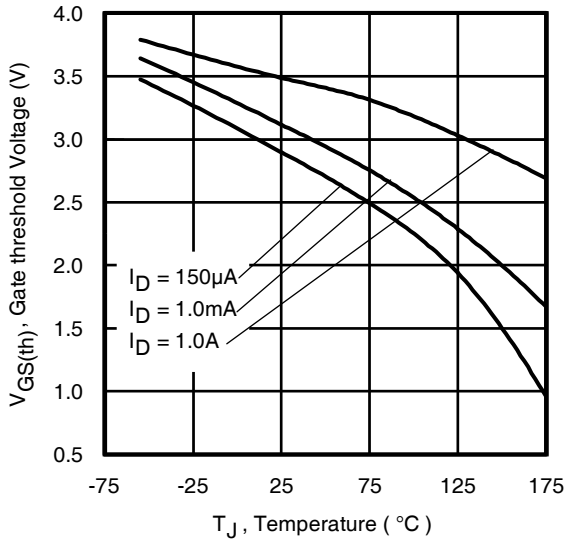
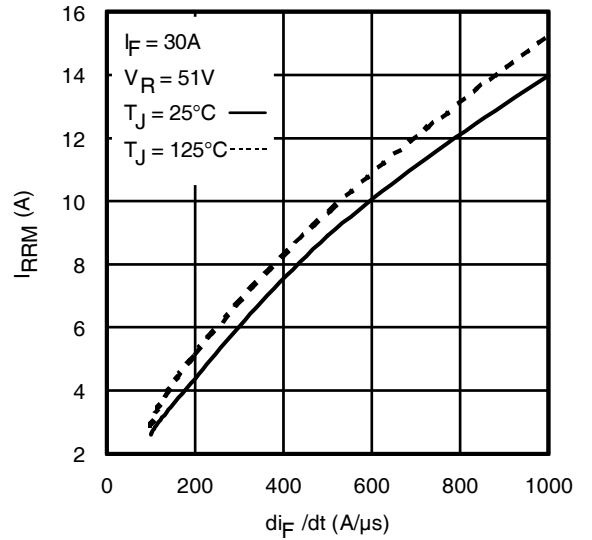
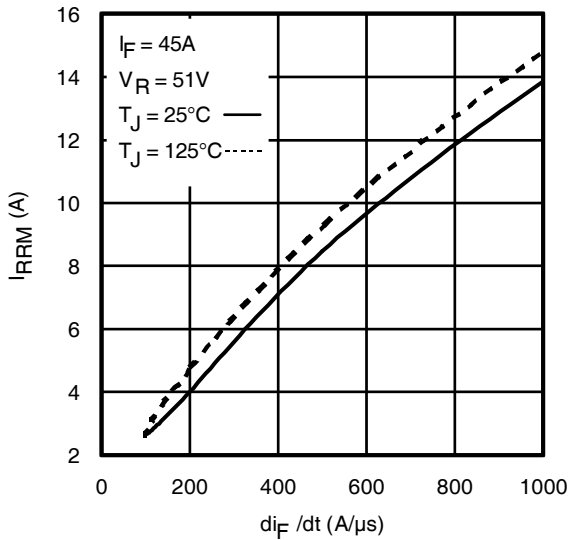
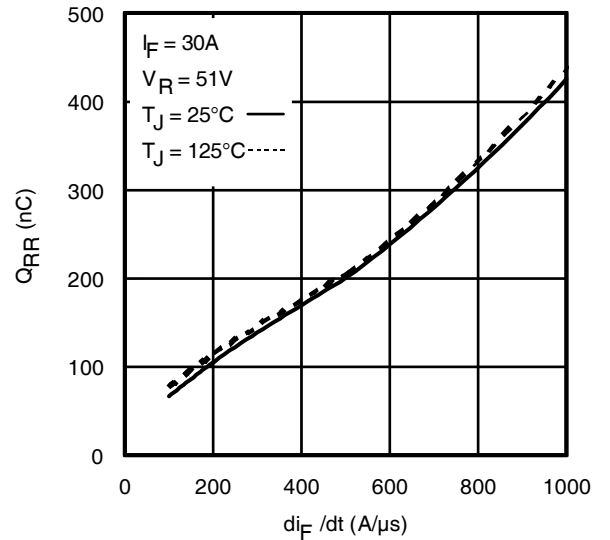
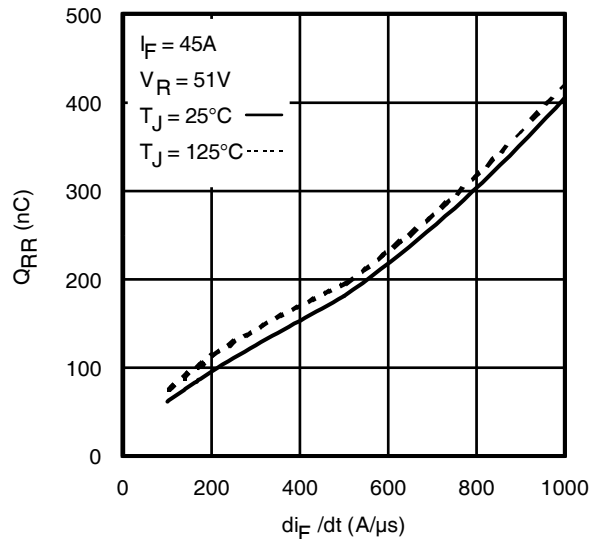
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

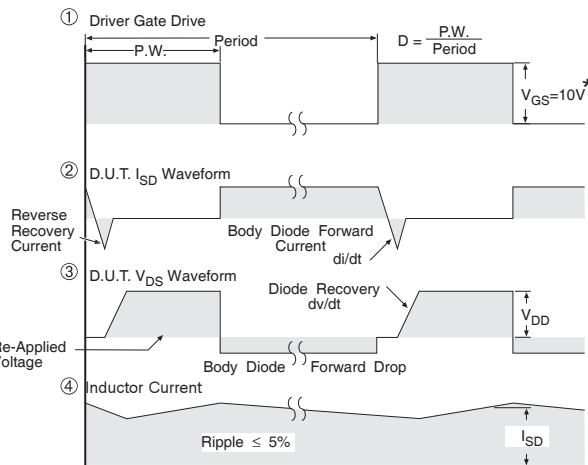
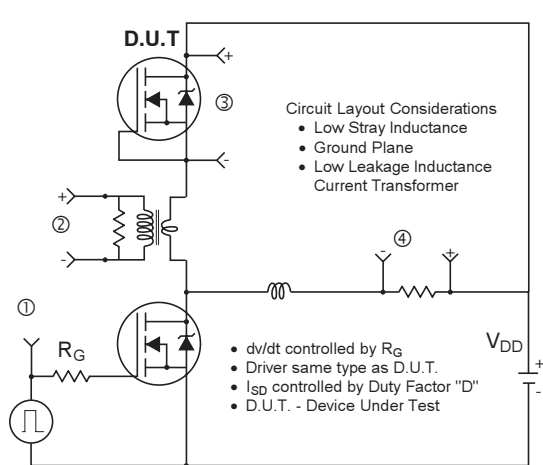
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

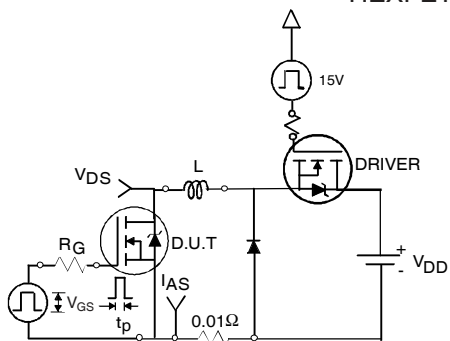
**Fig 15. Maximum Avalanche Energy vs. Temperature**


**Fig. 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18 -** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di_F/dt$

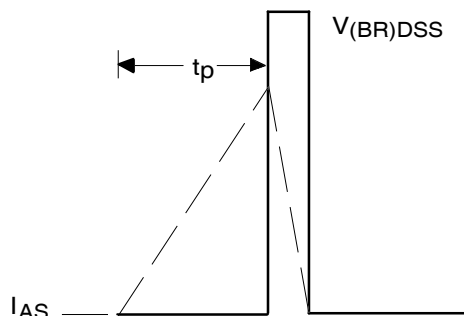


\*  $V_{GS} = 5V$  for Logic Level Devices

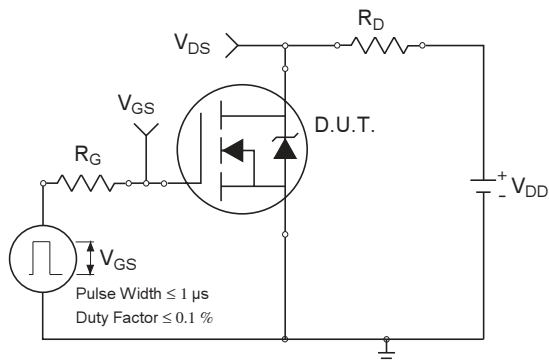
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



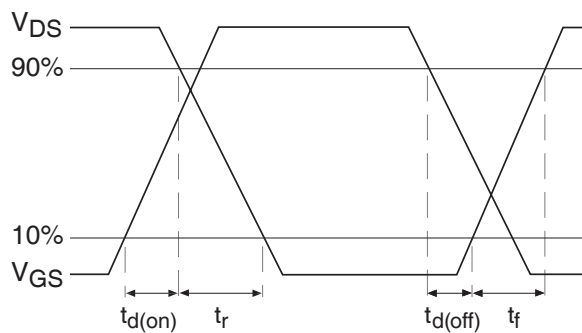
**Fig 22a. Unclamped Inductive Test Circuit**



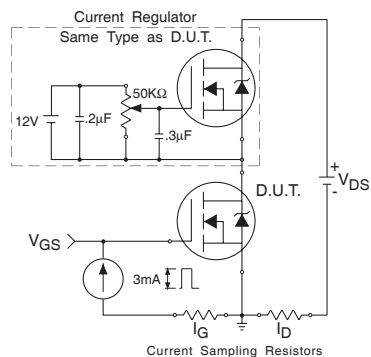
**Fig 22b. Unclamped Inductive Waveforms**



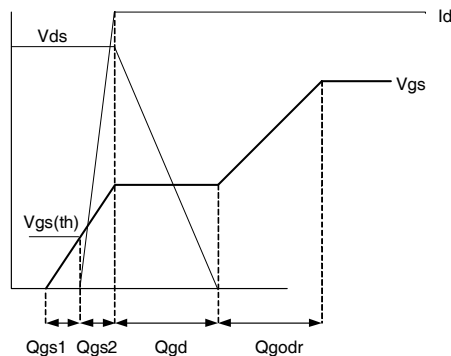
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



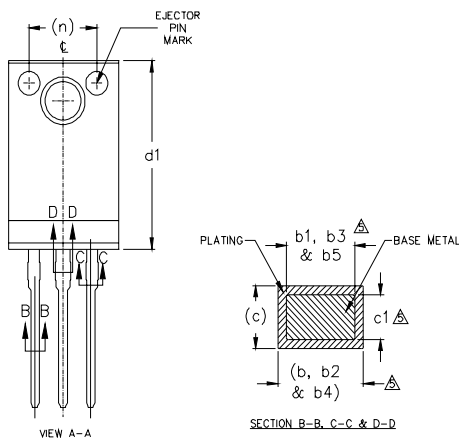
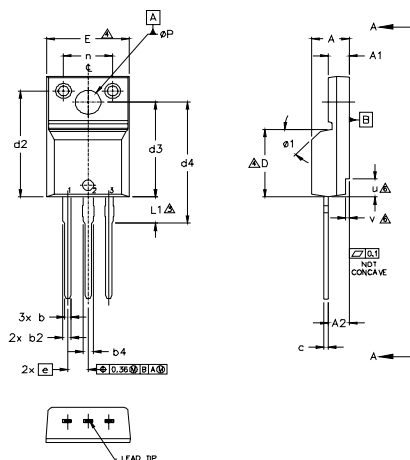
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.83	.101	.111	
A2	2.41	2.92	.095	.115	
b	0.62	.094	0.24	.037	
b1	0.62	0.89	.024	0.35	5
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	5
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	5
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.65	9.80	.341	.386	
d1	15.80	16.12	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.92	.484	.509	
d4	8.64	9.91	.340	.390	
E	9.63	10.63	.379	.419	4
e	2.54 BSC		.100 BSC		
L	13.20	13.72	.520	.540	
L1	3.10	2.31	.122	.138	3
n	6.05	6.15	.238	.242	
øP	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	6
v	0.40	0.50	.016	.020	6
ø1	-	45°	-	45°	

**LEAD ASSIGNMENTS**

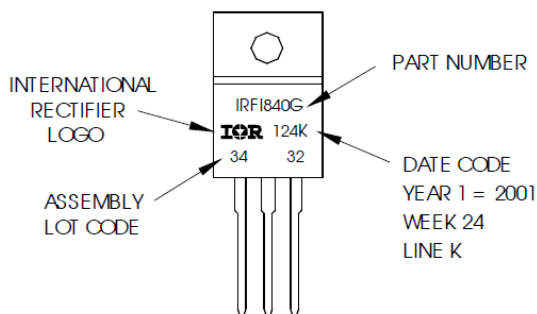
- HEXFET**  
 1.- GATE  
 2.- DRAIN  
 3.- SOURCE

- IGBTs, CoPACK**  
 1.- GATE  
 2.- COLLECTOR  
 3.- EMITTER

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON VV24, 2001  
 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
 indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Consumer <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	TSOP-6	MSL1 (per IPC/JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site

<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.