HARRIS
SEMICONDUCTOR

HIP6003

Buck Pulse-Width Modulator (PWM) Controller and Output Voltage Monitor

September 1997

Features

- **Drives N-Channel MOSFET**
- **Operates From +5V or +12V Input**
- **Simple Single-Loop Control Design**
  - **Voltage-Mode PWM Control**
- **Fast Transient Response**
  - **High-Bandwidth Error Amplifier**
  - **Full 0% to 100% Duty Ratio**
- **Excellent Output Voltage Regulation**
  - **±1% Over Line Voltage and Temperature**
- **4 Bit Digital-to-Analog Output Voltage Selection**
  - **Wide Range - 2.0VDC to 3.5VDC**
  - **0.1V Binary Steps**
- **Power-Good Output Voltage Monitor**
- **Over-Voltage and Over-Current Fault Monitors**
  - **Does Not Require Extra Current Sensing Element**
  - **Uses MOSFET's $r_{DS(ON)}$**
- **Small Converter Size**
  - **Constant Frequency Operation**
  - **200kHz Free-Running Oscillator Programmable from 50kHz to over 1MHz**

Applications

- **Power Supply for Pentium™, Pentium™ Pro, PowerPC™ and Alpha™ Microprocessors**
- **High-Power 5V to 3.xV DC-DC Regulators**
- **Low-Voltage Distributed Power Supplies**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP6003CB	0 to 70	16 Ld SOIC	M16.15

Alpha™ is a trademark of Digital Equipment Corporation.

Pentium™ is a trademark of Intel Corporation.

PowerPC™ is a trademark of IBM.

Description

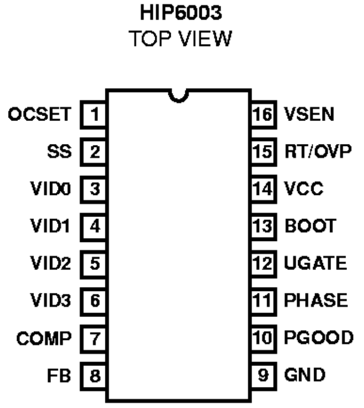
The HIP6003 provides complete control and protection for a DC-DC converter optimized for high-performance microprocessor applications. It is designed to drive an N-Channel MOSFET in a standard buck topology. The HIP6003 integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The output voltage of the converter is easily adjusted and precisely regulated. The HIP6003 includes a 4-Input Digital-to-Analog Converter (DAC) that adjusts the output voltage from 2.0VDC to 3.5VDC in 0.1V increments. The precision reference and voltage-mode regulator hold the selected output voltage to within ±1% over temperature and line voltage variations.

The HIP6003 provides simple, single feedback loop, voltage-mode control with fast transient response. It includes a 200kHz free-running triangle-wave oscillator that is adjustable from below 50kHz to over 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The HIP6003 monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The HIP6003 protects against over-current conditions by inhibiting PWM operation. Built-in over-voltage protection triggers an external SCR to crowbar the input supply. The HIP6003 monitors the current by using the $r_{DS(ON)}$ of the upper MOSFET which eliminates the need for a current sensing resistor.

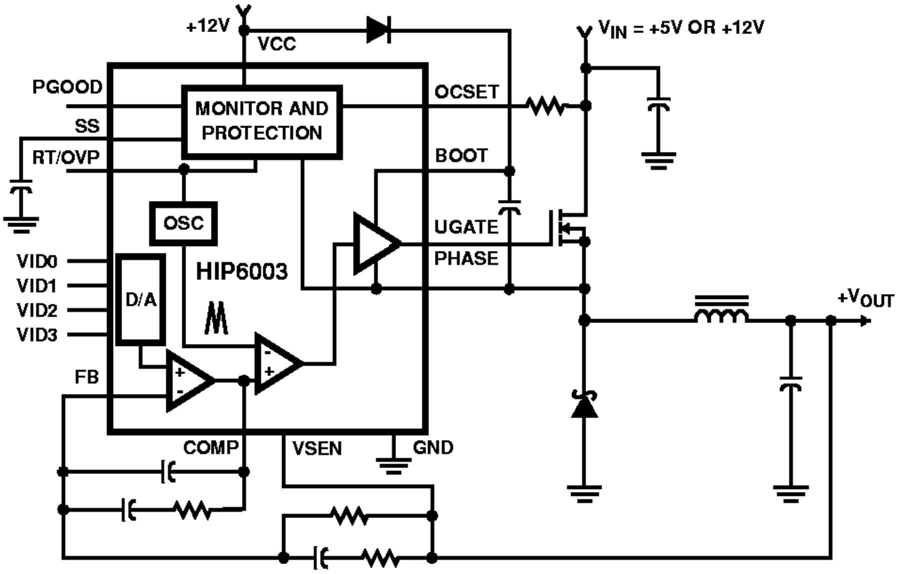
Pinout



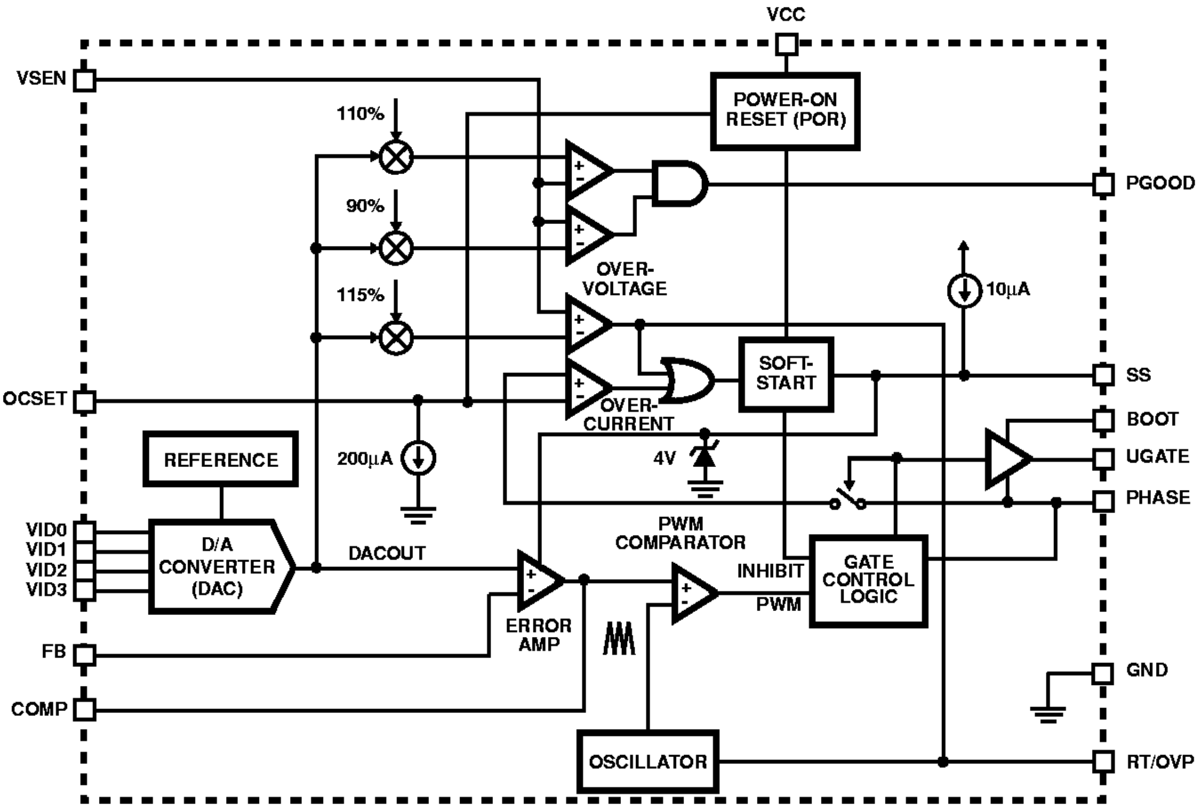
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
Copyright © Harris Corporation 1997

File Number **4274.1**

Typical Application



Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{CC}	+15.0V
Boot Voltage, V_{BOOT} - V_{PHASE}	+15.0V
Input, Output or I/O Voltage	GND -0.3V to VCC + 0.3V
ESD Classification	Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC}	+12V ±10%
Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	100
SOIC Package (with 3 in^2 of Copper)	90
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{CC}	UGATE Open	-	5	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	-	-	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.2	-	-	V
Rising V_{OCSET} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency		RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = OPEN	-	1.9	-	V_{P-P}
REFERENCE AND DAC						
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
ERROR AMPLIFIER						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBW		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/µs
GATE DRIVER						
Upper Gate Source	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} = 6V	350	500	-	mA
Upper Gate Sink	R_{UGATE}		-	5.5	10	Ω
PROTECTION						
Over-Voltage Trip (V_{SEN}/DACOUT)			-	115	120	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5VDC	170	200	230	µA
OVP Sourcing Current	I_{OVP}	V_{SEN} = 5.5V; V_{OVP} = 0V	60	-	-	mA
Soft Start Current	I_{SS}		-	10	-	µA

Electrical Specifications Recommended Operating Conditions, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD						
Upper Threshold (V_{SEN}/DACOUT)		V_{SEN} Rising	106	-	111	%
Lower Threshold (V_{SEN}/DACOUT)		V_{SEN} Falling	89	-	94	%
Hysteresis (V_{SEN}/DACOUT)		Upper and Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -5mA	-	0.5	-	V

Typical Performance Curves

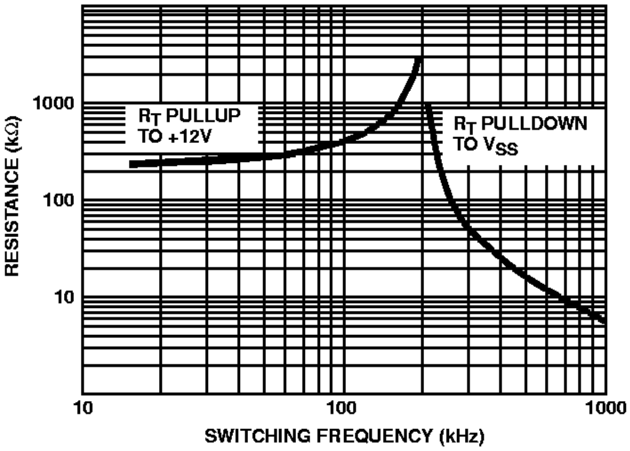


FIGURE 1. R_T RESISTANCE vs FREQUENCY

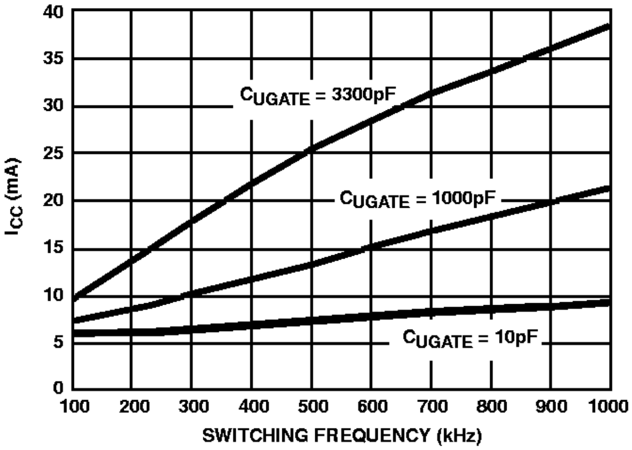
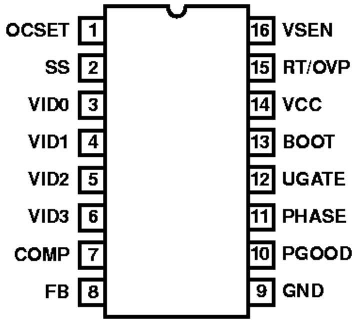


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Description



OCSET (Pin 1)

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCS}), and the upper MOSFET on-resistance. ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCS} \bullet R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

SS (Pin 2)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 10µA current source, sets the soft-start interval of the converter.

VID0-3 (Pins 3-6)

VID0-3 are the input pins to the 4-bit DAC. The states of these four pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 16 combinations of DAC inputs.

COMP (Pin 7) and FB (Pin 8)

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

GND (Pin 9)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGOOD (Pin 10)

PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage.

PHASE (Pin 11)

Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.

UGATE (Pin 12)

Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

BOOT (Pin 13)

This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

VCC (Pin 14)

Provide a 12V bias supply for the chip to this pin.

RT/OVP (Pin 15)

This pin is multiplexed, providing two functions. The first function is oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200KHz switching frequency is increased according to the following equation:

$$F_S \approx 200\text{kHz} + \frac{5 \bullet 10^6}{R_T(\text{k}\Omega)} \qquad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to V_{CC} reduces the switching frequency according to the following equation:

$$F_S \approx 200\text{kHz} + \frac{4 \bullet 10^7}{R_T(\text{k}\Omega)} \qquad (R_T \text{ to 12V})$$

The second function for this pin is to drive an external SCR in the event of an overvoltage condition.

VSEN (Pin 16)

This pin is connected to the converters output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.

Functional Description

Initialization

The HIP6003 automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage at the VCC pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

Soft Start

The POR function initiates the soft start sequence. An internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 3 shows the soft start interval with C_{SS} = 0.1µF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t1 in Figure 3, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t2 and t3 in Figure 3. At t3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (VSEN pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

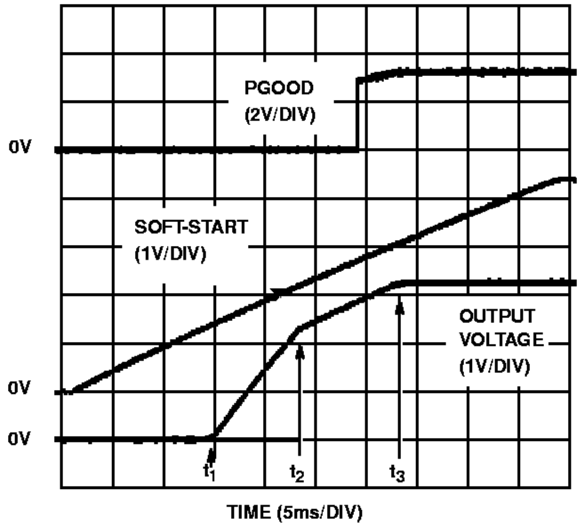


FIGURE 3. SOFT START INTERVAL

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200µA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET}, the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 4 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the C_{SS} charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 4 is 2.5W.

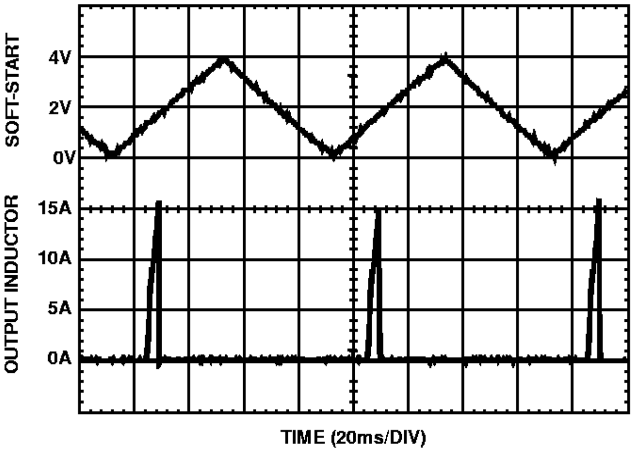


FIGURE 4. OVER-CURRENT OPERATION

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (200µA typical). The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1) The maximum $r_{DS(ON)}$ at the highest junction temperature.
2) The minimum I_{OCSET} from the specification table.
3) Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled ‘Output Inductor Selection’.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a HIP6003 converter is programmed to discrete levels between 2.0VDC and 3.5VDC. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a 4-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 16 combinations of open or short connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

TABLE 1. OUTPUT VOLTAGE PROGRAM

PIN NAME				NOMINAL DACOUT VOLTAGE
VID3	VID2	VID1	VID0	
1	1	1	1	2.0
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

NOTE: 0 = Connected to GND or V_{SS}, 1 = OPEN

The DAC function is a precision non-inverting summation amplifier shown in Figure 5. The resistor values shown are only approximations of the actual precision values used. Grounding any combination of the VID pins increases the DACOUT voltage. The ‘open’ circuit voltage on the VID pins is the band gap reference voltage, 1.26V.

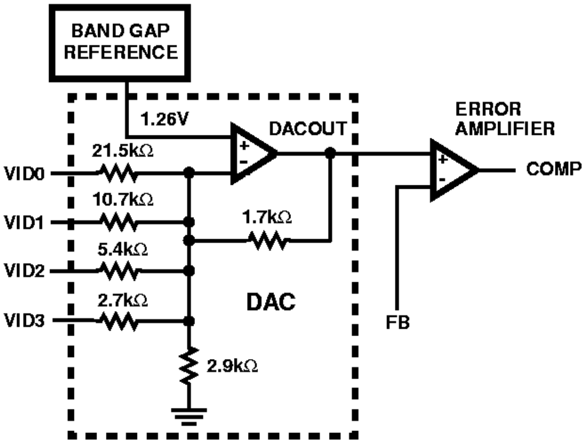


FIGURE 5. DAC FUNCTION SCHEMATIC

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

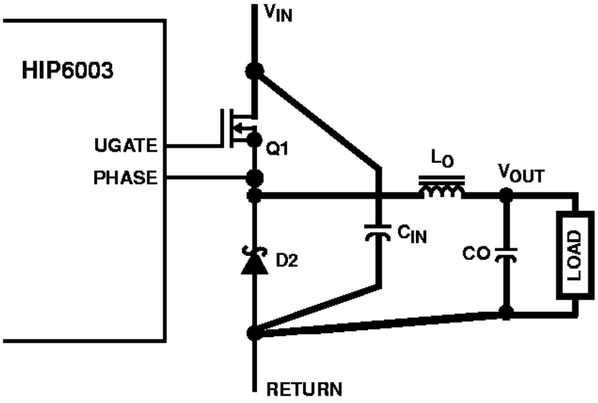


FIGURE 6. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 6 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 6 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the HIP6003 within 3 inches of the MOSFET, Q1. The circuit traces for the MOSFET’s gate and source connections from the HIP6003 must be sized to handle up to 1A peak current.

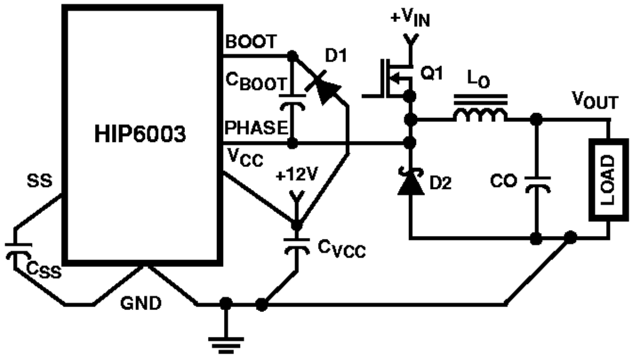


FIGURE 7. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Figure 7 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

Feedback Compensation

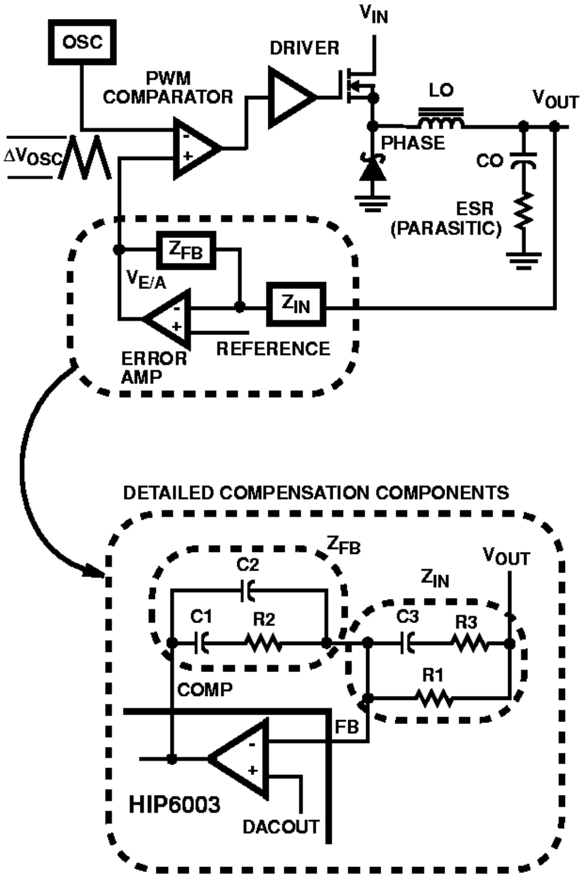


FIGURE 8. VOLTAGE - MODE BUCK CONVERTER COMPENSATION DESIGN

Figure 8 highlights the voltage-mode control loop for a buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \qquad F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)}$$

The compensation network consists of the error amplifier (internal to the HIP6003) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 8. Use these guidelines for locating the poles and zeros of the compensation network:

1) Pick Gain (R2/R1) for desired converter bandwidth
2) Place 1^{ST} Zero Below Filter's Double Pole (~75% F_{LC})
3) Place 2^{ND} Zero at Filter's Double Pole
4) Place 1^{ST} Pole at the ESR Zero
5) Place 2^{ND} Pole at Half the Switching Frequency
6) Check Gain against Error Amplifier's Open-Loop Gain
7) Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \qquad F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \qquad F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3}$$

Figure 9 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 9. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 9 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

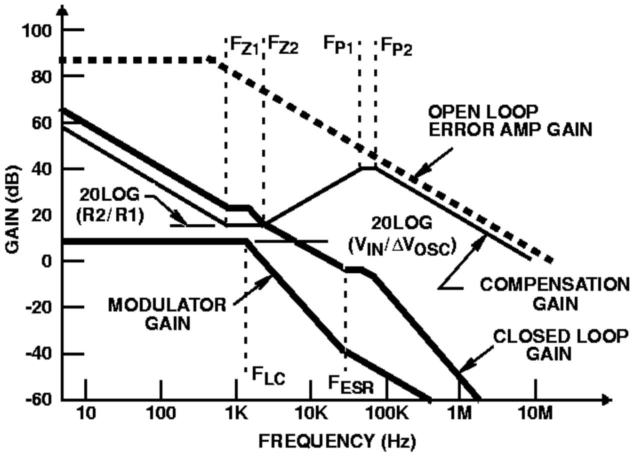


FIGURE 9. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1μF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{FS \times L} \cdot \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the HIP6003 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time. With a +12V input, and output voltage level equal to DACOUT, t_{FALL} is the longest response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the anode of Schottky diode D2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The HIP6003 requires an N-channel power MOSFET. It should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for the MOSFET. Switching losses also contribute to the overall MOSFET power loss (see the equations below). These equations assume linear voltage-current transitions and are approximations. The gate-charge losses are dissipated by the HIP6003 and don't heat the MOSFET. However, large gate-charge increases the switching interval, t_{SW}, which increases the upper MOSFET switching losses. Ensure that the MOSFET is within its maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{COND} = I_O^2 \times r_{DS(ON)} \times D$$

$$P_{SW} = \frac{1}{2} I_O \times V_{IN} \times t_{SW} \times Fs$$

Where: D is the duty cycle + V_{OUT}/V_{IN},
t_{SW} is the switching interval, and
Fs is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the HIP6003. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 10 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the Schottky diode, D2, conducts. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

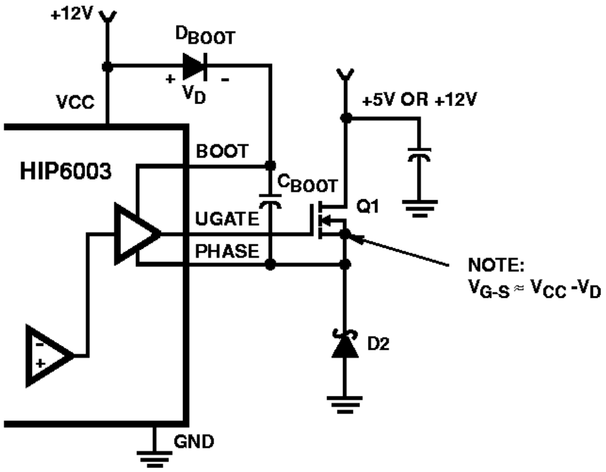


FIGURE 10. UPPER GATE DRIVE - BOOTSTRAP OPTION

Figure 11 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is + 5VDC or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and + 12VDC for the bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET is a good choice for Q1 under these conditions.

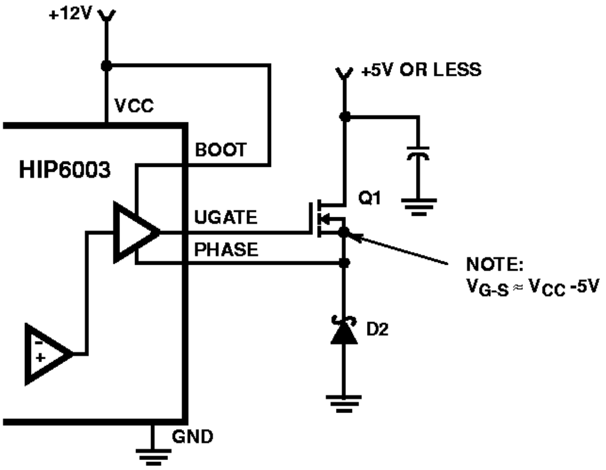


FIGURE 11. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE OPTION

Schottky Selection

Rectifier D2 conducts when the upper MOSFET Q1 is off. The diode should be a Schottky type for low power losses. The power dissipation in the Schottky rectifier is approximated by:

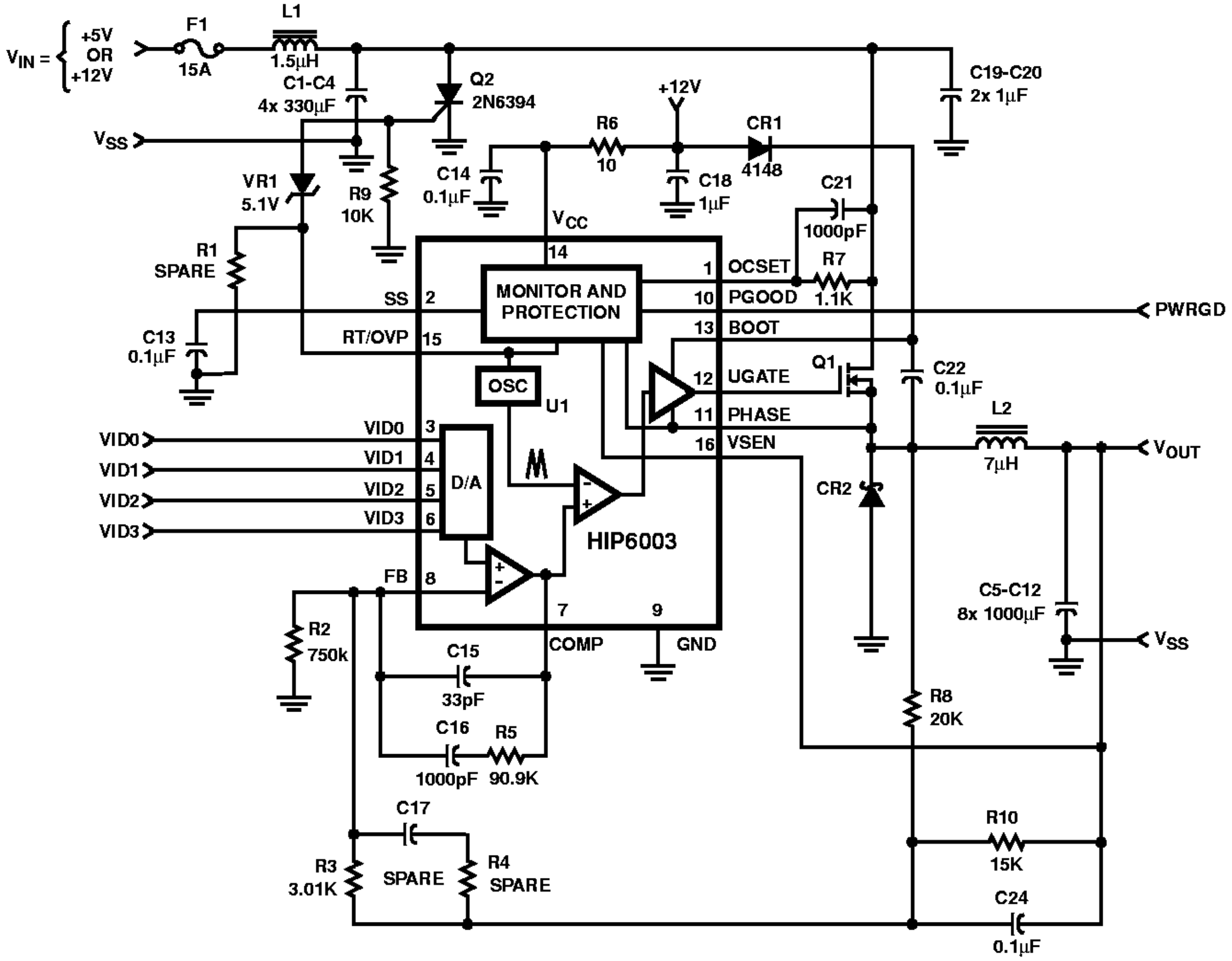
$$P_{COND} = I_O \times V_f \times (1 - D)$$

Where: D is the duty cycle = V_O/V_{IN}, and
V_f is the Schottky forward voltage drop

In addition to power dissipation, package selection and heatsink requirements are the main design tradeoffs in choosing the Schottky rectifier. Since the three factors are interrelated, the selection process is an iterative procedure. The maximum junction temperature of the rectifier must remain below the manufacturer's specified value, typically 125°C. By using the package thermal resistance specification and the Schottky power dissipation equation (shown above), the junction temperature of the rectifier can be estimated. Be sure to use the available airflow and ambient temperature to determine the junction temperature rise. HIP6003 DC-DC Converter Application Circuit.

HIP6003 DC-DC Converter Application Circuit

The figure below shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN9664. See Harris' home page on the web: http://www.semi.harris.com or Harris AnswerFAX (407-724-7800) document # 99664.



Component Selection Notes:
C5-C12 - 8 each 1000µF 6.3W VDC, Sanyo MV-GX or Equivalent
C1-C4 - 4 each 330µF 25W VDC, Sanyo MV-GX or Equivalent
L1 - Core: Micrometals T60-52; Each Winding: 14 Turns of 17AWG
L2 - Core: Micrometals T44-52; Winding: 7 Turns of 18AWG
CR1 - 1N4148 or Equivalent
CR2 - 25A, 35V Schottky, Motorola MBR2535CTL or Equivalent
Q1 - Harris MOSFET; RFP70N03

FIGURE 12. PENTIUM PRO DC-DC CONVERTER