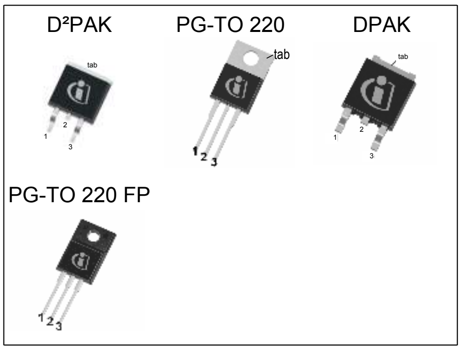
IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

MOSFET

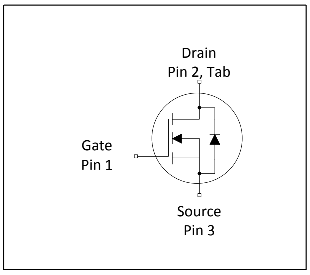
600V CoolMOS™ P6 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.



Features

- Increased MOSFET dv/dt ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)



Potential applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	380	mΩ
$Q_{g.typ}$	19	nC
$I_{D,pulse}$	29	A
E_{oss}@400V	2.7	µJ
Body diode di/dt	500	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPB60R380P6	PG-TO 263-3	6R380P6	see Appendix A
IPP60R380P6	PG-TO 220-3		
IPD60R380P6	PG-TO 252-3		
IPA60R380P6	PG-TO 220 FullPAK		

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	10.6 6.7	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	29	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	210	mJ	I_D=1.8A; V_{DD}=50V; see table 12
Avalanche energy, repetitive	E_{AR}	-	-	0.32	mJ	I_D=1.8A; V_{DD}=50V; see table 12
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (Non FullPAK) TO-220, TO-252, TO-263	P_{tot}	-	-	83	W	T_C=25°C
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	31	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque (Non FullPAK) TO-220	-	-	-	60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	9.2	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	29	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 10
Maximum diode commutation speed	di_f/dt	-	-	500	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 10
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.75
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (Non FullPAK) TO-220

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 5 Thermal characteristics TO-252, TO-263

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	V_{DS}=V_{GS}, I_D=0.32mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.342 0.889	0.380 -	Ω	V_{GS}=10V, I_D=3.8A, T_j=25°C V_{GS}=10V, I_D=3.8A, T_j=150°C
Gate resistance	R_G	-	7.8	-	Ω	f=1MHz, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	877	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	42	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	33	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	135	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=3.4Ω; see table 11
Rise time	t_r	-	6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=3.4Ω; see table 11
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.8A, R_G=3.4Ω; see table 11
Fall time	t_f	-	7	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=4.8A, R_G=3.4Ω; see table 11

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.4	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	7	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	19	-	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V

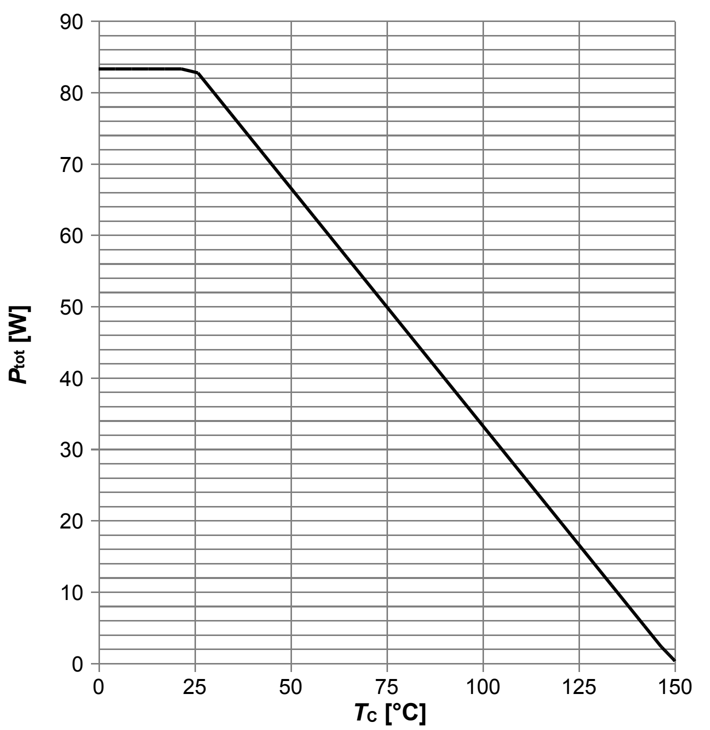
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=4.8A, T_j=25°C
Reverse recovery time	t_{rr}	-	232	-	ns	V_R=400V, I_F=4.8A, di_F/dt=100A/µs; see table 10
Reverse recovery charge	Q_{rr}	-	2.1	-	µC	V_R=400V, I_F=4.8A, di_F/dt=100A/µs; see table 10
Peak reverse recovery current	I_{rrm}	-	17	-	A	V_R=400V, I_F=4.8A, di_F/dt=100A/µs; see table 10

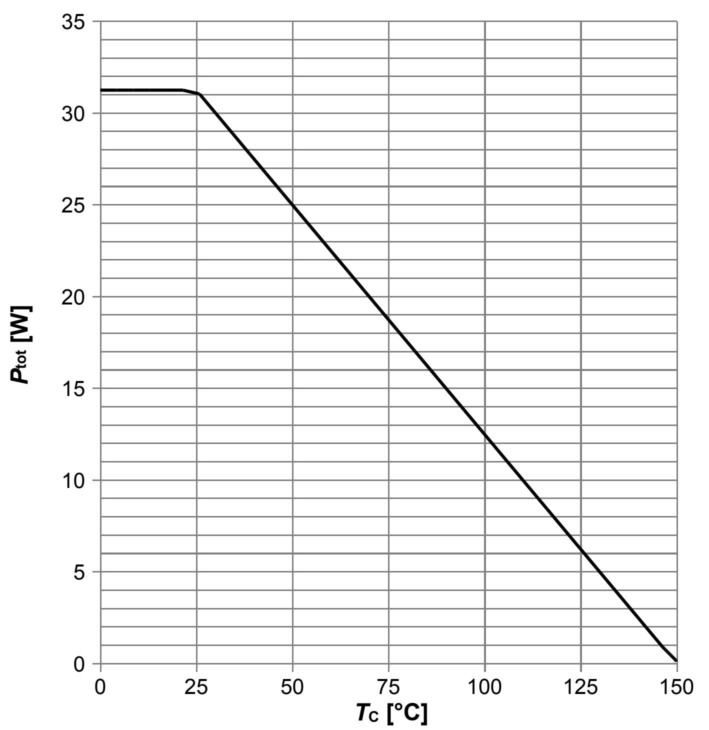
4 Electrical characteristics diagrams

Diagram 1: Power dissipation (Non FullPAK)



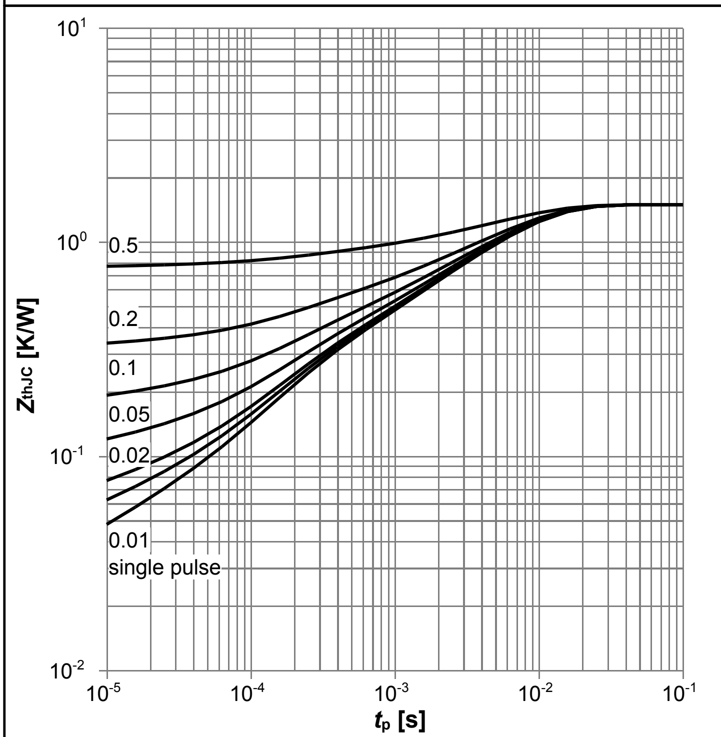
P_{tot}=f(T_C)

Diagram 2: Power dissipation (FullPAK)



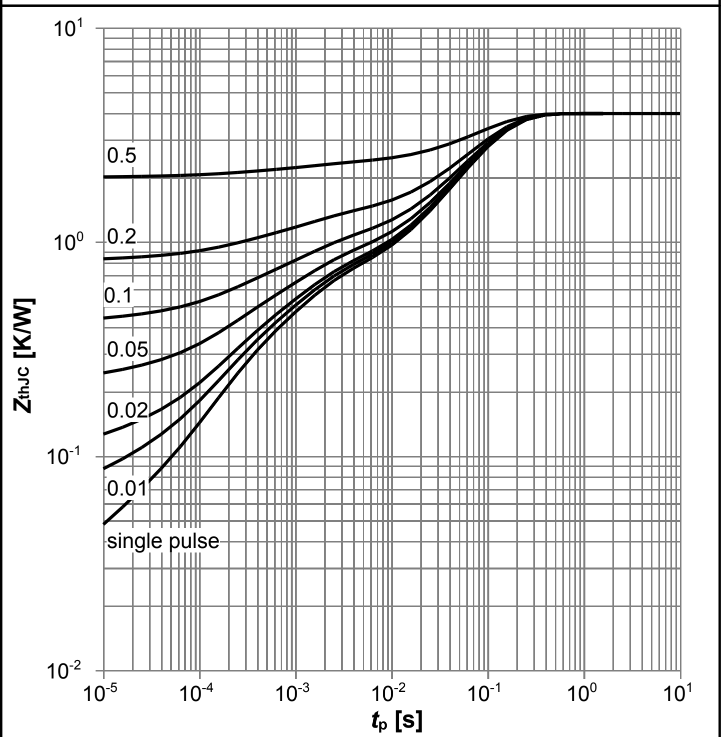
P_{tot}=f(T_C)

Diagram 3: Max. transient thermal impedance (Non FullPAK)



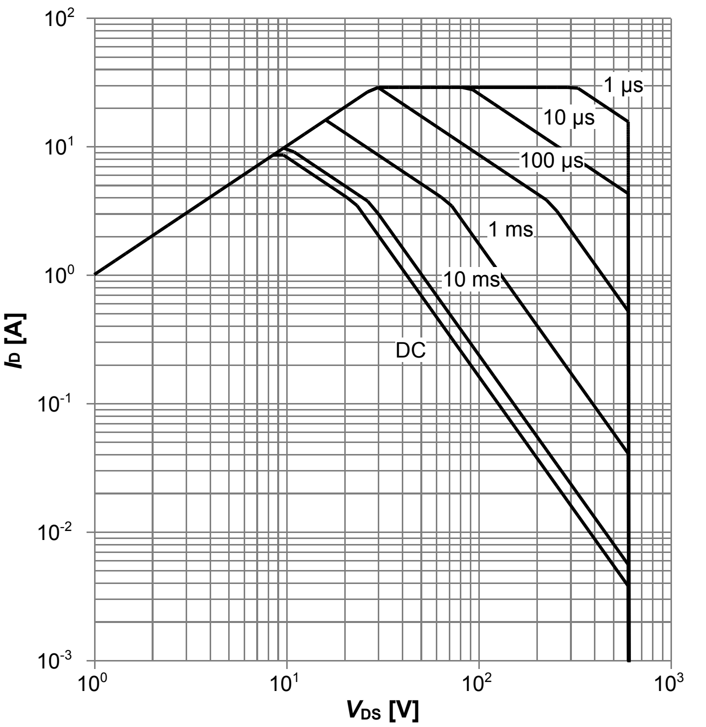
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 4: Max. transient thermal impedance (FullPAK)



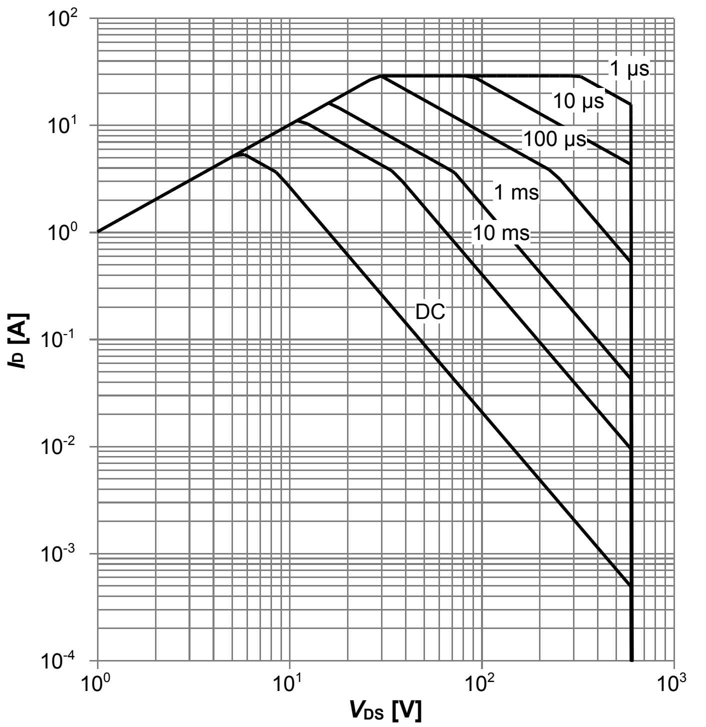
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Safe operating area (Non FullPAK)



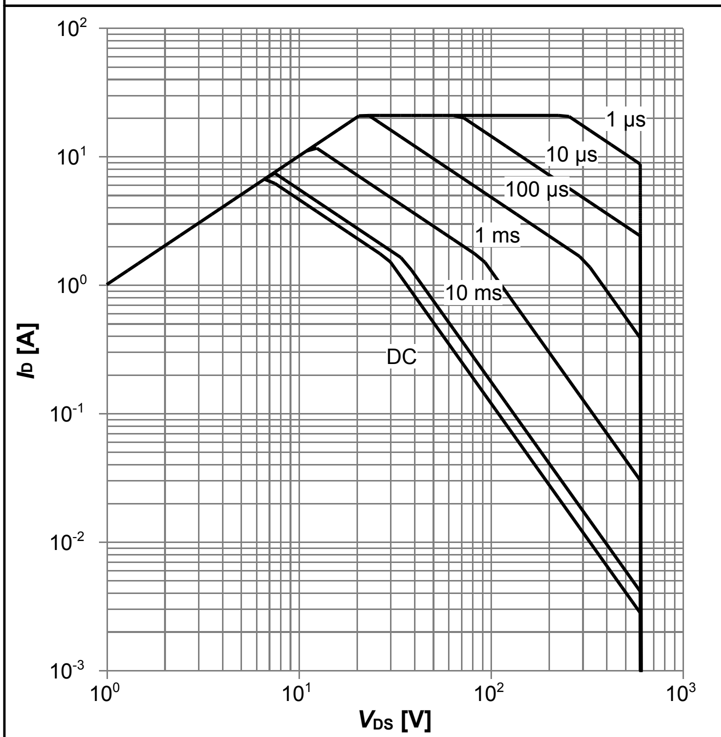
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



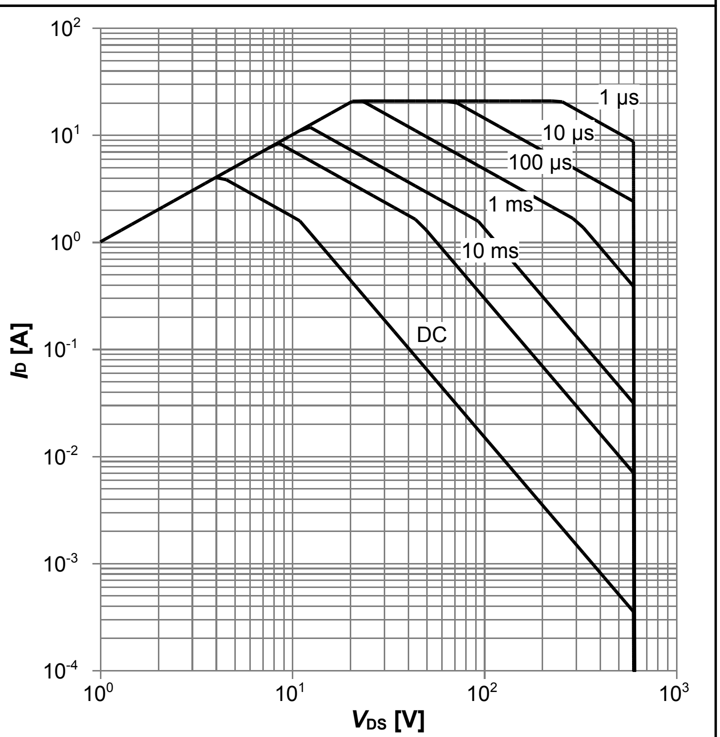
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



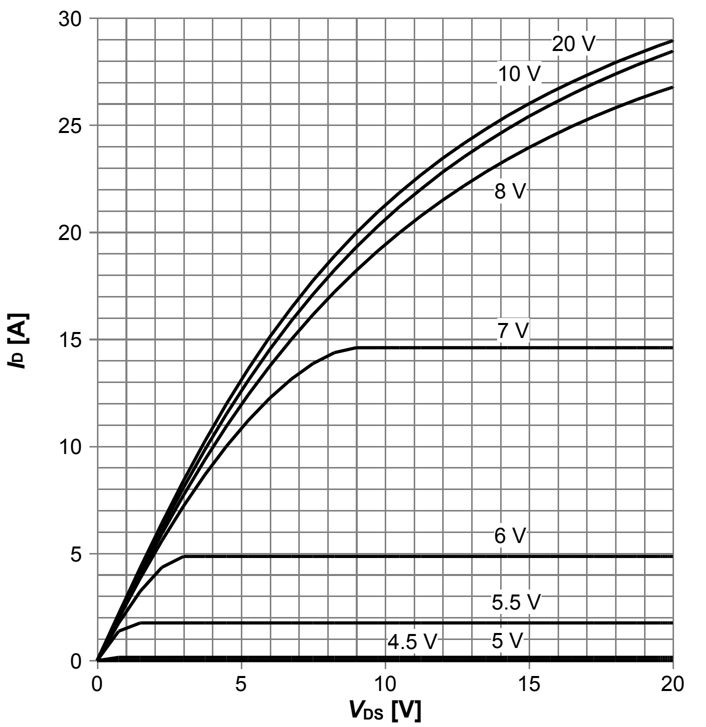
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



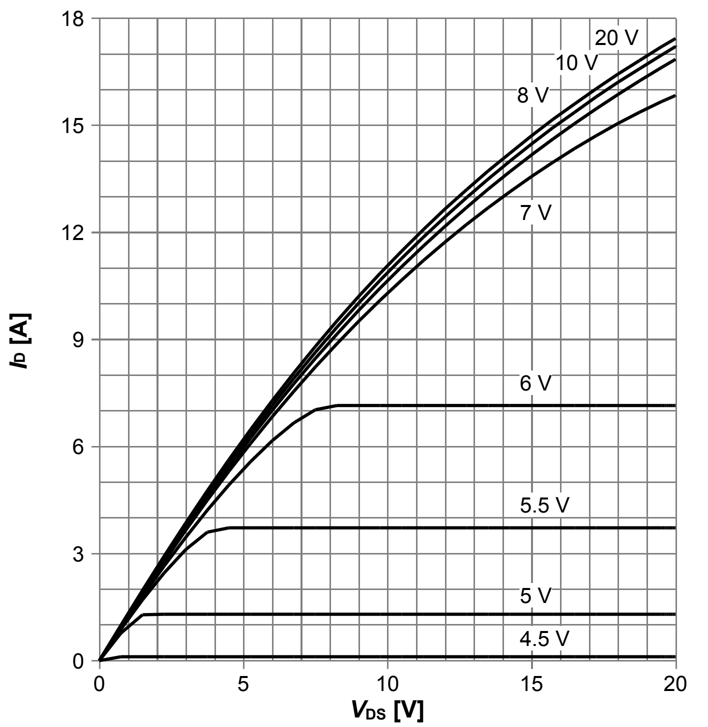
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 9: Typ. output characteristics



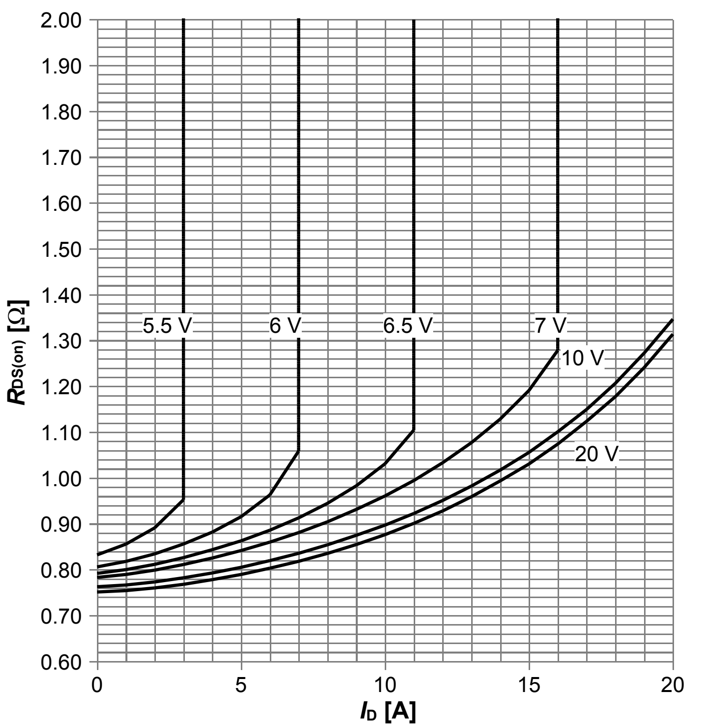
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 10: Typ. output characteristics



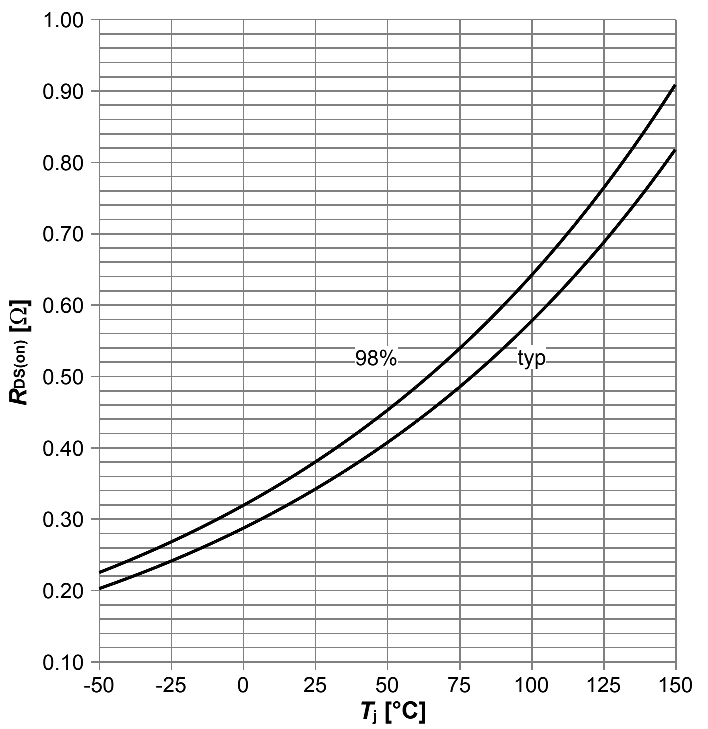
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=3.8 A; V_{GS}=10 V

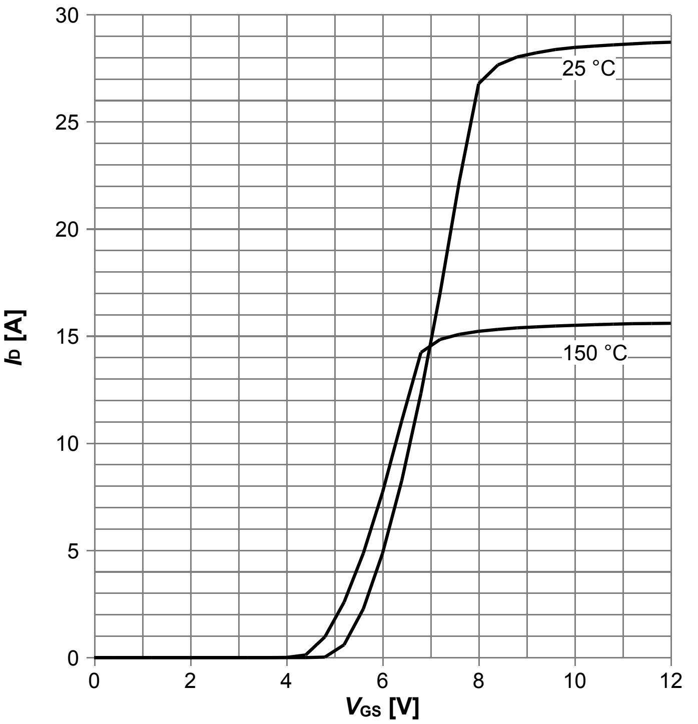
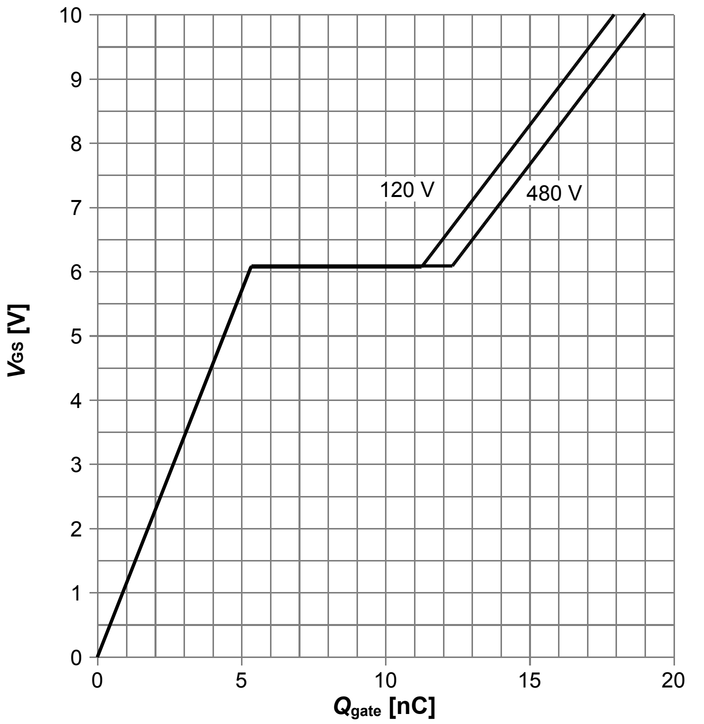
Diagram 13: Typ. transfer characteristics	Diagram 14: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=4.8 A pulsed; parameter: V_{DD}

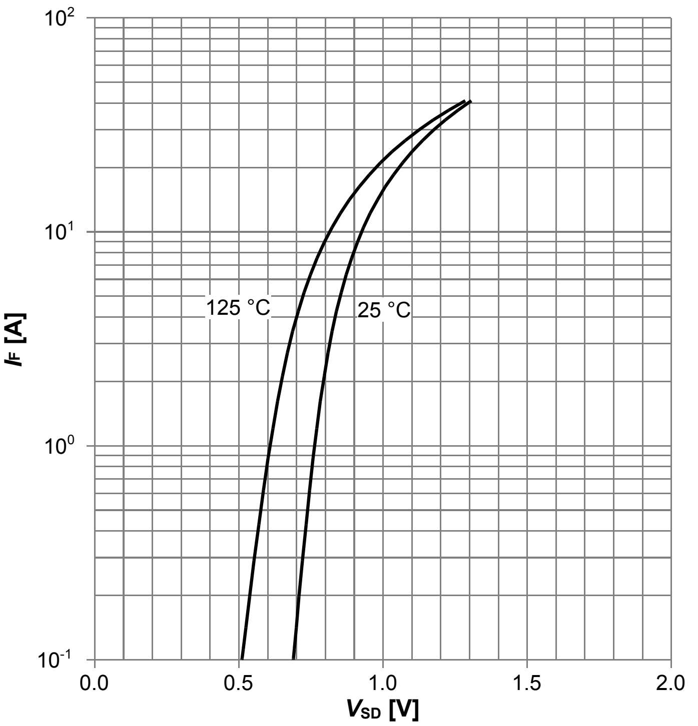
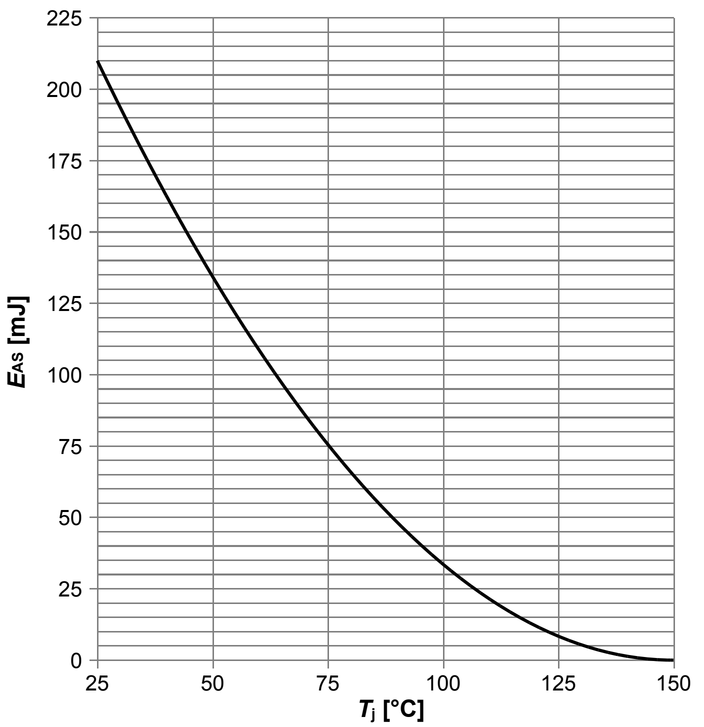
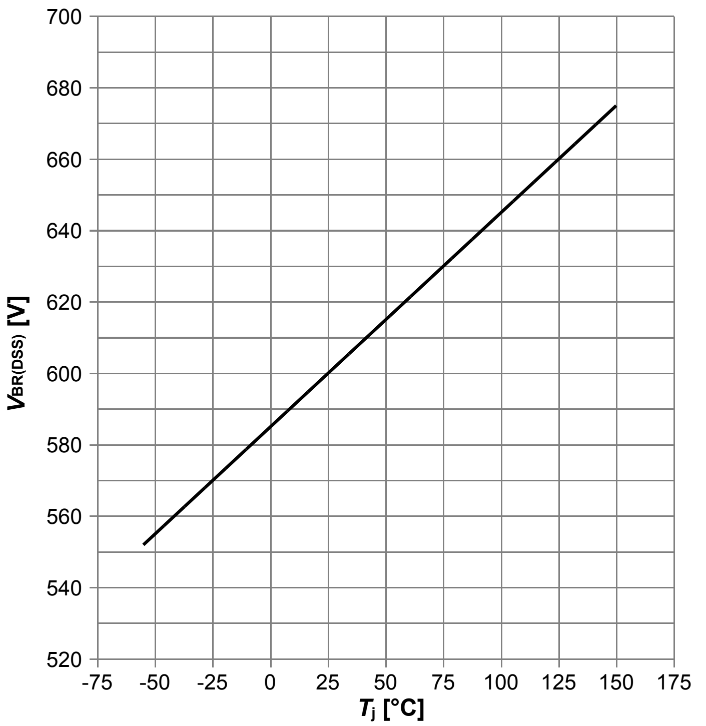
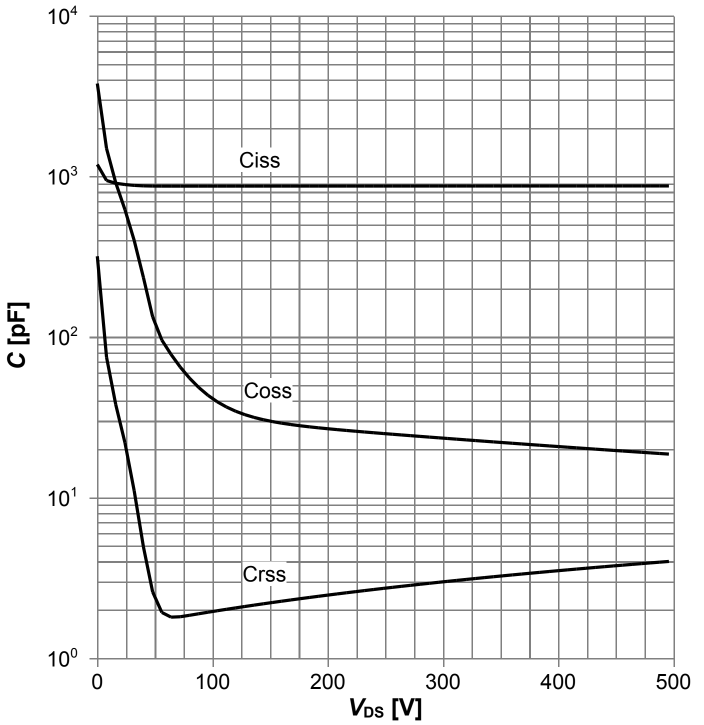
Diagram 15: Forward characteristics of reverse diode	Diagram 16: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=1.8 A; V_{DD}=50 V

Diagram 17: Drain-source breakdown voltage



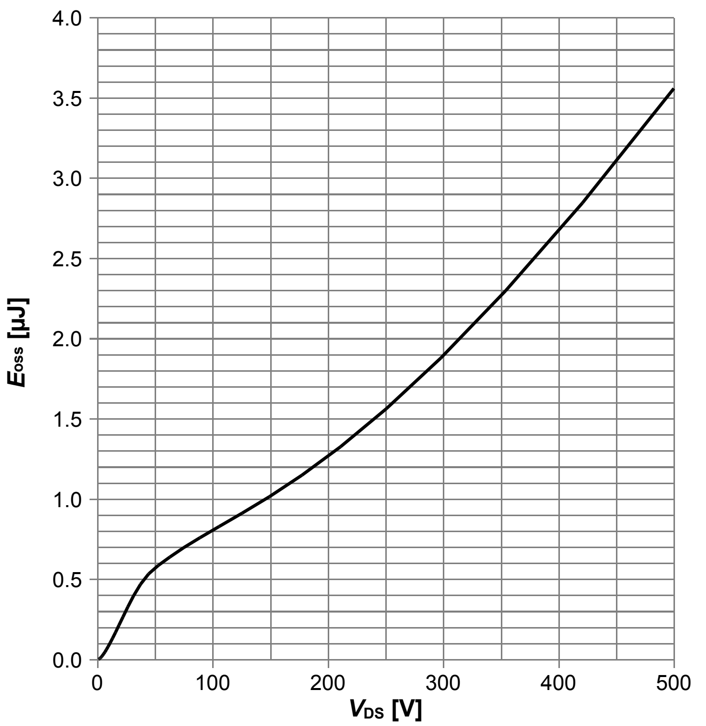
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 18: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 19: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 10 Diode characteristics

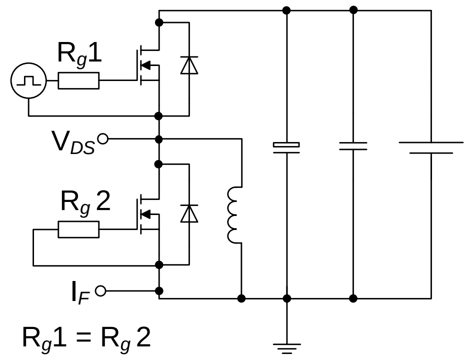
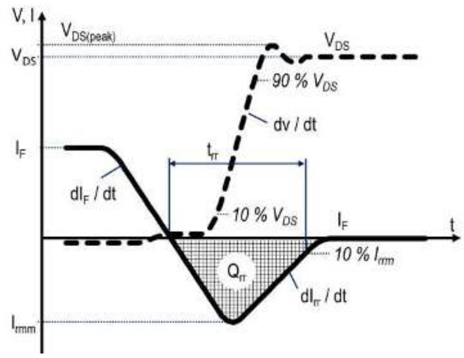
Test circuit for diode characteristics	Diode recovery waveform
	

Table 11 Switching times

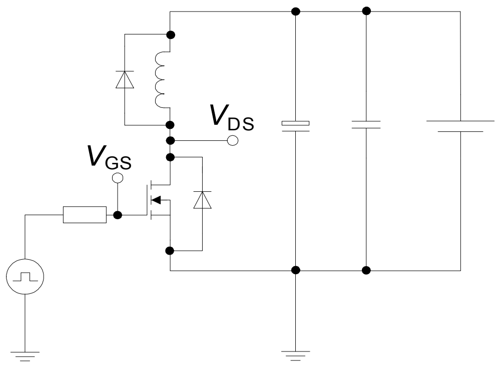
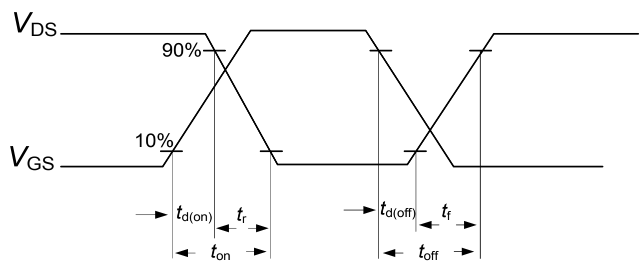
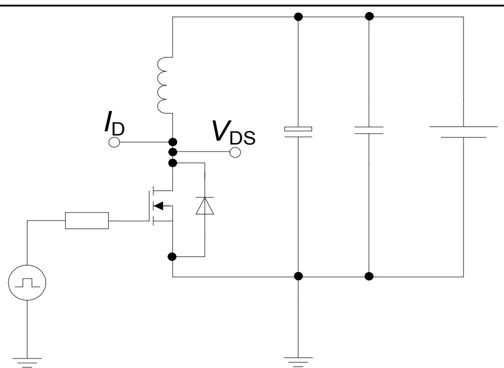
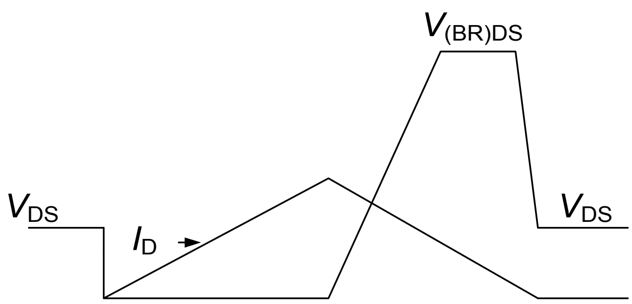
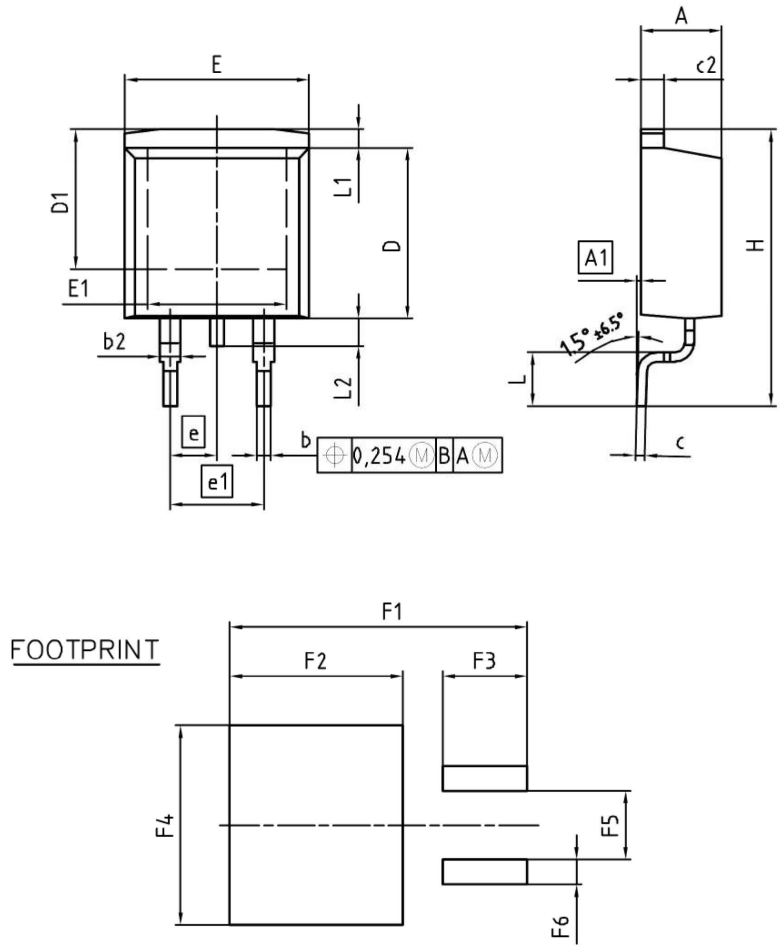
Switching times test circuit for inductive load	Switching times waveform
	

Table 12 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO.
Z8B00003324

SCALE 0 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
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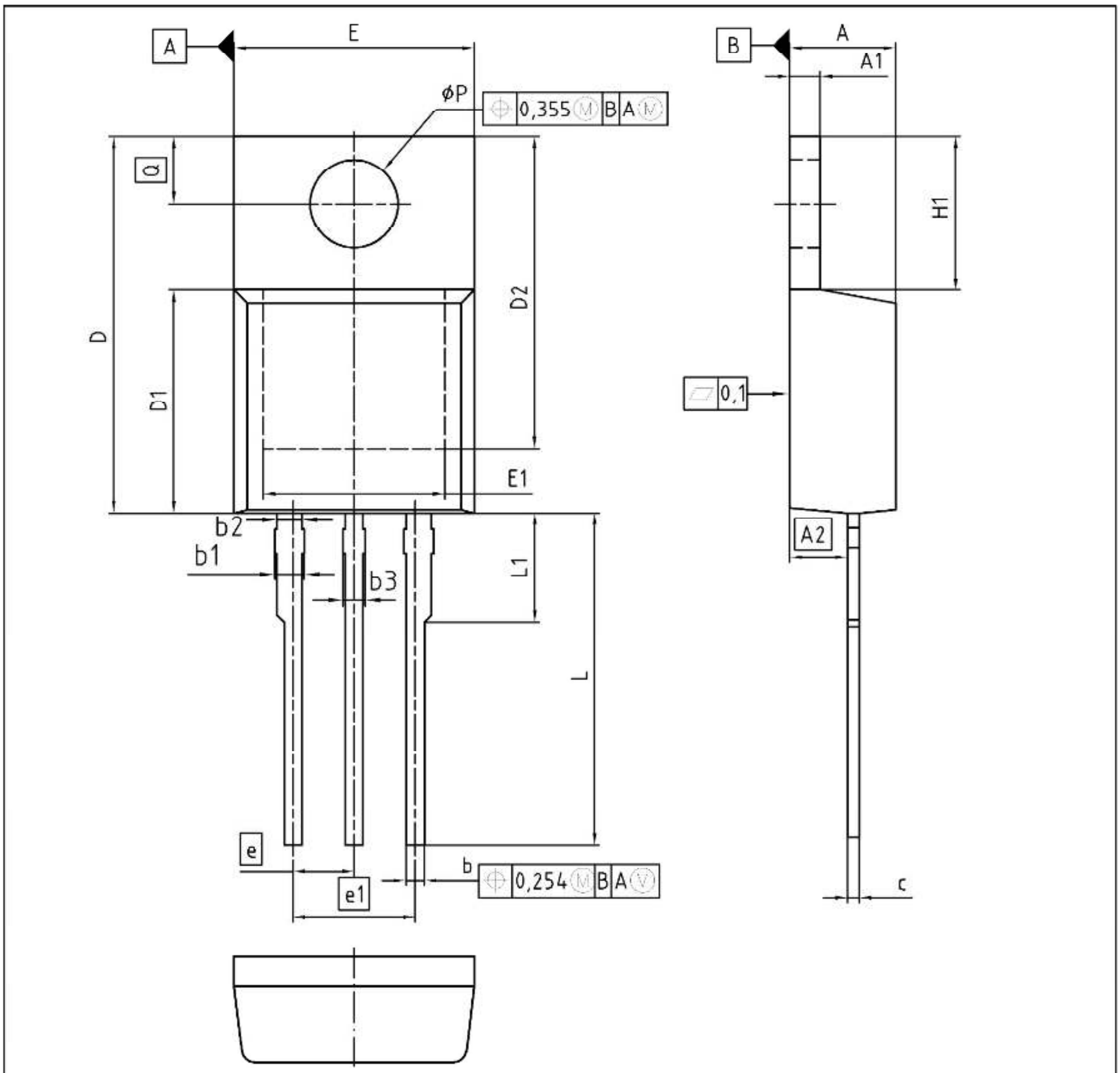
01

Figure 1 Outline PG-TO 263-3, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE 0 2.5 5mm

EUROPEAN PROJECTION

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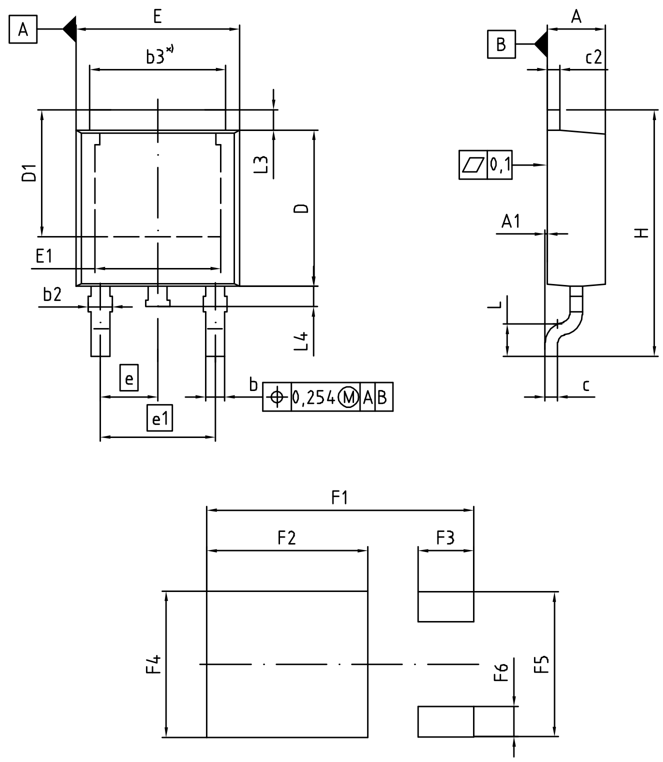
06

Figure 2 Outline PG-TO 220-3, dimensions in mm/inches

TO252-3 (DPAK)

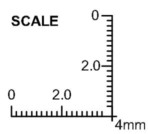


*) mold flash not included

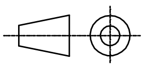
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

DOCUMENT NO.
Z8B00003328

SCALE



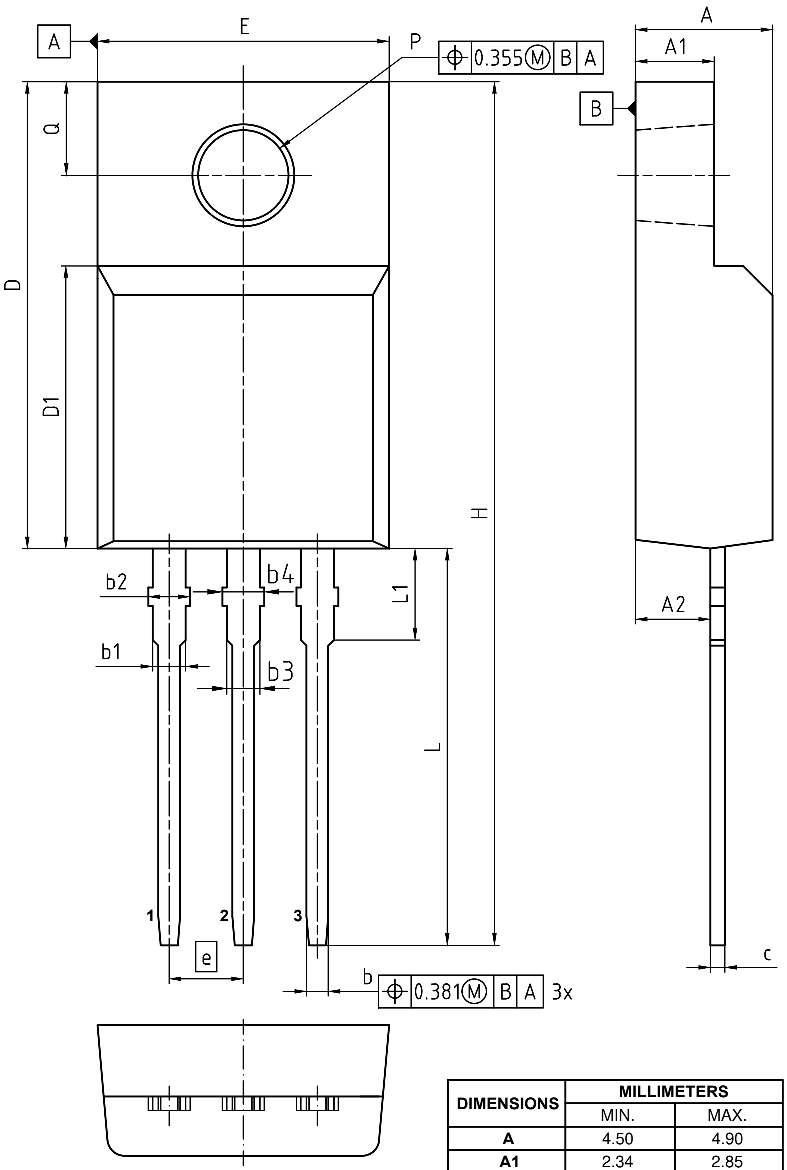
EUROPEAN PROJECTION



ISSUE DATE
16-02-2011

REVISION
04

Figure 3 Outline PG-TO 252-3, dimensions in mm/inches



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281
AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS
OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

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Z8B00003319

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07

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

ISSUE DATE
27.01.2017

Figure 4 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 13 Related Links

- **IFX CoolMOS^{TM} P6 Webpage:** www.infineon.com
- **IFX CoolMOS^{TM} P6 application note:** www.infineon.com
- **IFX CoolMOS^{TM} P6 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPB60R380P6, IPP60R380P6, IPD60R380P6, IPA60R380P6

Revision: 2017-08-22, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-12-05	Release of final version
2.1	2013-12-05	Release of multi-package datasheet
2.2	2015-07-10	PG-TO 263 package added
2.3	2017-08-22	Updated TO220 Full PAK package drawing on page 16

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