DAC161S055 Precision 16-Bit, Buffered Voltage-Output DAC

Check for Samples: DAC161S055

FEATURES

- **16-bit DAC with a Two-buffer SPI Interface**
- **Asynchronous Load DAC and Reset Pins**
- **Compatibility with 1.8V Controllers**
- **Buffered Voltage Output with Rail-to-Rail Capability**
- **Wide Voltage Reference Range of +2.5V to V_A**
- **Wide Temperature Range of −40°C to +105°C**
- **Packaged in a 16-pin WQFN**

APPLICATIONS

- **Process Control**
- **Automatic Test Equipment**
- **Programmable Voltage Sources**
- **Communication Systems**
- **Data Acquisition**
- **Industrial PLCs**
- **Portable Battery Powered Instruments**

KEY SPECIFICATIONS

- **Resolution (Specified Monotonic) 16 bits**
- **INL ±3 LSB (max)**
- **Very Low Output Noise 120 nV/$\sqrt{Hz}$ (typ)**
- **Glitch Impulse 7 nV-s (typ)**
- **Output Settling Time 5 µs (typ)**
- **Power Consumption 5.5 mW at 5.25 V (max)**

DESCRIPTION

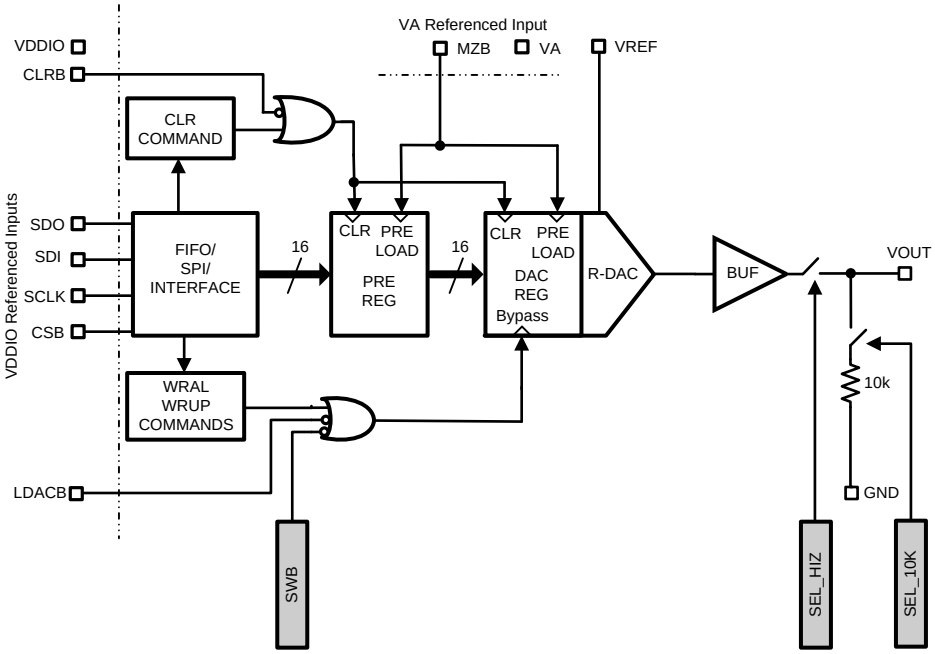
The DAC161S055 is a precision 16-bit, buffered voltage output Digital-to-Analog Converter (DAC) that operates from a 2.7V to 5.25V supply with a separate I/O supply pin that operates down to 1.7V. The on-chip precision output buffer provides rail-to-rail output swing and has a typical settling time of 5 µsec. The external voltage reference can be set between 2.5V and V_A (the analog supply voltage), providing the widest dynamic output range possible.

The 4-wire SPI compatible interface operates at clock rates up to 20 MHz. The part is capable of Diasy Chain and Data Read Back. An on board power-on-reset (POR) circuit ensures the output powers up to a known state.

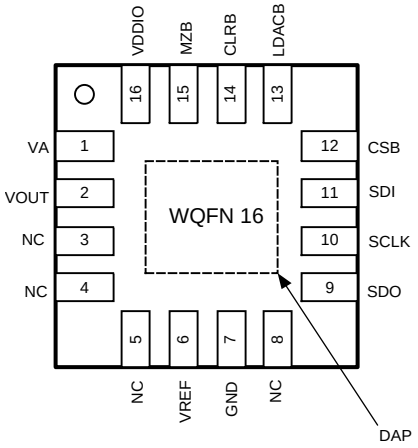
The DAC161S055 features a power-up value pin (MZB), a load DAC pin (LDACB) and a DAC clear (CLRB) pin. MZB sets the startup output voltage to either GND or mid-scale. LDACB updates the output, allowing multiple DACs to update their outputs simultaneously. CLRB can be used to reset the output signal to the value determined by MZB.

The DAC161S055 has a power-down option that reduces power consumption when the part is not in use. It is available in a 16-lead WQFN package.

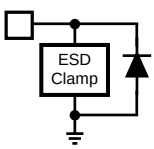
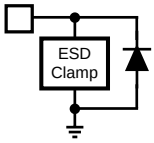
BLOCK DIAGRAM



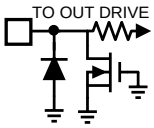
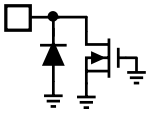
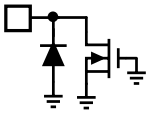
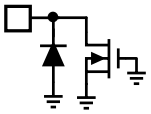
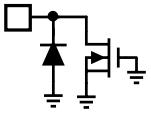
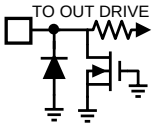
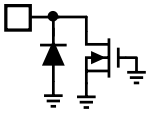
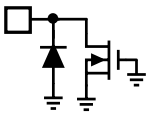
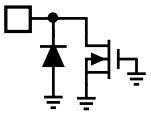
CONNECTION DIAGRAM



PIN DESCRIPTIONS

Pin Name	Pin # WQFN-16	ESD Structure	Type	Function and Connection
VDDIO	16		Power	SPI, CLRB, LDACB Supply Voltage.
VA	1		Power	Analog Supply Voltage.

PIN DESCRIPTIONS (continued)

Pin Name	Pin # WQFN-16	ESD Structure	Type	Function and Connection
VOUT	2		Analog Output	DAC output.
VREF	6		Analog Input	Voltage Reference Input.
GND	7		Ground	Ground (Analog and Digital).
SDI	11		Digital Input	SPI data input .
CSB	12		Digital Input	Chip select signal for SPI interface. On the falling edge of CSB the chip begins to accept data and output data with the SCLK signal. This pin is active low.
SCLK	10		Digital Input	Serial data clock for SPI Interface.
SDO	9		Digital Output	Data Out for daisy chain or data read back verification.
LDACB	13		Digital Input	Load DAC signal. This signal transfers DAC data from the SPI input register to the DAC output register. The signal is active low.
CLRB	14		Digital Input	Asynchronous Reset. If this pin is pulled low, the output will be updated to its power up condition set by the MZB pin. This pin is active low.
MZB	15		Digital Input	Power up at Zero/Mid-scale. Tie this pin to GND to power up to Zero or to VA to power up to mid-scale.
NC	3,4,5,8			No connect pins. Connect to GND in board layout will result in the lowest amount of coupled noise.
DAP	DAP			Attach die attach paddle to GND for best noise performance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)

Supply Voltage, V_A	−0.3V to 6.0V
Supply Voltage V_{DDIO}	−0.3V to V_A+0.3V
Any pin relative to GND	6V, −0.3V
Voltage on MZB or VREF Input Pin (3)	−0.3V to V_A+0.3V
Voltage on any other Input Pin (3)	−0.3V to V_{DDIO}+0.3V
Voltage on V_{OUT} (3)	−0.3V to V_A+0.3V
Voltage on SDO (3)	−0.3V to V_{DDIO}+0.3V
Input Current at Any Pin (3)	5mA
Output Current Source or Sink by Vout	10mA
Output Current Source or Sink by SDO	3mA
Total Package Input and Output Current	20mA
ESD Susceptibility Human Body Model Machine Model Charged Device Model (CDM)	 3000V 250V 1250V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
For soldering specifications: see product folder at www.ti.com and SNOA549	

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) The Electrical characteristics tables list specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are **NOT** specified.

(3) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > VDD) the current at that pin must be limited to 5mA and V_I has to be within the Absolute Maximum Rating for that pin. The 20mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four.

RECOMMENDED OPERATING CONDITIONS (1) (2)

Operating Temperature Range	−40°C to +105°C
Supply Voltage, V_A	+2.7V to 5.25V
Supply Voltage VDDIO	+1.7 V to V_A
Reference Voltage VREF	+2.5V to V_A
Digital Input Voltage	0 to VDDIO
Output Load	0 to 200 pF
Package Thermal Resistance θ_{JA} (3) θ_{JC}	 41°C/W 6.5°C/W

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(2) The Electrical characteristics tables list specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are **NOT** specified.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$ and θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D=(T_{J(MAX)}-T_A)/\theta_{JA}$

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_A = 2.7V to 5.25V, VDDIO = V_A, VREF = 2.5V to VA, RL = 10k to GND, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 512 to 65023. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$**: all other limits apply to T_A = 25°C, unless otherwise specified.(1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PERFORMANCE						
N	Resolution		16			Bits
INL	Integral Non-Linearity	No load. From code 512 to Full Scale - 512. V_A=5V, V_{REF}=4.096V		± 1	**±3**	LSB
DNL	Differential Non-Linearity	No load. From code 512 to Full Scale - 512. V_A=5V, V_{REF}=4.096V	**-1**		**1.1**	LSB
ZE	Zero Code Error			4	**15**	mV
FSE	Full Scale Error		**-15**		**15**	mV
OE	Offset Error		**-11**	±1	**11**	mV
	Offset Error Drift			±4		µV/°C
GE	Gain Error	No load. From code 512 to Full Scale - 512. V_A=5V, V_{REF}=4.096V		±0.05		% of FS
			-25		**25**	mV
	Gain Temperature Coefficient	No load. From code 512 to Full Scale - 512. V_A=5V, V_{REF}=4.096V		± 2		ppm FS/°C
REFERENCE INPUT CHARACTERISTICS						
V_{REF}	Reference Input Voltage Range	V_A = 2.7V to 5.25V	2.5		V_A	V
	Reference Input Impedance			12.5		kΩ
ANALOG OUTPUT CHARACTERISTICS						
	Output Voltage Range	No load.	**0.015**		**VA-0.04**	V
	DC Output Impedance			2		Ω
ZCO	Zero Code Output	V_A=3V, I_{OUT}=200 µA; V_{REF}=2.5		3		mV
		V_A=3V, I_{OUT}=1mA; V_{REF}=2.5		4		
		V_A=5V, I_{OUT}=200 µA; V_{REF}=4.096		4		
		V_A=5V, I_{OUT}=1mA; V_{REF}=4.096		4		
FSO	Full Scale Output	V_A=3V, I_{OUT}=200 µA; V_{REF}=2.5		2.495		V
		V_A=3V, I_{OUT}=1mA; V_{REF}=2.5		2.494		
		V_A=5V, I_{OUT}=200 µA; V_{REF}=4.096		4.091		
		V_A=5V, I_{OUT}=1mA; V_{REF}=4.096		4.089		
C_L	Maximum Capacitive Load	Parallel R = 10KΩ		500		pF
		Series R = 50Ω		15		µF
R_L	Minimum Resistive Load			10		kΩ
I_{SC}	Short Circuit Current	VA = +5V, V_{REF}=4.096		353		mA
t_{PU}	Power-up Time	From Power Down Mode		25		ms
ANALOG OUTPUT DYNAMIC CHARCTERISTICS						
SR	Voltage Output Slew Rate	Positive and negative		2		V/µs
t_s	Voltage Output Settling Time	1/4 scale to 3/4 scale V_{REF}= VA = +5V, settle to ±1 LSB.		5		µs
	Digital Feedthrough	Code 0, all digital inputs from GND to VDDIO		1		nV-s
	Major Code Transition Analog Glitch Impulse	V_A=5V, V_{REF}=2.5V. Transition from mid-scale − 1LSB to mid-scale.		7		nV-s

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) The Electrical characteristics tables list specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are **NOT** specified.

(3) Typical values represent most likely parametric norms at specific conditions (Example VA; specific temperature) and at the recommended Operating Conditions at the time of product characterizations and are **NOT** specified.

ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for V_A = 2.7V to 5.25V, VDDIO = V_A, VREF = 2.5V to VA, RL = 10k to GND, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 512 to 65023. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$**: all other limits apply to T_A = 25°C, unless otherwise specified.(1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Output Noise	Spot noise at 20 kHz		120		nV/√Hz
	Integrated Output Noise	1Hz to 10 kHz		18		µV
DIGITAL INPUT CHARACTERISTICS						
I_{IN}	Input Current				**±1**	µA
V_{IL}	Input Low Voltage	VDDIO=5V			**0.8**	V
		VDDIO=3V			**0.8**	
		VDDIO=1.8V			**0.4**	
V_{IH}	Input High Voltage	VDDIO=5V	**2.1**			V
		VDDIO=3V	**2.1**			
		VDDIO=1.8V	**1.4**			
V_{ILMZB}	MZB Input Low Voltage	VA=5V			**0.8**	V
		VA=3V			**0.8**	V
V_{IHMZB}	MZB Input High Voltage	VA=5V	**2.1**			V
		VA=3V	**2.1**			V
C_{IN}	Input Capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OL}	Output Low Voltage	Isink=200 µA; VDDIO>3V			**400**	mV
		Isink=2mA;VDDIO>3V			**400**	
		Isink=200 µA; VDDIO=1.8V			**400**	
		Isink=2mA;VDDIO=1.8V			**400**	
V_{OH}	Output High Voltage	Isink=200 µA; VDDIO>3V	**VDDIO - 0.2**			V
		Isink=2mA;VDDIO>3V	**VDDIO - 0.2**			
		Isink=200 µA; VDDIO=1.8V	**VDDIO - 0.2**			
		Isink=2mA;VDDIO=1.8V	**1.15**			
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current			<1n	**±1µ**	A
C_{OUT}	TRI-STATE Output Capacitance			4		pF
POWER REQUIREMENTS						
V_A	Analog Supply Voltage Range		**2.7**		**5.25**	V
VDDIO	Digital Supply Voltage Range		**1.7**		**VA**	V
I_{VA}	VA Supply Current	No load. SCLK Idle. All digital inputs at GND or VDDIO. VA=5V		0.75	**1**	mA
		No load. SCLK Idle. All digital inputs at GND or VDDIO. VA=3.3V		0.62	**1**	mA
I_{REF}	Reference Current				**350**	µA
I_{PDVA}	VA Power Down Supply Current	All digital inputs at GND or VDDIO		0.5	**3**	
I_{PDVO}	VDDIO Power Down Supply Current	All digital inputs at GND or VDDIO			**1**	
I_{PDVR}	VREF Power Down Supply Current				**1**	

DIGITAL INTERFACE TIMING CHARACTERISTICS

These specifications apply for V_A = 2.7V to 5.25V, VDDIO = 1.7V to V_A, C_L = 200 pF. **Boldface limits apply for T_A = −40°C to 105°C**. All other limits apply to T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCLK}	SCLK Frequency	VDDIO=1.7V to 2.7V	0		**10**	MHz
		VDDIO=2.7V to 5.25V	0		**20**	
t_H	SCLK High Time		**15**	25		ns
t_L	SCLK Low Time		**20**	25		
t_{CSB}	CSB High Pulse width	VDDIO=1.7V to 2.7V		75		
		VDDIO=2.7V to 5.25V		40		
t_{CSS}	CSB Set-up Time Prior to SCLK Rising edge		**10**			
t_{CSH}	CSB Hold Time after the 24th Falling Edge of SCLK			0		
t_{ZSDO}	CSB Falling Edge to SDO Valid	VDDIO=1.8V		40		
		VDDIO=3V		10		
		VDDIO=5V		6		
t_{SDOZ}	CSB Rising Edge to SDO HiZ	VDDIO=1.8V		75		
		VDDIO=3V		40		
		VDDIO=5V		27		
t_{CLRS}	CSB Rising Edge to CLRB Falling Edge	CLRB must not transition anytime CSB is low.		5		
t_{LDACS}	CSB Rising Edge to LDACB Falling Edge	LDACB must not transition anytime CSB is low.		5		
t_{LDAC}	LDACB Low Time		**10**	2.5		
t_{CLR}	CLRB Low Time		**10**	2.5		
t_{DS}	SDI Data Set-up Time prior to SCLK Rising Edge			10		
t_{DH}	SDI Data Hold Time after SCLK Rising Edge			0		
t_{DO}	SDO Output Data Valid	VDDIO=1.7			**62**	
		VDDIO=3.3			**25**	
		VDDIO=5			**15**	

TIMING DIAGRAMS

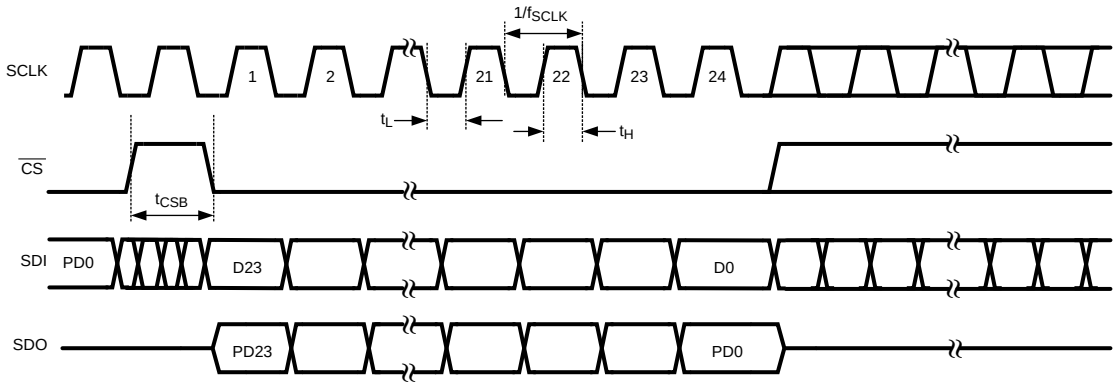


Figure 1. DAC161S055 Input/Output Waveforms

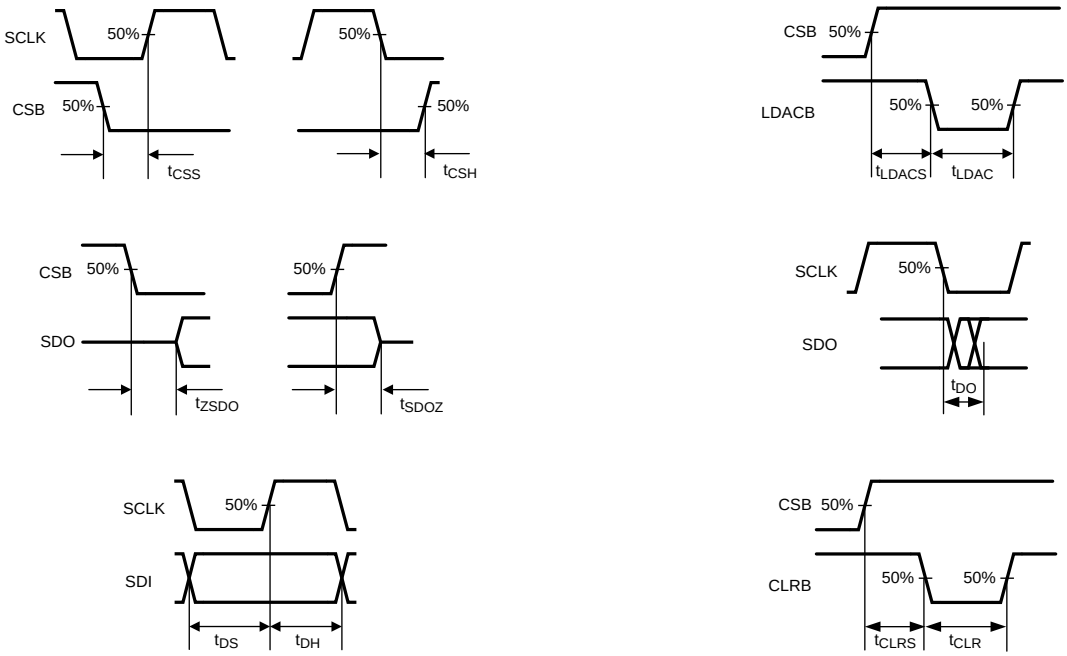


Figure 2. Timing Parameter Specifics

TRANSFER CHARACTERISTICS

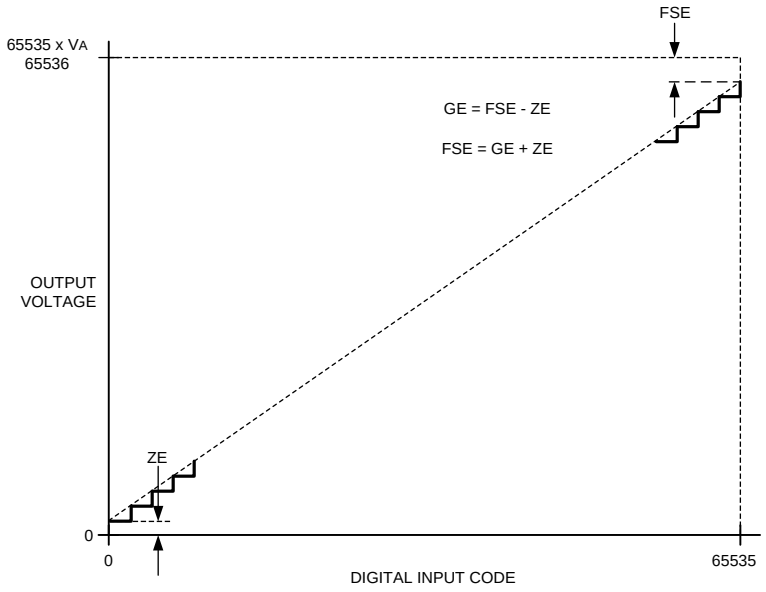


Figure 3. Input/Output Transfer Characteristic

SPECIFICATION DEFINITIONS

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 65536.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of V_{REF} x 65535 / 65536.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON_LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (MSB) is the bit that has the smallest value or weight of all bits in a word. This value is LSB = V_{REF} / 2^n where V_{REF} is the reference voltage for this product, and "n" is the DAC resolution in bits, which is 16 for the DAC161S055.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained, although some ringing may be present.

MONOTONICITY is the condition of being monotonic, where the DAC output never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_{REF}.

OFFSET ERROR is the difference between zero voltage and a where a straight line fit to the actual transfer function intersects the y axis.

SETTLING TIME is the time for the output to settle to within 1 LSB of the final value after the input code is updated.

WAKE-UP TIME is the time for the output to recover after the device is commanded to the active mode from any of the power down modes.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 0000h has been entered.

TYPICAL PERFORMANCE CHARACTERISTICS

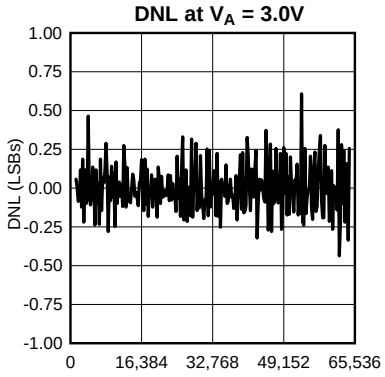


Figure 4.

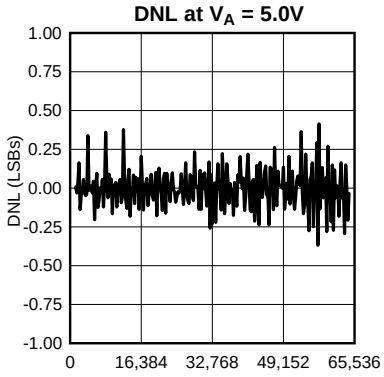


Figure 5.

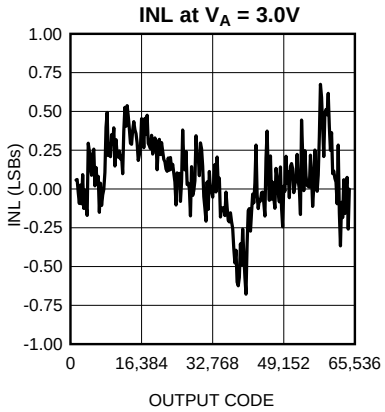


Figure 6.

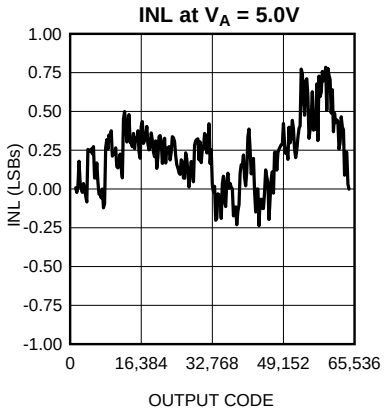


Figure 7.

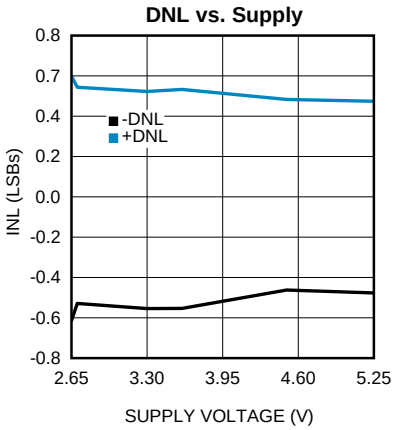


Figure 8.

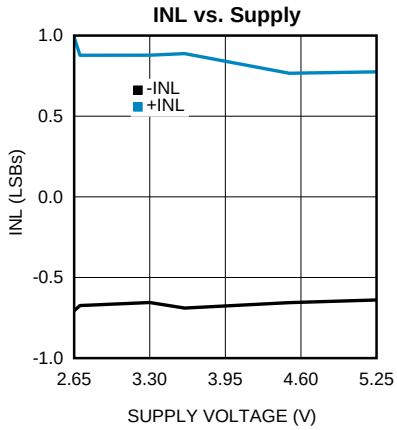


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

DNL vs. V_{REF}, V_A=5V

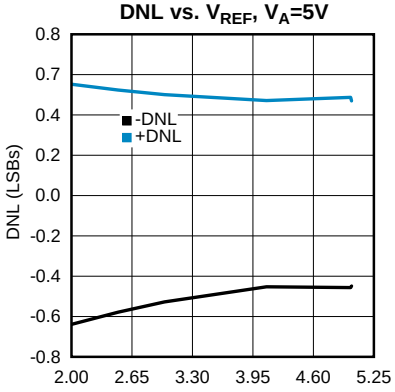


Figure 10.

INL vs. V_{REF}, V_A=5V

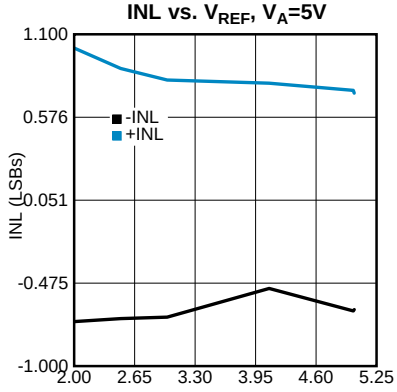


Figure 11.

DNL vs. Temperature, V_A=5V, V_{REF}=4.096

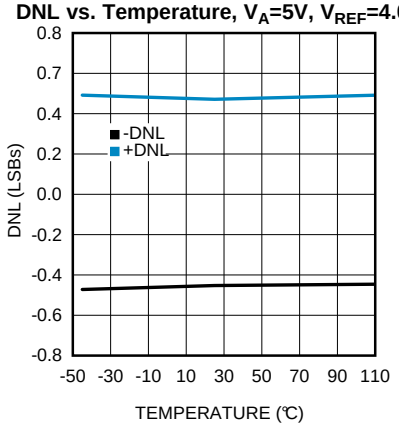


Figure 12.

INL vs. Temperature, V_A=5V, V_{REF}=4.096

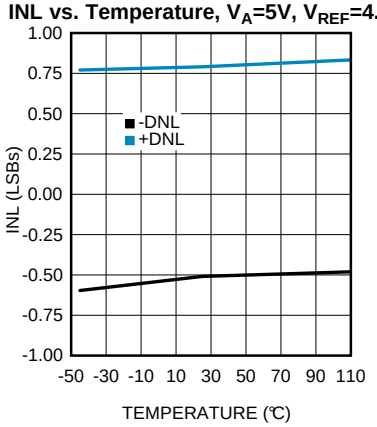


Figure 13.

Zero Code Error vs. I_{OUT}

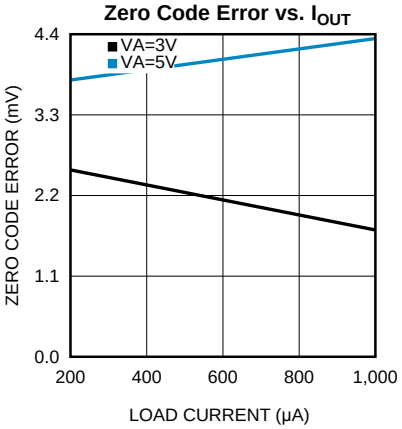


Figure 14.

Full Scale Error vs. I_{OUT}

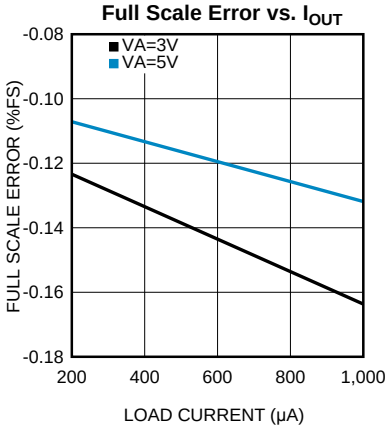


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

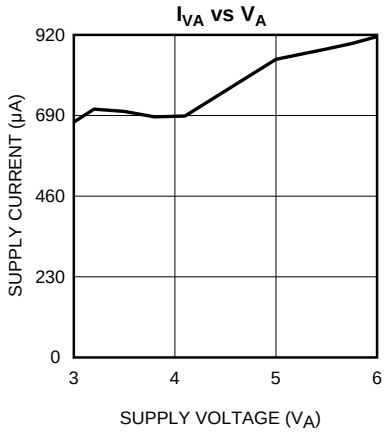


Figure 16.

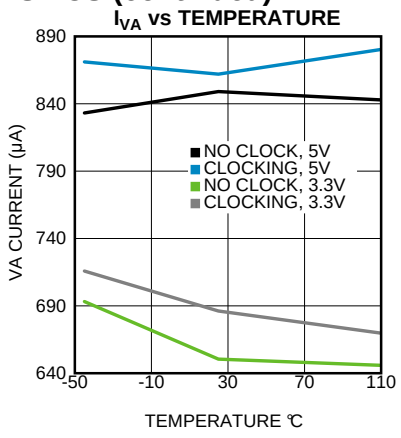


Figure 17.

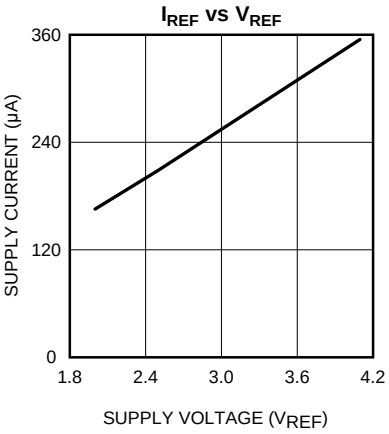


Figure 18.

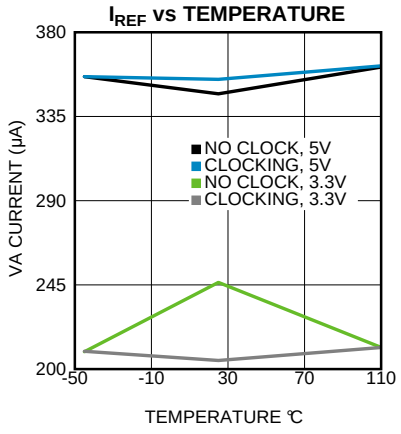


Figure 19.

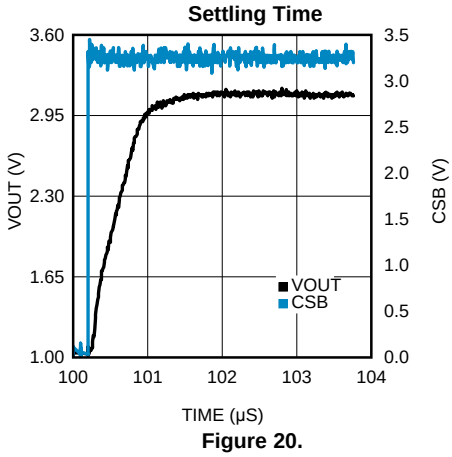


Figure 20.

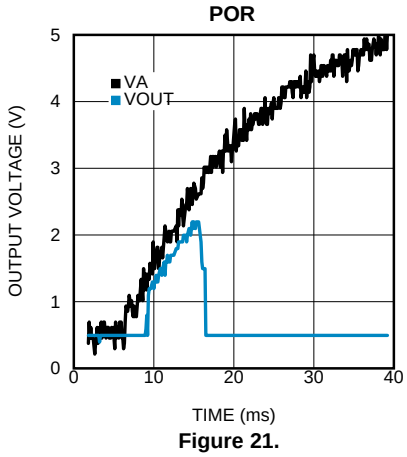


Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

5V Glitch Response

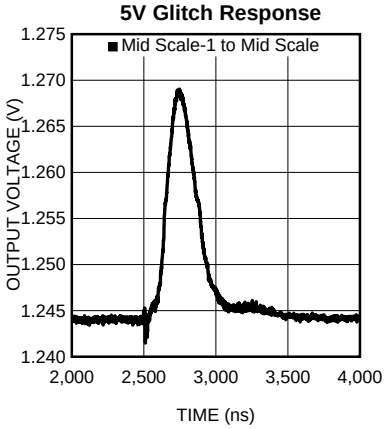


Figure 22.

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE OVERVIEW

The DAC161S055 uses a resistor array to convert the input code to an analog signal, which in turn is buffered by the rail-to-rail output amplifier. The resistor array is factory trimmed to achieve 16-bit accuracy.

An SPI interface shifts the input codes into the device. The acquired input code is stored in the PREREG register. After the input code is transferred to the DACREG register it affects the state of the resistor array and the output level of the DAC. The transfer can be initiated by the type of write command used, by a software LDAC command or by the state of the LDACB pin.

The user can control the power up state of the output using the MZB pin and the power down state of the output using the CONFIG register. Additionally, there are external pins and CONFIG register bits that also control clearing the DAC.

NOTE

Although the DAC161S055 is a single channel device, the instruction set is for multichannel DACs. The user must address channel 0 (A2,A1,A0={000}).

OUTPUT AMPLIFIER

The output buffer amplifier is a rail to rail type which buffers the signal produced by the resistor array and drives the external load. All amplifiers, including rail to rail amplifiers, exhibit a loss of linearity as the output nears the power rails (in this case GND and V_A). Thus the linearity of the part is specified over less than the full output range. The user can program the CONFIG register to power down the amplifier and either place it in the high impedance state (HiZ), or have the output terminated by an internal 10 kΩ pull-down resistor.

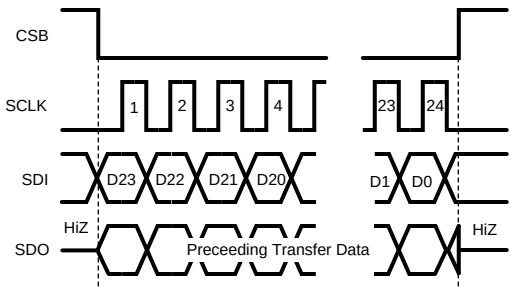
REFERENCE

An external reference source is required to produce an output. The reference input is not internally buffered and presents a resistive load to the external source. Loading presented by the VREF pin varies by about 12.5% depending on the input code. Thus a low impedance reference should be used for best results.

SERIAL INTERFACE

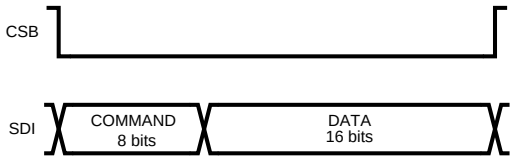
The 4-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the TIMING DIAGRAMS for timing information about the read and write sequences. The serial interface is the four signals CSB, SCLK, SDI and SDO.

A bus transaction is initiated by the falling edge of the CSB. Once CSB is low, the input data is sampled at the SDI pin by the rising edge of the SCLK. The output data is put out on the SDO pin on the falling edge of SCLK. At least 24 SCLK cycles are required for a valid transfer to occur. If CSB is raised before 24th rising edge of the SCLK, the transfer is aborted. If the CSB is held low after the 24th falling edge of the SCLK, the data will continue to flow through the FIFO and out the SDO pin. Once CSB transitions high, the internal controller will decode the most recent 24 bits that were received before the rising edge of CSB. The DAC will then change state depending on the instruction sent and the state of the LDACB pin.



The acquired data is shifted into an internal 24 bit shift register (MSB first) which is configured as a 24 bit deep FIFO. As the data is being shifted into the FIFO via the SDI pin, the prior contents of the register are being shifted out through the SDO output. While CSB is high, SDO is in a high-Z state. At the falling edge of CSB, SDO presents the MSB of the data present in the shift register. SDO is updated on every subsequent falling edge of SCLK (note — the first SDO transition will happen on the first falling edge AFTER the first rising edge of SCLK when CSB is low).

The 24 bits of data contained in the FIFO are interpreted as an 8 bit COMMAND word followed by 16 bits of DATA. The general format of the 24 bit data stream is shown below. The full Instruction Set is tabulated in Section INSTRUCTION SET.



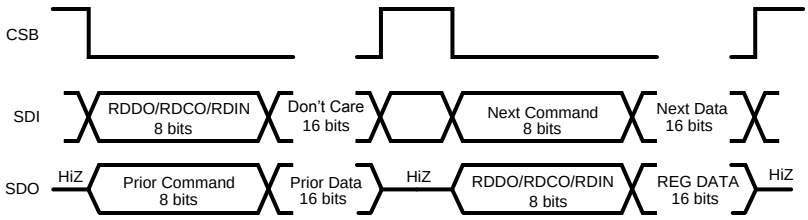
1.4.1 SPI Write

SPI write operation is the simplest transaction available to the user. There is no handshaking between master and the slave (DAC161S055), and the master is the source of all signals required for communication: SCLK, CSB, SDI. The format of the data transfer is described in the section 1.4. The user instruction set is shown in Section INSTRUCTION SET.

SPI Read

The read operation requires all 4 wires of the SPI interface: SCLK, SCB, SDI, SDO. The simplest READ operation occurs automatically during any valid transaction on the SPI bus since SDO pin of DAC161S055 always shifts out the contents of the internal FIFO. Therefore the user can verify the data being shifted in to the FIFO by initiating another transaction and acquiring data at SDO. This allows for verification of the FIFO contents only.

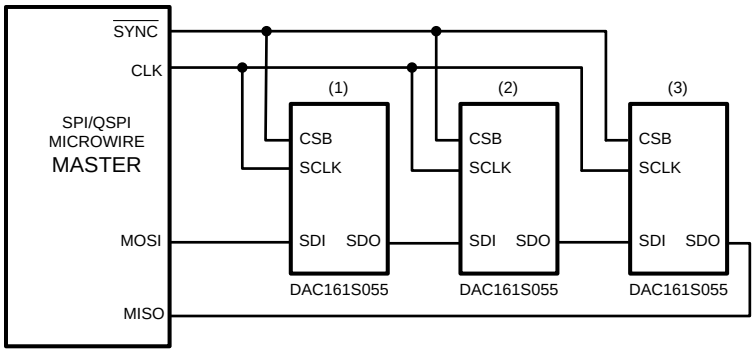
The 3 internal registers (PREREG, DACREG, CONFIG) can be accessed by the user through the Register Read commands: RDDO, RDIN, RDCO respectively (see Section INSTRUCTION SET). These operations require 2 SPI transaction to recover the register data. The first transaction shifts in the Register Read command; an 8 bit command byte followed by 16 bit “dummy” data. The Register Read command will cause the transfer of contents of the internal register into the FIFO. The second transaction will shift out the FIFO contents; an 8 bit command byte (which is a copy of previous transaction) followed by the register data. The Register Read operation is shown in the figure below.



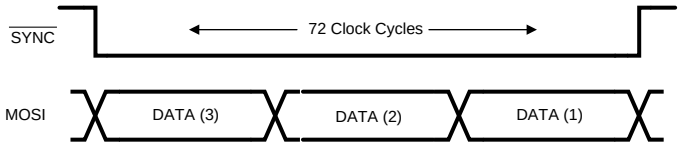
SPI Daisy Chain

It is possible to control multiple DACs or other SPI devices with a single master equipped with one SPI interface. This is accomplished by connecting the DACs in a Daisy Chain. The scheme is depicted in the figure below. An arbitrary length of the chain and an arbitrary number of control bits for other devices in the chain is possible since individual DAC devices do not count the data bits shifted in. Instead, they wait to decode the contents of their respective shift registers until CSB is raised high.

A typical bus cycle for this scheme is initiated by the falling CSB. After the 24 SCLK cycles new data starts to appear at the SDO pin of the first device in the chain, and starts shifting into the second device. After 72 SCLK cycles following the falling CSB edge, all three devices in this example will contain new data in their input shift registers. Raising CSB will begin the process of decoding data in each DAC. When in the Daisy Chain the full READ and WRITE capability of every device is maintained.



A sample of SPI data transfer appropriate for a 3 DAC Daisy Chain is shown in the figure below.



POWER-UP DEFAULT OUTPUT

It is possible to power up the DAC with the output either at GND or midscale. This functionality is achieved by connecting the MZB pin either to GND or to VA (note, the MZB pin is referenced to VA, not VDDIO). Usually this function is hardwired in the application, but can also be controlled by a GPIO pin of the µC. To power up with output at zero, tie the MZB pin low. To power up with output at midscale, tie MZB high. The MZB pin is level sensitive.

CHANGING DAC OUTPUT

There are multiple different ways to affect the DAC output. The CONFIG register can be changed so that a write to the PREREG is seen instantly at the output. The LDAC function or LDACB pin updates the output instantly. Finally, the type of write command (WRUP, WRAL, WR) can affect if the output updates instantly or not.

Write-Through and Write-Block Modes

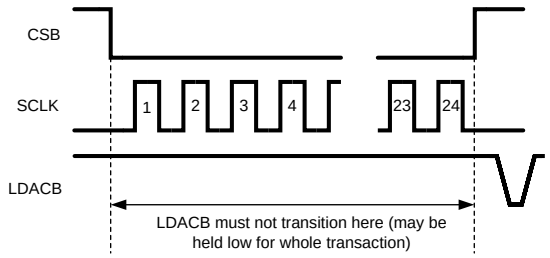
Using the SWB bit of the CONFIG register, the user can set the part in **WRITE-BLOCK** or **WRITE-THROUGH** mode.

If the DAC channel is configured in the **WRITE-BLOCK** mode (SWB=0, default), the DAC input DATA is held in the PREREG until the controller forces the transfer of DATA from PREREG to DACREG register. Only DATA in DACREG register is converted to the equivalent analog output. The transfer from PREREG into DACREG can be forced by both software and hardware LDAC commands. The Data Writing commands WRUP and WRAL update both PREREG and DACREG at the same time regardless of the channel mode. **WRITE-BLOCK** mode is used in multi device or multi channel applications. A user can preload all DAC channels with desired data, in multiple SPI transactions, and then issue a single software LDAC command (or toggle the LDACB pin) to simultaneously update all analog outputs.

If the DAC channel is configured in **WRITE-THROUGH** mode (SWB=1) the controller updates both PREREG and DACREG registers simultaneously. Therefore in WRITE-THROUGH mode the channel output is updated as soon as the SPI transfer is completed i.e. upon the rising edge of CSB.

LDAC Function

The LDACB (Load DAC) pin provides a easy way to synchronize several DACs and update the output without any SPI latency. If the LDACB is asserted low, the content of the PREREG register is instantaneously moved into the DACREG register. The LDACB pin is level sensitive. If the LDACB pin is held low continuously, the DAC output will update as soon as the CSB pin goes high.



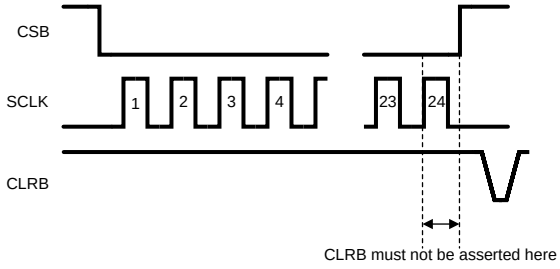
The DAC Configuration command LDAC (see Section INSTRUCTION SET below) will also update the DAC output as soon as it is received. The effect of hardware LDACB or software LDAC is the same i.e. data is transferred from the PREREG to DACREG and output of the DAC is updated.

Write Commands

There are three write commands available in the DAC command set. Issuing a WR command causes the DAC to update either the PREREG or the DACREG depending on the setting of the SWB bit (see Section Write-Through and Write-Block Modes). Issuing a WRUP command causes the specified channels output (for multiple channel parts) to update immediately, regardless of the SWB bit setting. Issuing a WRAL command causes all channels (for multiple channel parts) to update immediately with the same data, regardless of the SWB bit setting.

CLEAR FUNCTION

The CLRB pin provides a easy way to reset the DAC161S055 output. If the CLRB pin goes low, VOUT instantaneously slews to the value indicated by the MZB pin, either zero or midscale. The CLRB pin is level sensitive.



Clear function can also be accessed via the software instruction CLR, see Section INSTRUCTION SET below. The effect of hardware CLRB or software CLR is the same.

POWER ON RESET

An on-chip power on reset circuit (POR) ensures that the DAC always powers on in the same state. The registers will be loaded with the defaults shown in Section INSTRUCTION SET. The output state will be controlled by the state of the MZB pin.

POWER DOWN

Power down is achieved by writing the PD instruction and setting the appropriate bit to a logic '1'. In the PD command, it is possible to specify if the output is left in a high impedance (HIZ) state or if it is pulled to GND through a 10K resistor. During power down, the output amplifier is disabled and the resistor ladder is disconnected from Vref. The SPI interface remains active. To exit power down, write the PD command again, setting the appropriate bit to a logic '0'. Note that the SPI interface and the registers are all active during power down.

INTERNAL REGISTERS

There are 3 registers that are accessible to the user. The data registers (PREREG and DACREG) are both readable and writable from the command set. The CONFIG register is only readable from the command set. Bits in the CONFIG register are set by the commands detailed in Section INSTRUCTION SET.

PREREG: DAC Preload Data Register(16Bits)

	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MSB	PRD15	PRD14	PRD13	PRD12	PRD11	PRD10	PRD9	PRD8
	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LSB	PRD7	PRD6	PRD5	PRD4	PRD3	PRD2	PRD1	PRD0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bit15–0: 16 bit data word to be converted. Bit 15 has a weight of 1/2*Vref. Bit 0 has a weight of $Vref/2^{16}$.

DACREG: DAC Output Data Register(16Bits)

	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MSB	IND15	IND14	IND13	IND12	IND11	IND10	IND9	IND8
	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LSB	IND7	IND6	IND5	IND4	IND3	IND2	IND1	IND0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bit15–0: 16 bit data word to be converted. Bit 15 has a weight of 1/2*Vref. Bit 0 has a weight of $Vref/2^{16}$.

CONFIG: DAC Configuration Reporting Register (8 Bits)

	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LSB	IND7	IND6	IND5	IND4	IND3	IND2	IND1	IND0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bit7–3: Reserved. Read value is undefined and should be discarded.

Bit2: SWB: Set Write Block bit

0: Channel is in WRITE THROUGH mode.

1: Channel is in WRITE BLOCK mode.

Bit1: 0: Channel is either active or SEL_HIZ is set.

1: Channel is powered down and output is terminated by a 10K resistor to GND.

Bit0: 0: Channel is either active or SEL_10K is set.

1: Channel is powered down and output is in high impedance state.

INSTRUCTION SET

The instruction set for the DAC161S055 is common to the family of single and multi channel devices (DAC16xS055). The DAC161S055 has only a single channel — Channel 0.

NOTE

DATA WRITING and REGISTER READING instructions encode the channel address as a binary triplet (A2,A1,A0) as the last three LSBs of the command byte. DAC CONFIGURATION instructions encode the channel selection by a bit set in the data bytes. For example, when executing the LDAC instruction a payload of {0100 0001} in the least significant byte of the instruction indicates channels 6 and 0 are targeted.

MNEMONIC	Command Byte[7:0]								DATA[15:8]	DATA [7:0]	Description	DEFAULT
DAC Configuration												
NOP	0	0	0	0	0	0	0	0	xxxx xxxx	xxxx xxxx	No Operation	
CLR	0	0	0	0	0	0	0	1	xxxx xxxx	xxxx xxxx	Clear internal registers, return to Power-Up default state	
LDAC	0	0	0	1	1	0	0	0	xxxx xxxx	CHANNEL[7:0]	Software LOAD DAC. A '1' causes data stored in the specified channel's PREREG to be transferred to DACREG and the output updated.	
SWB	0	0	1	0	1	0	0	0	xxxx xxxx	CHANNEL[7:0]	Set WRITE BLOCK or WRITE THROUGH for the selected channels.	00FFh
											0: WRITE THROUGH	
											1: WRITE BLOCK	
PD	0	0	1	1	0	0	0	0	CHANNEL[7:0]	CHANNEL[7:0]	Sets SEL_10K or SEL_HIZ. Upper 8 bits PD Hi-Z; Lower 8-bits PD 10K; if both are 1's; PD -> 10K	0000h
											1: Upper 8 bits: SEL_HIZ	
											1: Lower 8 bits: SEL_10K	
											1: Both upper and lower: SEL_10K	
Data Writing												
WR	0	0	0	0	1	A2	A1	A0	DACDATA[15:8]	DACDATA[7:0]	Write to specified channel. WRITE BLOCK or WRITE TRHOUGH setting controls destination register (PREREG or DACREG).	
WRUP	0	0	0	1	0	A2	A1	A0	DACDATA[15:8]	DACDATA[7:0]	Update specified channel's DACREG and PREREG regardless of WRITE BLOCK or WRITE THROUGH setting.	
WRAL	0	0	1	0	0	0	0	0	DACDATA[15:8]	DACDATA[7:0]	Update all channel's DACREG and PREREG regardless of WRITE BLOCK or WRITE THROUGH setting.	
Register Reading												
<Reserved>	1	0	0	0	0	x	x	x			<Reserved>	
RDDO	1	0	0	0	1	A2	A1	A0	DACDATA[15:8]	DACDATA[7:0]	Read PREREG register.	

MNEMONIC	Command Byte[7:0]								DATA[15:8]	DATA [7:0]	Description	DEFAULT
RDCO	1	0	0	1	0	A2	A1	A0	0000 0000	0000 0,swb,sel_10k, sel_hiz	Read CONFIG register.	0004h
RDIN	1	0	0	1	1	A2	A1	A0	DACDATA[15:8]	DACDATA[7:0]	Read DACREG register.	

APPLICATIONS INFORMATION

SAMPLE INSTRUCTION SEQUENCE

The following table shows an example instruction sequence to illustrate the usage of different modes of operation of the DAC. This sequence is for a one channel DAC.

Step	Instruction	8-bit Command	16 bit Payload	Comments
1	CLR	0000 0001	0000 0000 0000 0000	Clear device - return to Power-Up Default State
2	WR	0000 1000	0100 0000 0000 0000	Write 1/4 FS into channel 0. Since device by default is in WRITE-BLOCK mode the data will be written into PREREG, and DAC output will not update
3	LDAC	0001 1000	xxxx xxxx 0000 0001	Issue LDAC command to channel 0. Data is transferred from PREREG into DACREG and DAC output updates to 1/4 FS
4	SWB	0010 1000	xxxx xxxx 1111 1110	Set channels 1 to 7 to WRITE-BLOCK mode, and channel 0 to WRITE-THROUGH mode
5	WR	0000 1000	1111 1111 1111 1111	DAC output updates immediately to FS since the channel is set to write through mode.
6	PD	0011 0000	0000 0001 0000 0000	Power down the device, and set the channel 0 DAC output to the HIZ state

USING REFERENCES AS POWER SUPPLIES

Although the DAC has a separate reference and analog power pin, it is still possible to use a reference to drive both. This arrangement will avoid a separate voltage regulator for V_A and will provide a more stable voltage source. The LM4140 has an initial accuracy of 0.1%, is capable of driving 8mA and comes in a 4.096V version. Bypassing both the input and the output will improve noise performance.

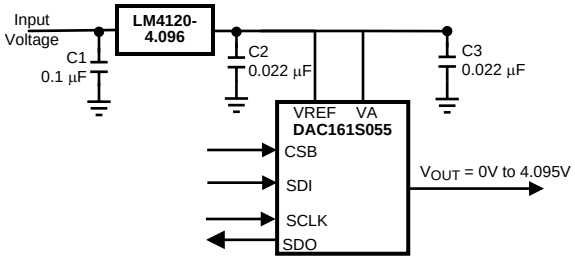


Figure 23. Using the LM4120 as a power supply

A LOW NOISE EXAMPLE

A LM4050 powered off of a battery is a good choice for very low noise prototype circuits. The minimum value for R must be chosen so that the LM4050 does not draw more than its 15mA rating. Note the largest current through the LM4050 will occur when the DAC is shutdown. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum V_{REF} current.

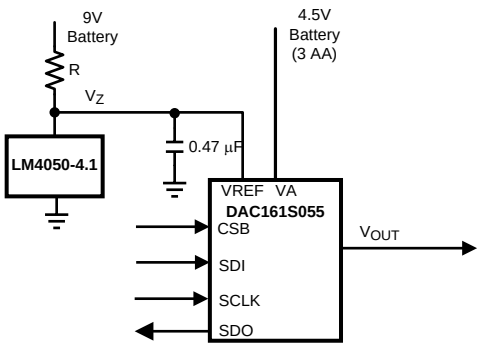


Figure 24. Using the LM4050 in a low noise circuit

LAYOUT, GROUNDING AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC should have separate analog and digital areas. These areas are defined by the locations of the analog and digital power planes. Both power planes should be in the same board layer. There should be a single ground plane. Frequently a single ground plane design will utilize a fencing technique to prevent the mixing of analog and digital ground currents. Separate ground planes should only be used if the fencing technique proves inadequate. The separate ground planes must be connected in a single place, preferably near the DAC. Special care is required to specify that digital signals with fast edge rates do not pass over split ground planes. The fast digital signals must always have a continuous return path below their traces.

When possible, the DAC power supply should be bypassed with a 10µF and a 0.1µF capacitor placed as close as possible to the device with the 0.1µF closest to the supply pin. The 10µF capacitor should be a tantalum type and the 0.1µF capacitor should be a low ESL, low ESR type. Sometime, the loading requirements of the regulator driving the DAC do not allow such capacitance to be placed on the regulator output. In those cases, bypass should be as large as allowed by the regulator using a low ESL, low ESR capacitance. In the LM4120 example above, the supply is bypassed with 0.022µF ceramic capacitors. The DAC should be fed with power that is only used for analog circuits.

Avoid crossing analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC161S055CISQ/NOPB	ACTIVE	WQFN	RGH	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	161S055	Samples
DAC161S055CISQE/NOPB	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	161S055	Samples
DAC161S055CISQX/NOPB	ACTIVE	WQFN	RGH	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	161S055	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

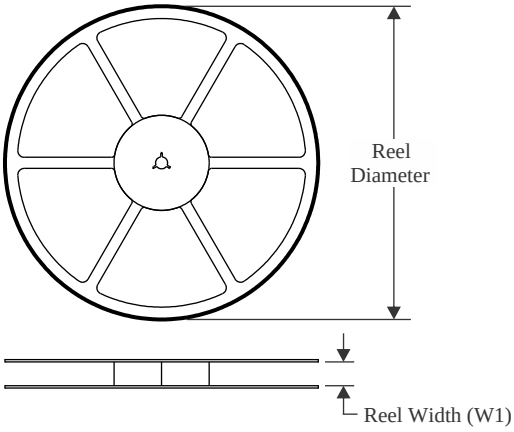
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

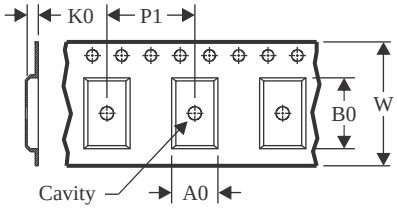
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

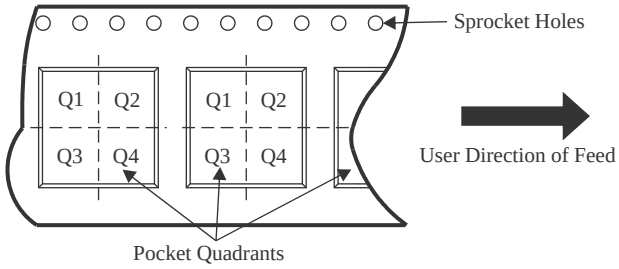


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

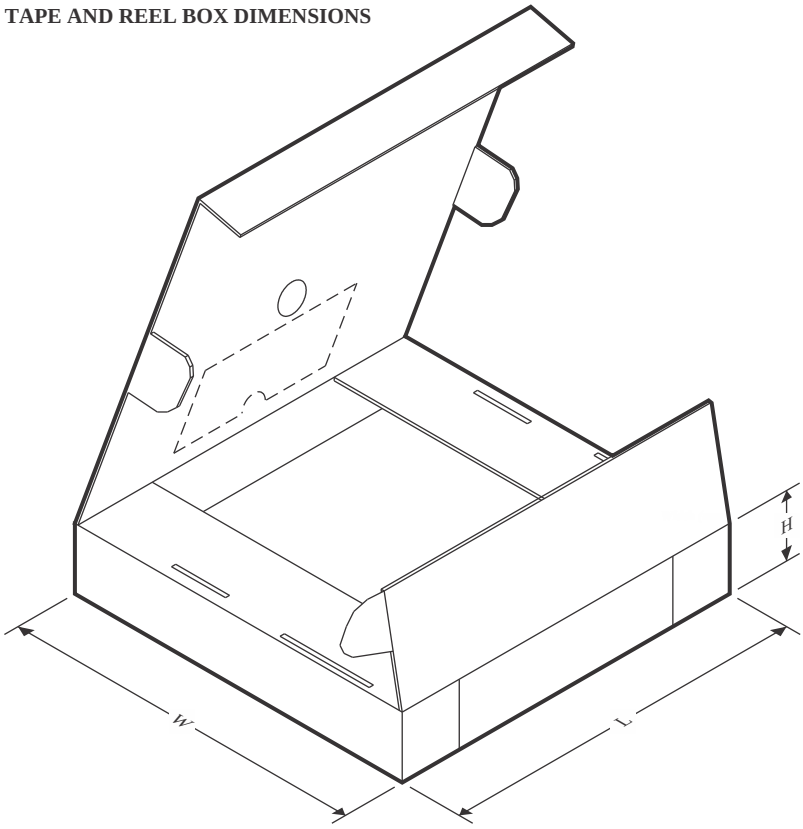
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC161S055CISQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC161S055CISQE/ NOPB	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC161S055CISQX/ NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

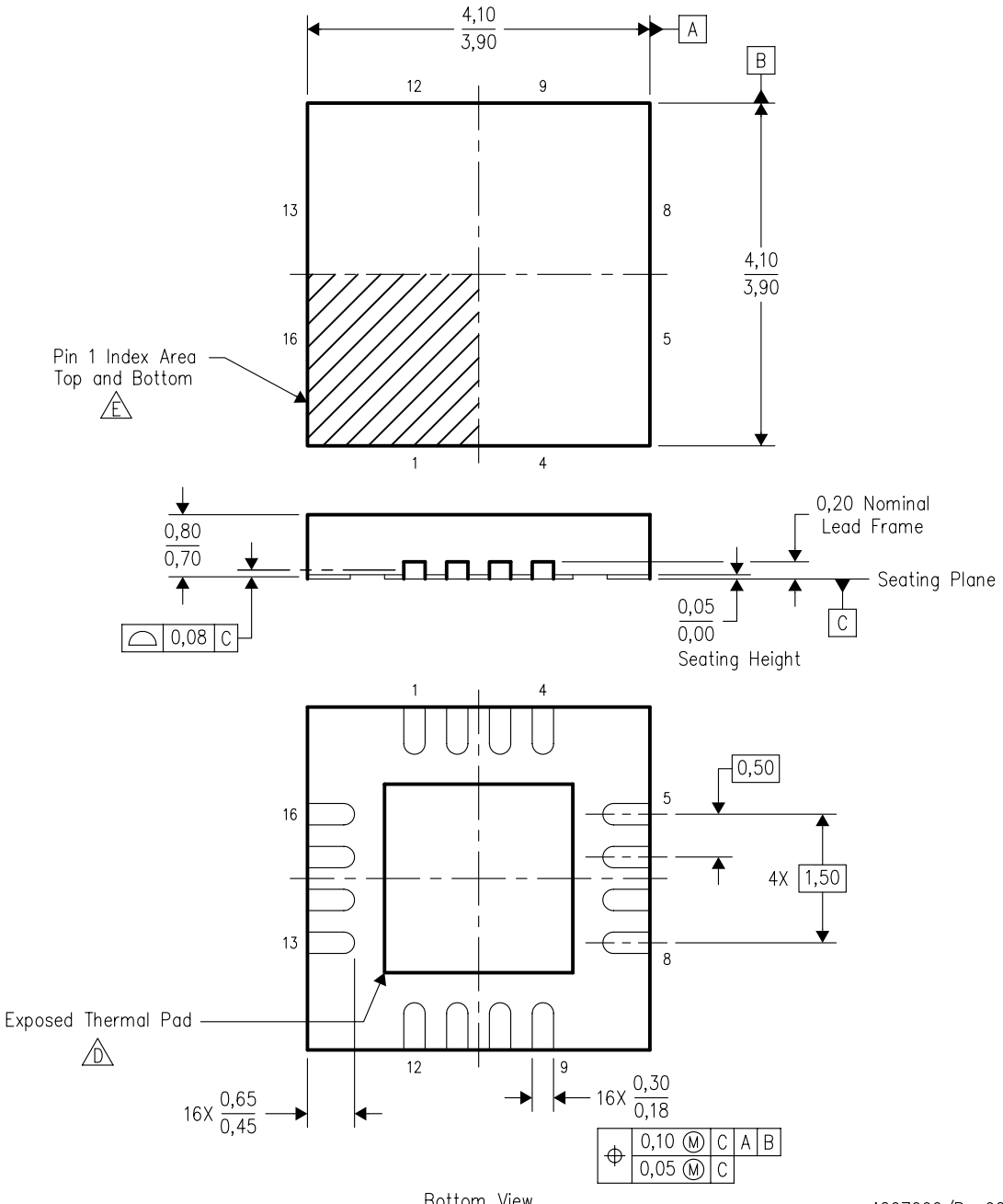
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC161S055CISQ/NOPB	WQFN	RGH	16	1000	367.0	367.0	35.0
DAC161S055CISQE/ NOPB	WQFN	RGH	16	250	367.0	367.0	35.0
DAC161S055CISQX/ NOPB	WQFN	RGH	16	4500	356.0	356.0	35.0

RGH (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Complies to JEDEC MO–220 variation WGGD–4.

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