STS2DNF30L

Dual n-channel 30 V, 0.09 Ω, 3 A SO-8 STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS2DNF30L	30V	<0.11Ω	3A

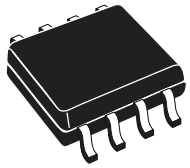
- Standard outline for easy automated surface mount assembly
- Low threshold gate drive

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.



S0-8

Figure 1. Internal schematic diagram

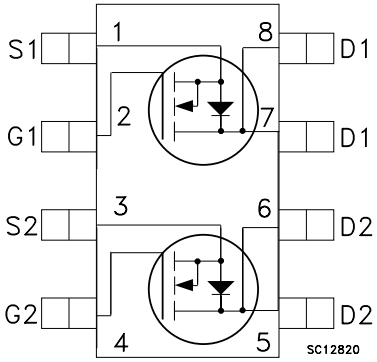


Table 1. Device summary

Order code	Marking	Package	Packaging
STS2DNF30L	2DF30L	SO-8	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	30	V
V_{GS}	Gate- source voltage	±18	V
I_D	Drain current (continuous) at T_C = 25°C	3	A
I_D	Drain current (continuous) at T_C = 100°C	1.9	A
I_{DM} (1)	Drain current (pulsed)	9	A
P_{TOT}	Total dissipation at T_C = 25°C dual operation Total dissipation at T_C = 25°C single operation	1.6 2	W W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max single operation	62.5	°C/W
	Thermal resistance junction-ambient max dual operation	78	
T_J	Maximum operating junction ambient	150	°C
T_{stg}	Storage temperature	-55 to 175	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating, T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±18V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 1A V_{GS} = 5V, I_D = 1A		0.09 0.13	0.11 0.15	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}>$I_{D(on)}$x$R_{DS(on)max}$ I_D=2.5A	-	2.5	-	S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	-	121	-	pF
C_{oss}	Output capacitance			45		pF
C_{rss}	Reverse transfer capacitance			11		pF
Q_g	Total gate charge	V_{DD} = 24V, I_D = 2A, V_{GS} = 10V	-	4.5	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	0.9	-	nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D=1A, R_G=4.7Ω, V_{GS}= 4.5V (see Figure 13)	-	19	-	ns
t_r	Rise time			20		ns
$t_{d(off)}$	Turn-off delay time	V_{DD}=15 V, I_D=1A, R_G=4.7Ω, V_{GS}= 4.5V (see Figure 13)	-	12	-	ns
t_f	Fall time			8		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		3	A
I_{SDM} (1)	Source-drain current (pulsed)		-		12	A
V_{SD} (2)	Forward on voltage	I_{SD} = 2A, V_{GS} = 0	-		1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2A, V_{DD} = 30V di/dt = 100A/µs, T_j = 150°C (see Figure 15)	-	19 8.1 0.85		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

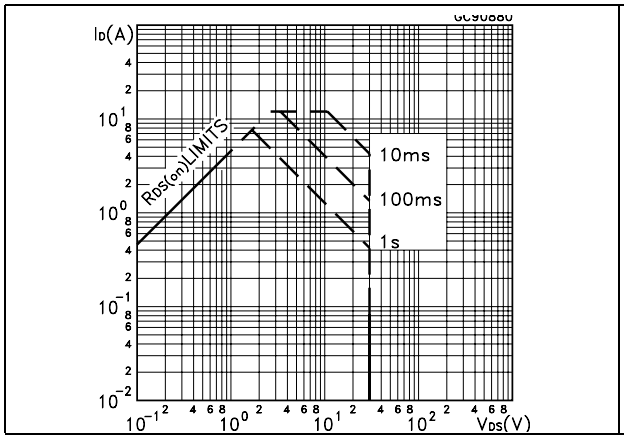


Figure 3. Thermal impedance

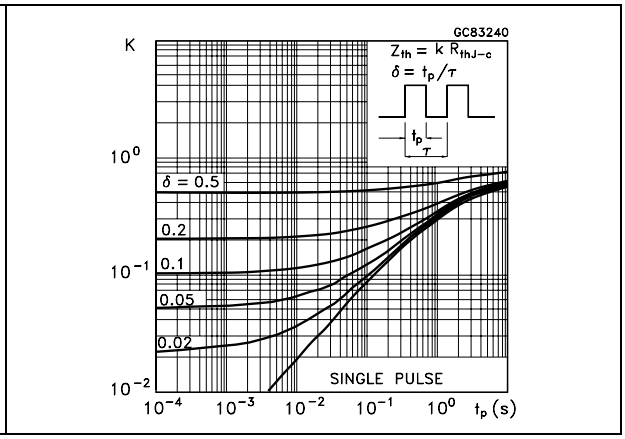


Figure 4. Output characteristics

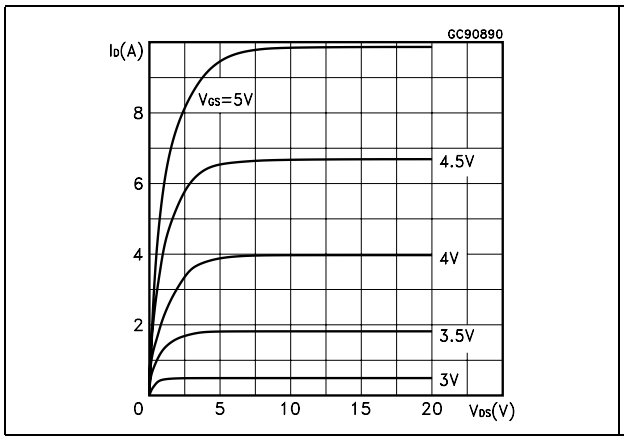


Figure 5. Transfer characteristics

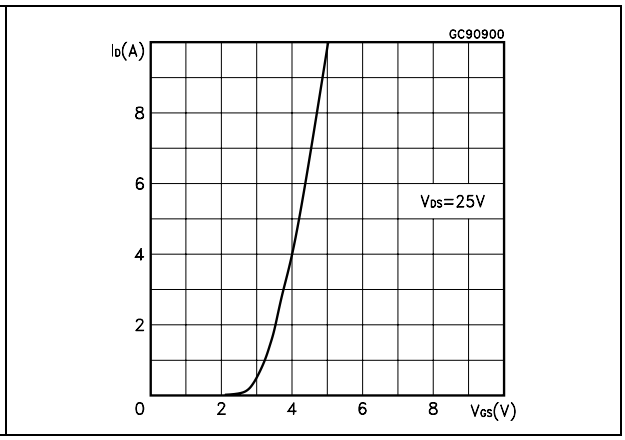


Figure 6. Transconductance

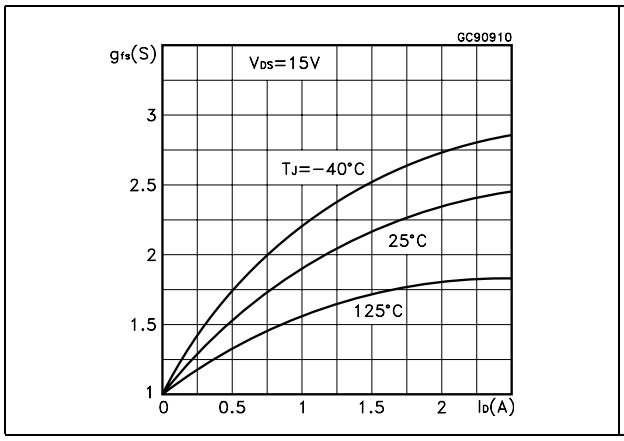


Figure 7. Static drain-source on resistance

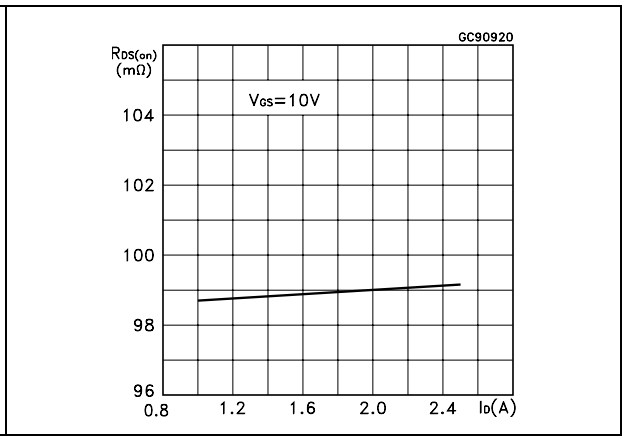


Figure 8. Gate charge vs. gate-source voltage

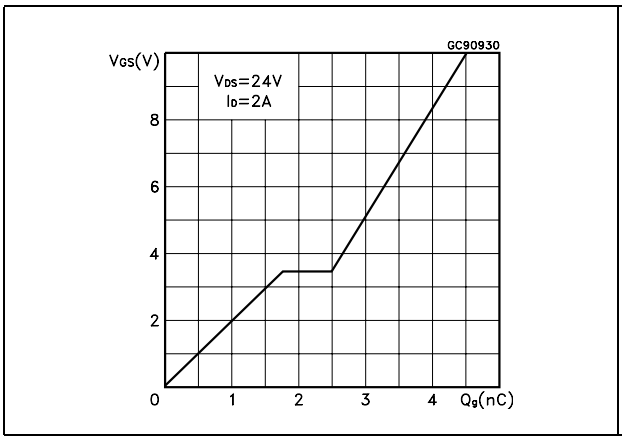


Figure 9. Capacitance variations

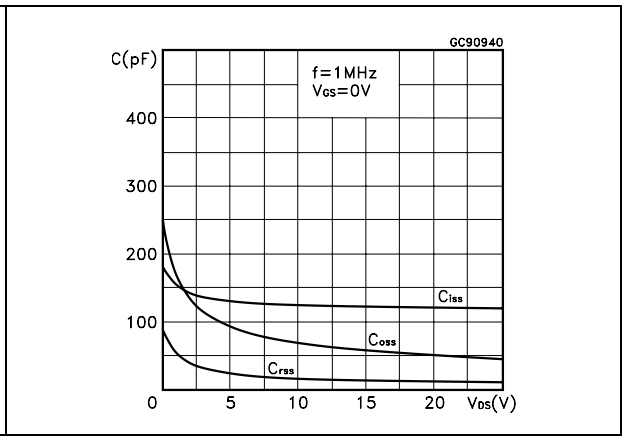


Figure 10. Normalized gate threshold voltage vs. temperature

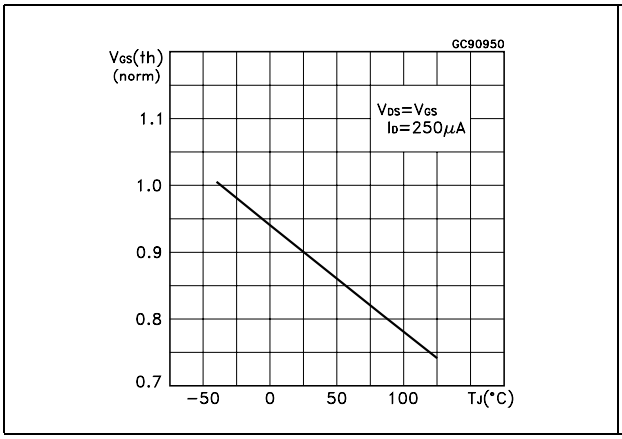


Figure 11. Normalized on resistance vs. temperature

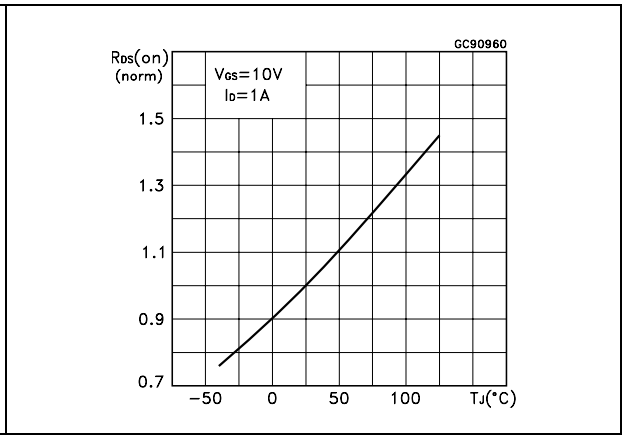
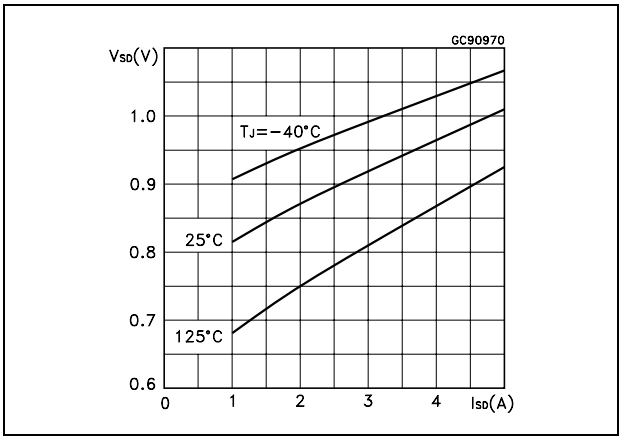


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

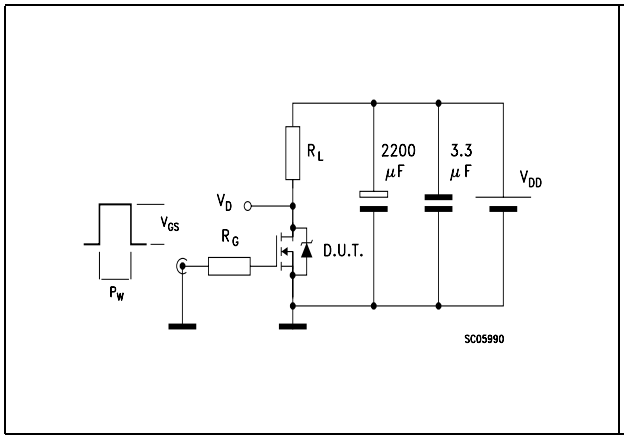


Figure 14. Gate charge test circuit

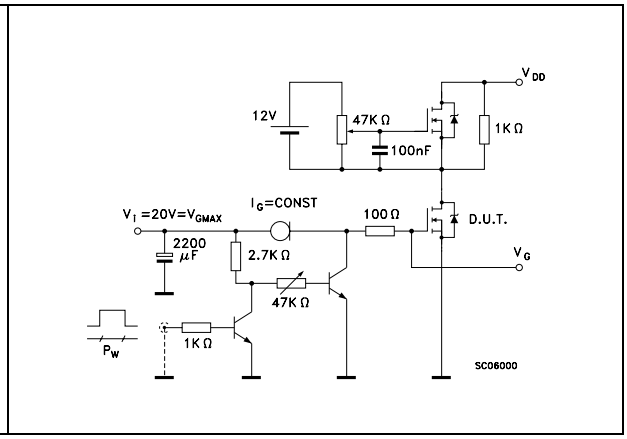


Figure 15. Test circuit for inductive load switching and diode recovery times

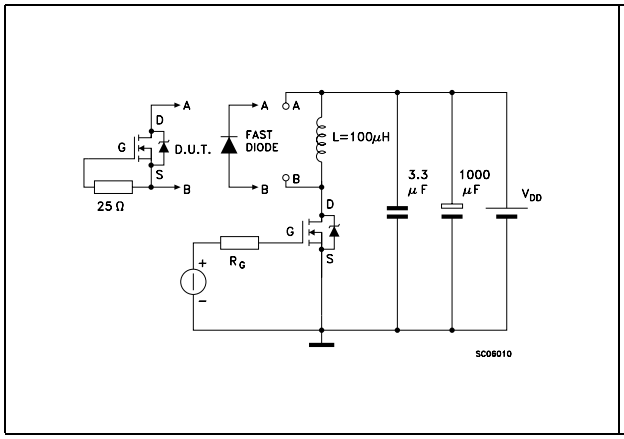


Figure 16. Unclamped inductive load test circuit

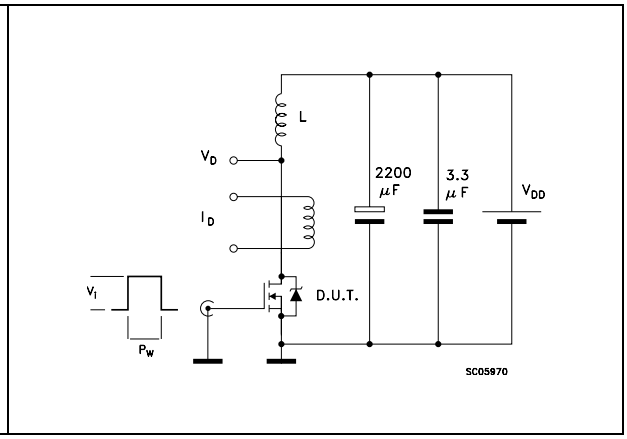


Figure 17. Unclamped inductive waveform

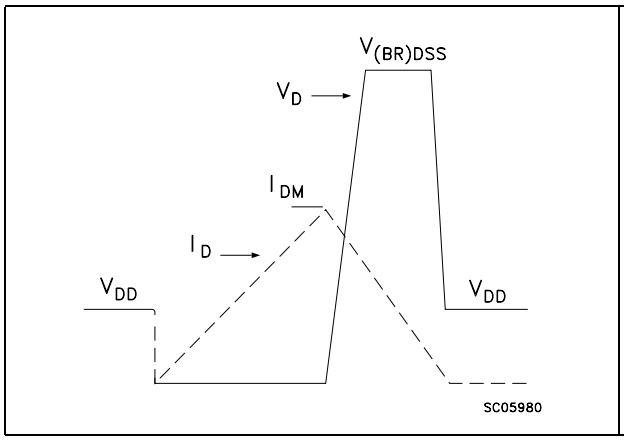
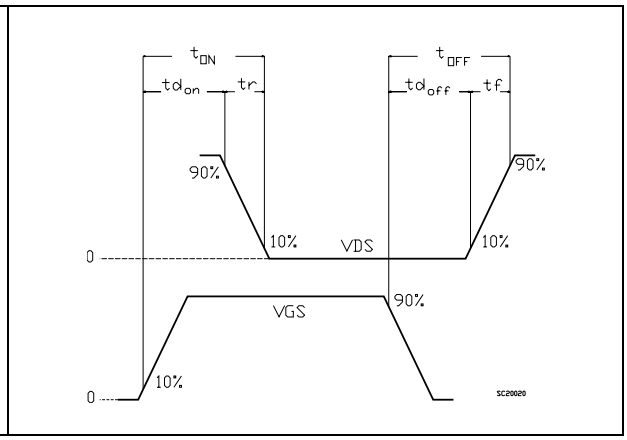


Figure 18. Switching time waveform

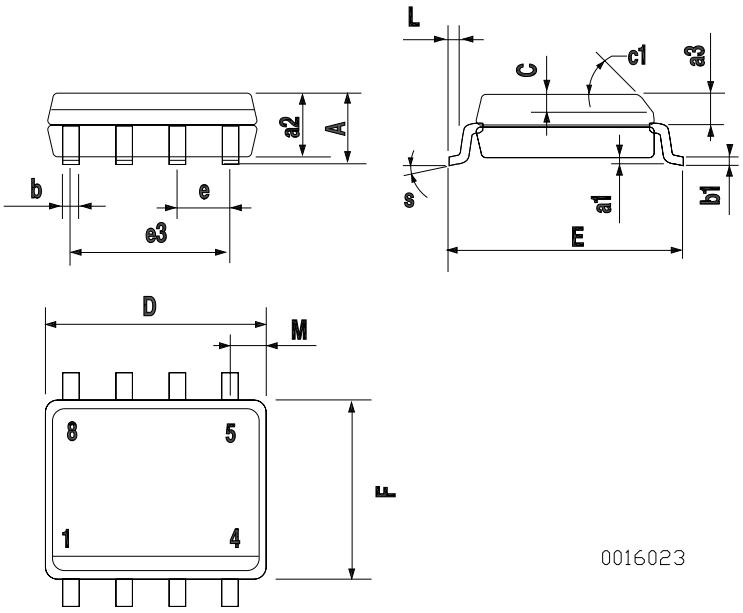


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jun-2004	3	Complete document.
10-Nov-2006	4	The document has been reformatted.
31-Jan-2007	5	Typo mistake on *Table 2*.
03-May-2007	6	$R_{DS(on)}$ Max value has been changed.
03-Nov-2009	7	Updated marking in *Table 1*.

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