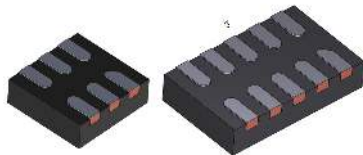
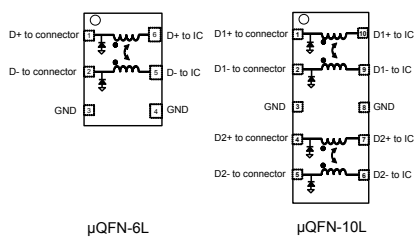


## Common mode filter with ESD protection for high speed serial interface



μQFN-6L (Bottom view) 1.35 mm x 1.4 mm x 0.5mm  
 μQFN-10L (Bottom view) 1.35 mm x 2.2 mm x 0.5mm

### Functional schematic



### Features

- 10.7 GHz differential bandwidth to comply with HDMI 2.1, HDMI 2.0, HDMI 1.4, USB4, USB 3.2 Gen2, USB 2.0, MIPI, Display port 2.0, etc.
- High common mode attenuation on WLAN frequencies:
  - -15 dB at 2.4 GHz
  - -21 dB at 5.0 GHz
  - -17 dB at 6.0 GHz
- Low serial resistance: 3.0 Ω
- Very low PCB space consumption
- Thin package: 0.5 mm max.
- High reduction of parasitic elements through integration
- Lead free and RoHS package
- Exceeds IEC 61000-4-2 level 4 standard:
  - Contact discharge:
    - ±9 kV (contact discharge, ECMF2-40A100N6)
    - ±10 kV (contact discharge, ECMF4-40A100N10)
  - Air discharge:
    - ±20 kV (air discharge, ECMF2-40A100N6)
    - ±25 kV (air discharge, ECMF4-40A100N10)

Product status	
Part number	Package
ECMF2-40A100N6	μQFN-6L
ECMF4-40A100N10	μQFN-10L

### Applications

- Notebook, laptop
- Streaming box, HDMI stick
- Game console, Set top box
- Tablet
- Portable devices

### Description

The ECMF2-40A100N6 and ECMF4-40A100N10 are highly integrated common mode filters designed to suppress EMI/RFI common mode noise on high speed differential serial buses like HDMI 2.1, HDMI 2.0, HDMI1.4, USB4, USB 3.2 Gen 2, USB 2.0, ethernet, MIPI, Display Port and other high speed serial interfaces.

They have a very large differential bandwidth to comply with these standards and can also protect and filter one or two differential lanes.

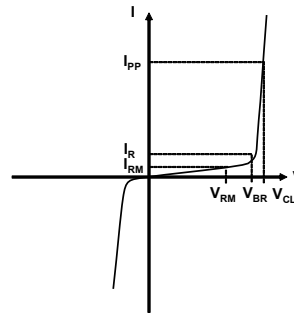
# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ °C}$ )**

Symbol	Parameter	Value	Unit	
$V_{PP}$	Peak pulse voltage	IEC 61000-4-2 contact discharge:		
		ECMF2-40A100N6	$\pm 9$	kV
		ECMF4-40A100N10	$\pm 10$	
		IEC 61000-4-2 air discharge:		
	ECMF2-40A100N6	$\pm 20$	kV	
	ECMF4-40A100N10	$\pm 25$		
$I_{RMS}$	Maximum RMS current	100	mA	
$T_{op}$	Maximum operating temperature range	-55 to +125	°C	
$T_{stg}$	Storage temperature range	-55 to +150		
$T_L$	Maximum temperature for soldering during 10 s	260		

**Figure 1. Electrical characteristics (definitions)**

- $V_{RM}$  Maximum stand-off voltage
- $V_{CL}$  Clamping voltage at peak pulse current  $I_{PP}$
- $I_{RM}$  Leakage current at  $V_{RM}$
- $I_{PP}$  Peak pulse current
- $V_{BR}$  Breakdown voltage
- $C_{DIODE}$  ESD diode capacitance
- $R_{DC}$  DC serial resistance
- $f_c$  Differential cut off frequency


**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ °C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	Breakdown voltage	$I_R = 1\text{ mA}$	5.3	5.8		V
$I_{RM}$	Leakage current	$V_{RM} = 3.6\text{ V per line}$		< 1	50	nA
		$V_{RM} = 5\text{ V per line}$		3	70	
$V_{RM}$	Reverse working voltage				5	V
$R_{DC}$	DC serial resistance, $I_{DC} = 20\text{ mA}$			3.0		$\Omega$
$f_c$	Differential mode cut-off frequency <sup>(1)</sup>			10.7		GHz
$V_{CL}$	Reverse clamping voltage	TLP measurement (pulse duration 100 ns), 16 A $I_{PP}$		20.5		V
		8 kV contact discharge after 30 ns, IEC 61000-4-2		18		
$C_{DIODE}$	Capacitance	$V_{BIAS} = 0\text{ V}$ , $F = 2.5\text{ GHz to }9\text{ GHz}$ , $V_{OSC} = 30\text{ mV}$		0.25	0.40	pF
$R_D$	Dynamic resistance, TLP measurement (pulse duration 100 ns)			0.8		$\Omega$

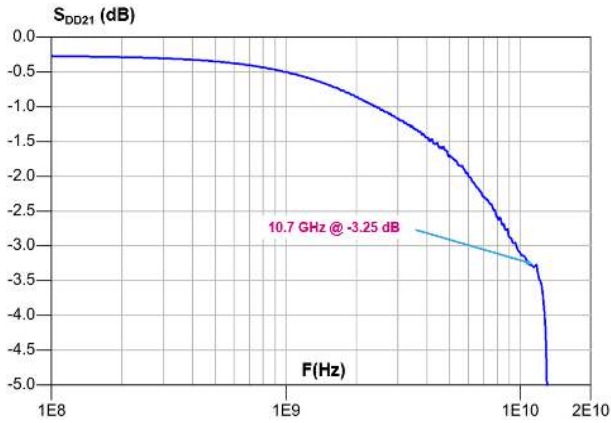
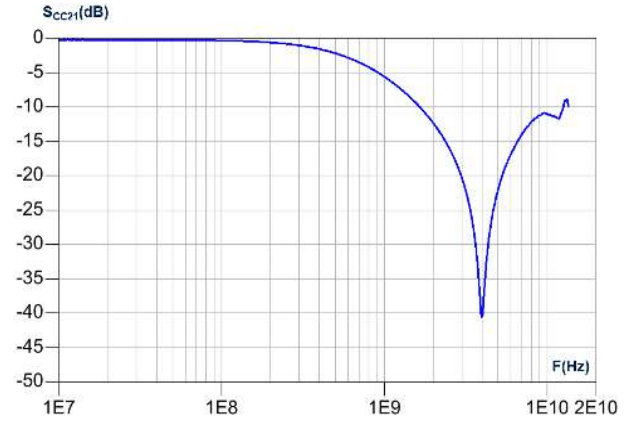
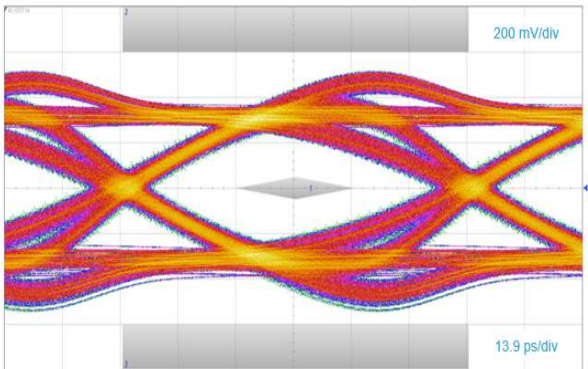
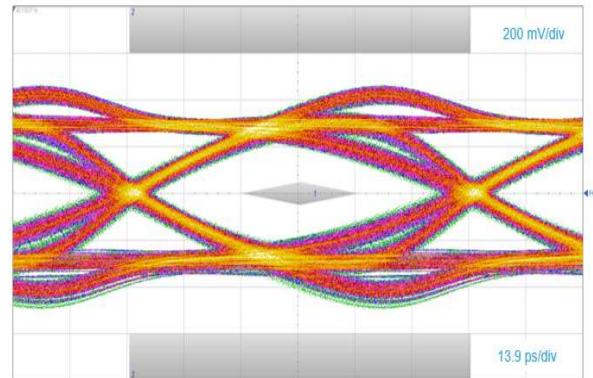
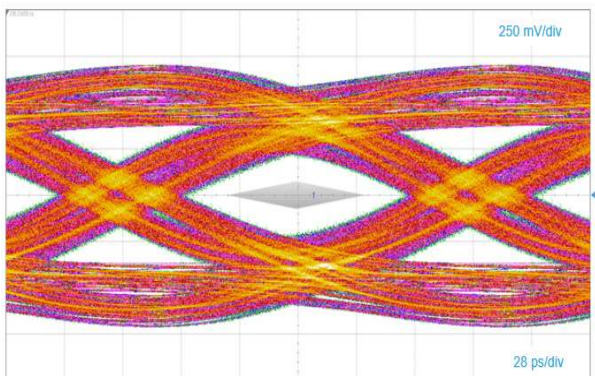
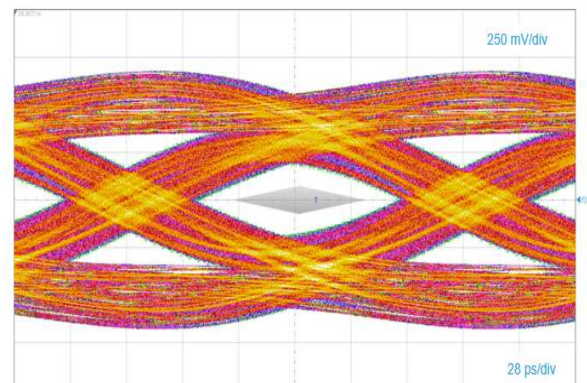
1. Attenuation at 10 MHz as reference.

**Table 3. ECMF2-40A100N6 pin discription**

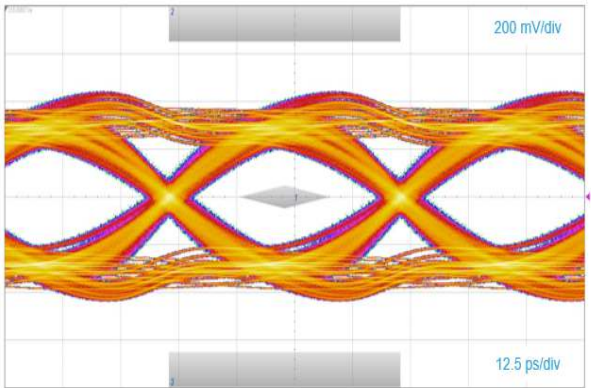
Pin number	Description	Pin number	Description
1	D+ to connector	4	GND
2	D- to connector	5	D- to IC
3	GND	6	D+ to IC

**Table 4. ECMF4-40A100N10 pin description**

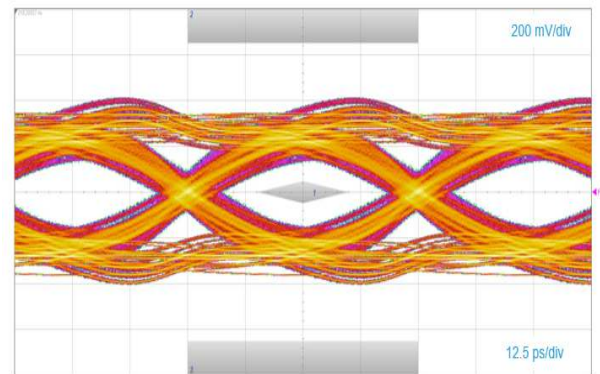
Pin number	Description	Pin number	Description
1	D1+ to connector	6	D2- to IC
2	D1- to connector	7	D2+ to IC
3	GND	8	GND
4	D2+ to connector	9	D1- to IC
5	D2- to connector	10	D1+ to IC

**1.1 Characteristics (curves)**
**Figure 2. Differential attenuation versus frequency**  
 $(Z_0 \text{ DIFF} = 100 \Omega)$ 

**Figure 3. Common mode attenuation versus frequency**  
 $(Z_0 \text{ COM} = 50 \Omega)$ 

**Figure 4. HDMI2.1 12 Gbps eye diagram without**  
 ECMFx-40A100Nx (with worst cable model (WCM3),  
 EQ with 8 dB CTLE and One-tap DFE)

**Figure 5. HDMI2.1 12 Gbps eye diagram with**  
 ECMFx-40A100Nx (with worst cable model (WCM3),  
 EQ with 8 dB CTLE and One-tap DFE)

**Figure 6. HDMI2.0 5.94 Gbps eye diagram without**  
 ECMFx-40A100Nx (with worst cable model and equalizer)

**Figure 7. HDMI2.0 5.94 Gbps eye diagram with**  
 ECMFx-40A100Nx (with worst cable model and equalizer)


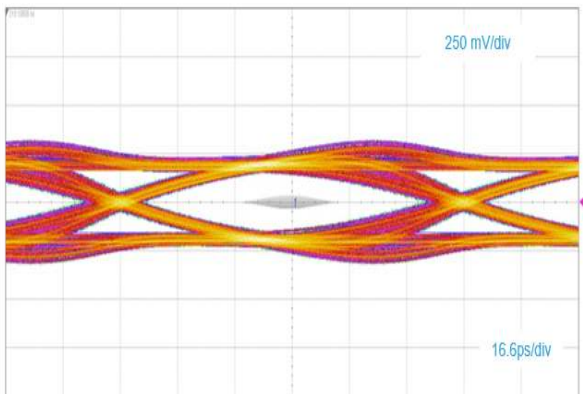
**Figure 8.** USB4 20.0 Gbps eye diagram without ECMFx-40A100Nx (with Preset 0, reference cable 0.8m, equalizer with ADC = 0dB and DFE)



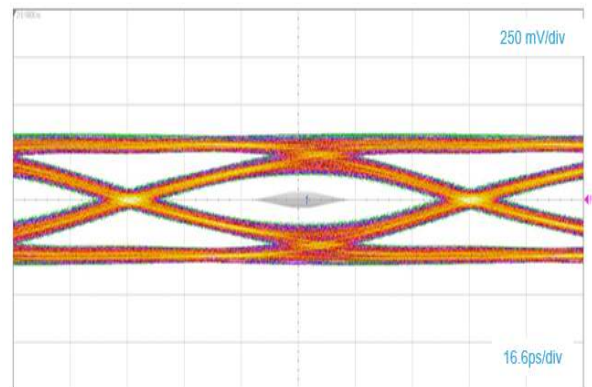
**Figure 9.** USB4 20.0 Gbps eye diagram with ECMFx-40A100Nx (with Preset 0, reference cable 0.8m, equalizer with ADC = 0dB and DFE)



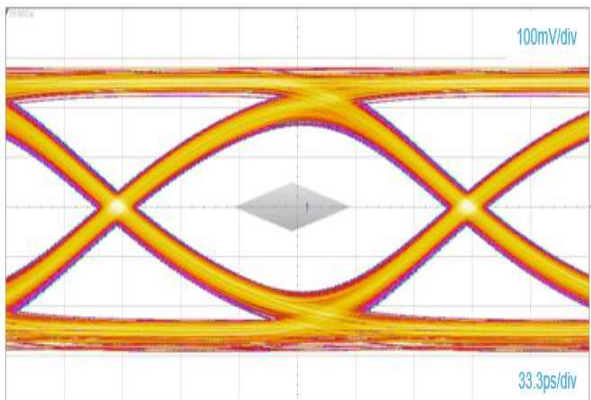
**Figure 10.** USB3.2 Gen 2 10.0 Gbps eye diagram without ECMFx-40A100Nx (with type C connector, reference cable, equalizer with ADC = 5 dB and DFE)



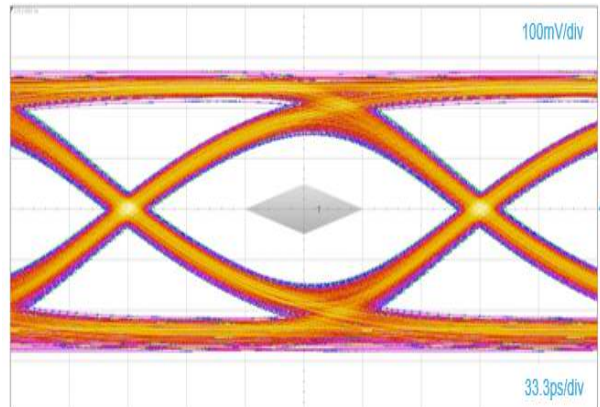
**Figure 11.** USB3.2 Gen 2 10.0 Gbps eye diagram with ECMFx-40A100Nx (with type C connector, reference cable, equalizer with ADC = 5 dB and DFE)



**Figure 12.** USB3.2 Gen 1 5.0 Gbps eye diagram without ECMFx-40A100Nx (with type C connector, reference cable and equalizer)

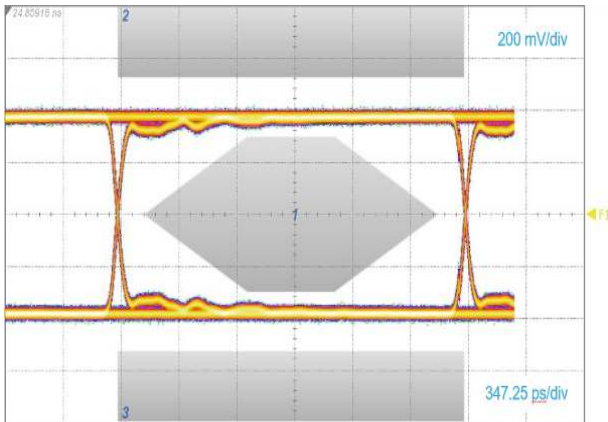


**Figure 13.** USB3.2 Gen 1 5.0 Gbps eye diagram with ECMFx-40A100Nx (with type C connector, reference cable and equalizer)

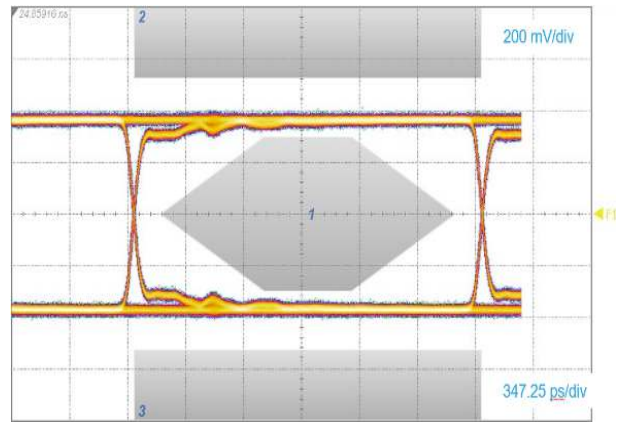




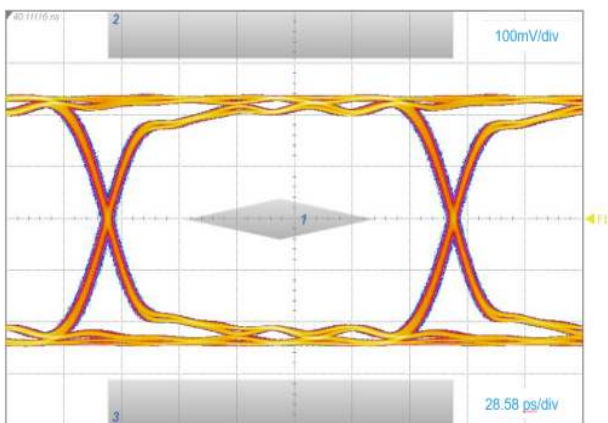
**Figure 14.** USB 2.0 High Speed 480 Mbps eye diagram, Template 1, without ECMFx-40A100Nx



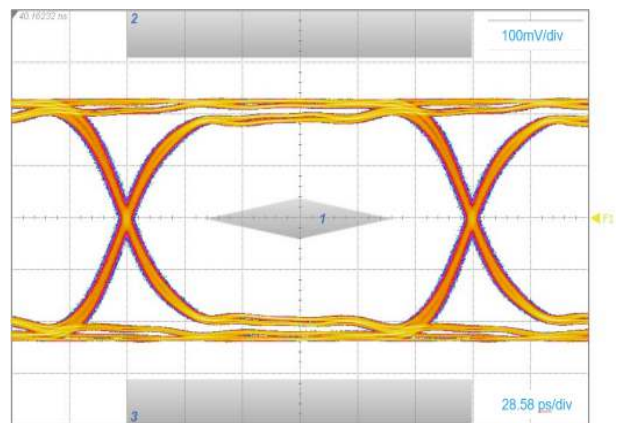
**Figure 15.** USB 2.0 High Speed 480 Mbps eye diagram, Template 1, with ECMFx-40A100Nx



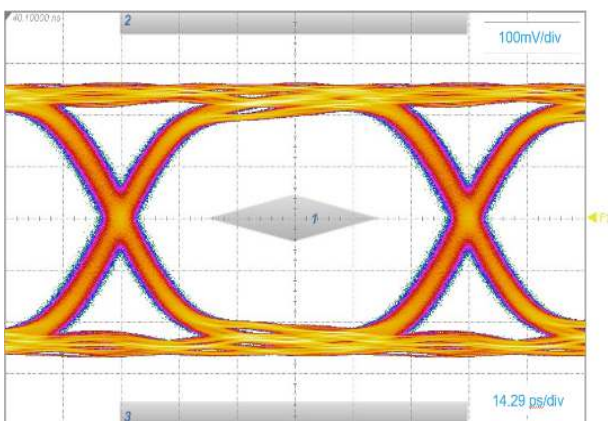
**Figure 16.** MIPI M-PHY – Gear 3 at 5.83 Gbps eye diagram without ECMFx-40A100Nx



**Figure 17.** MIPI M-PHY – Gear 3 at 5.83 Gbps eye diagram with ECMFx-40A100Nx



**Figure 18.** MIPI M-PHY – Gear 4 at 11.66 Gbps eye diagram without ECMFx-40A100Nx



**Figure 19.** MIPI M-PHY – Gear 4 at 11.66 Gbps eye diagram with ECMFx-40A100Nx

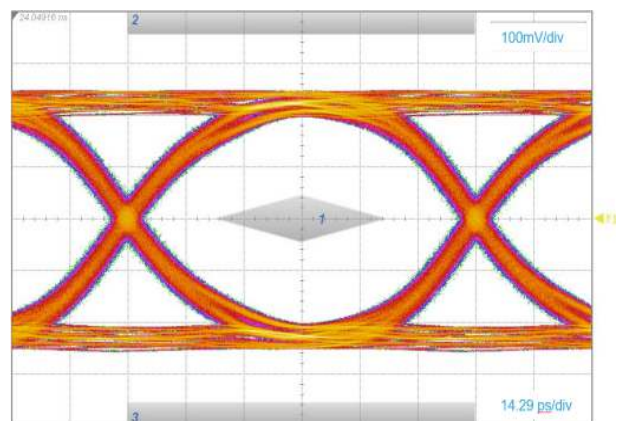


Figure 20. ESD response to IEC61000-4-2 (+8 kV contact discharge)

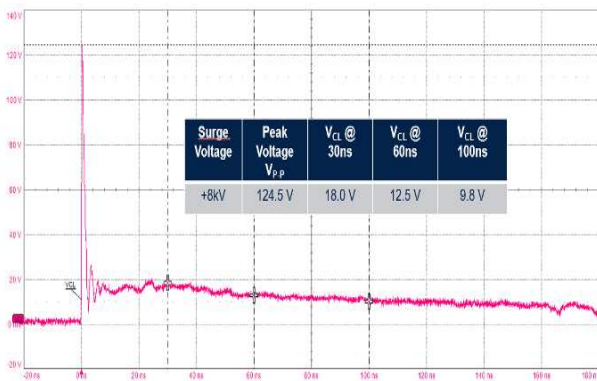


Figure 21. ESD response to IEC61000-4-2 (-8 kV contact discharge)

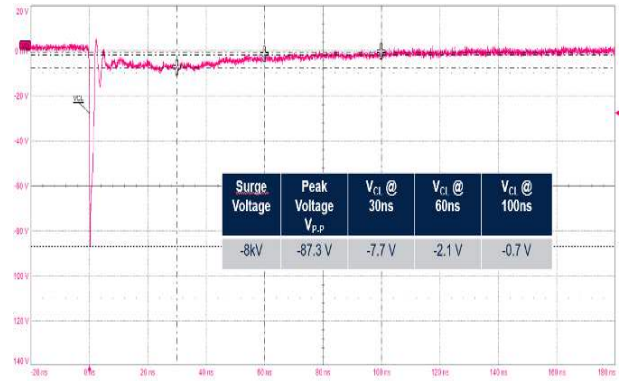
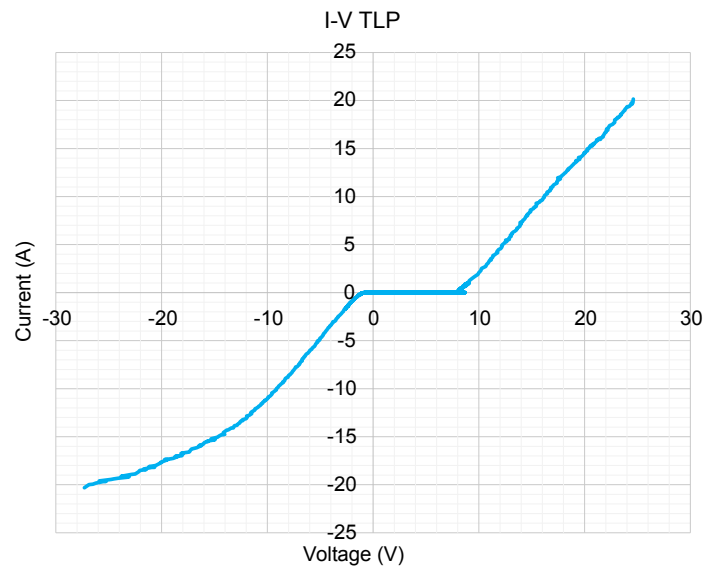


Figure 22. TLP characteristic

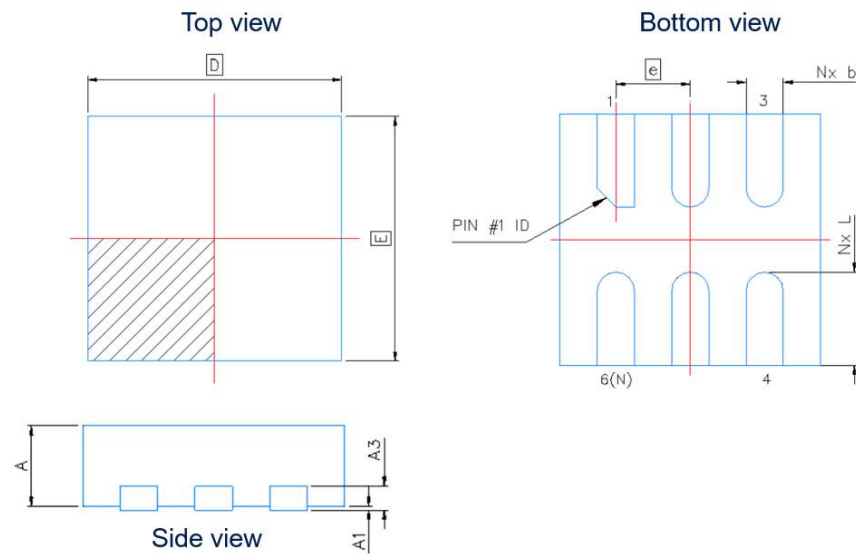


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 2.1 $\mu$ QFN6L package information

**Figure 23.**  $\mu$ QFN6L package outline



**Table 5.**  $\mu$ QFN6L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.41	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.35	1.40	1.45
E	1.30	1.35	1.40
e		0.40	
L	0.40	0.50	0.60
N		6	



## 2.2 μQFN10L package information

Figure 24. μQFN10L package outline

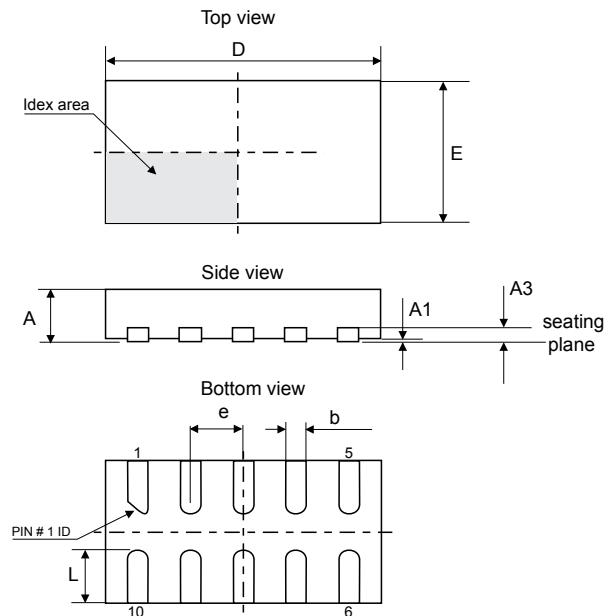
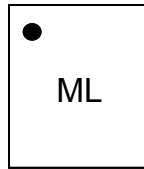
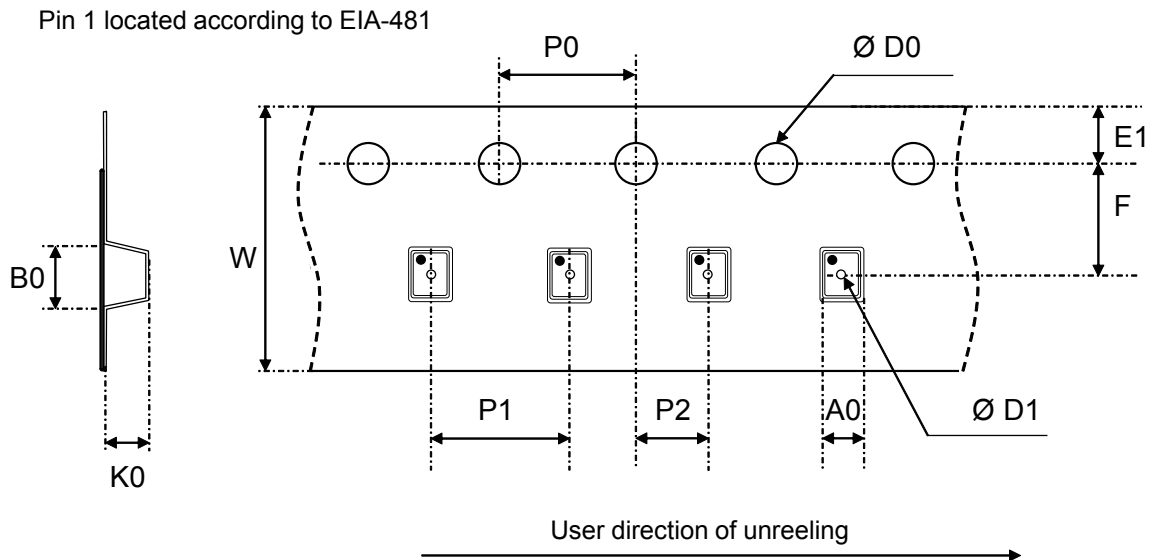


Table 6. μQFN10L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.41	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	2.15	2.20	2.25
E	1.30	1.35	1.40
e		0.40	
L	0.40	0.50	0.60

**2.3 Packing information**
**Figure 25. ECMF2-40A100N6 marking**

**Figure 26. ECMF4-40A100N10 marking**


**Note:** The marking codes can be rotated by 90 ° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

**Figure 27. Tape and reel outline**


**Note:** Pocket dimensions are not on scale  
 Pocket shape may vary depending on package

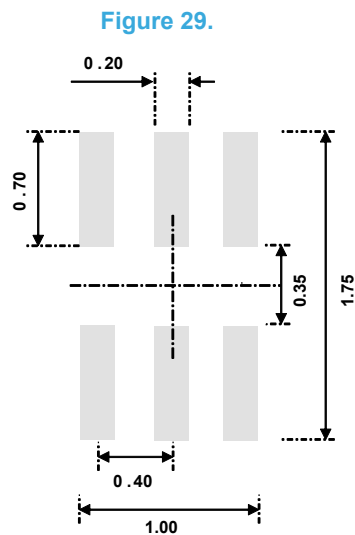
**Table 7. Tape and reel mechanical data**

Ref.	Dimensions (millimeters)		
	Min.	Typ.	Max.
P1	3.90	4.00	4.10
P0	3.90	4.00	4.10
Ø D0	1.40	1.50	1.60
Ø D1 (ECMF2-40A100N6)	0.45	0.50	0.55
Ø D1 (ECMF4-40A100N10)	0.8		
F	3.45	3.50	3.55
E1	1.65	1.75	1.85
K0 (ECMF2-40A100N6)	0.70	0.75	0.80
K0 (ECMF4-40A100N10)	0.60	0.65	0.70
P2	1.95	2.00	2.05
W	7.90	8.00	8.10
A0 (ECMF2-40A100N6)	1.43	1.48	1.53
A0 (ECMF4-40A100N10)	1.50	1.55	1.60
B0 (ECMF2-40A100N6)	1.75	1.80	1.85
B0 (ECMF4-40A100N10)	2.35	2.40	2.45

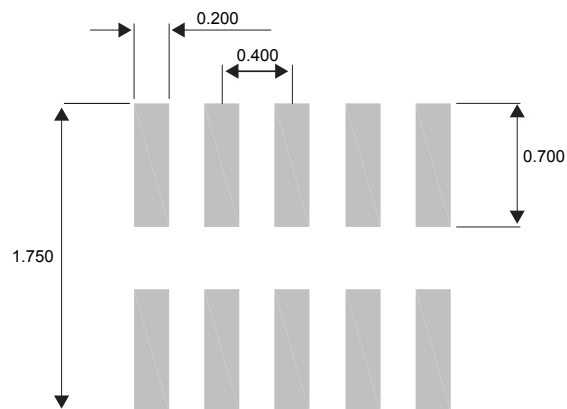
### 3 Recommendation on PCB assembly

#### 3.1 Footprint

Figure 28. ECMF2-40A100N6 footprint in mm



ECMF4-40A100N10 footprint in mm



SMD footprint design is recommended.

### 3.2 Stencil opening design

Recommended design reference: stencil opening thickness: 100 µm

Figure 30. ECMF2-40A100N6 stencil opening recommendations

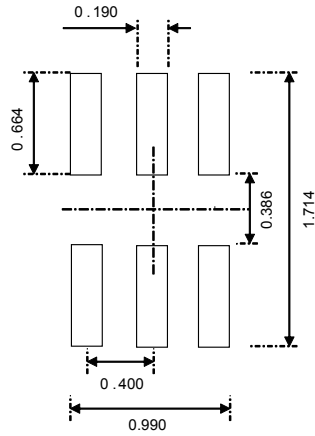
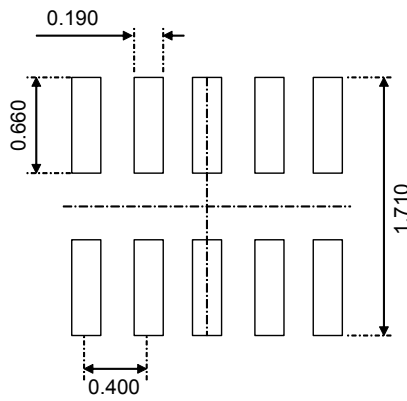


Figure 31. ECMF4-40A100N10 stencil opening recommendations





### 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during PCB movement.
4. Solder paste with fine particles: powder particle size is 20-38  $\mu\text{m}$ .

### 3.4 Placement

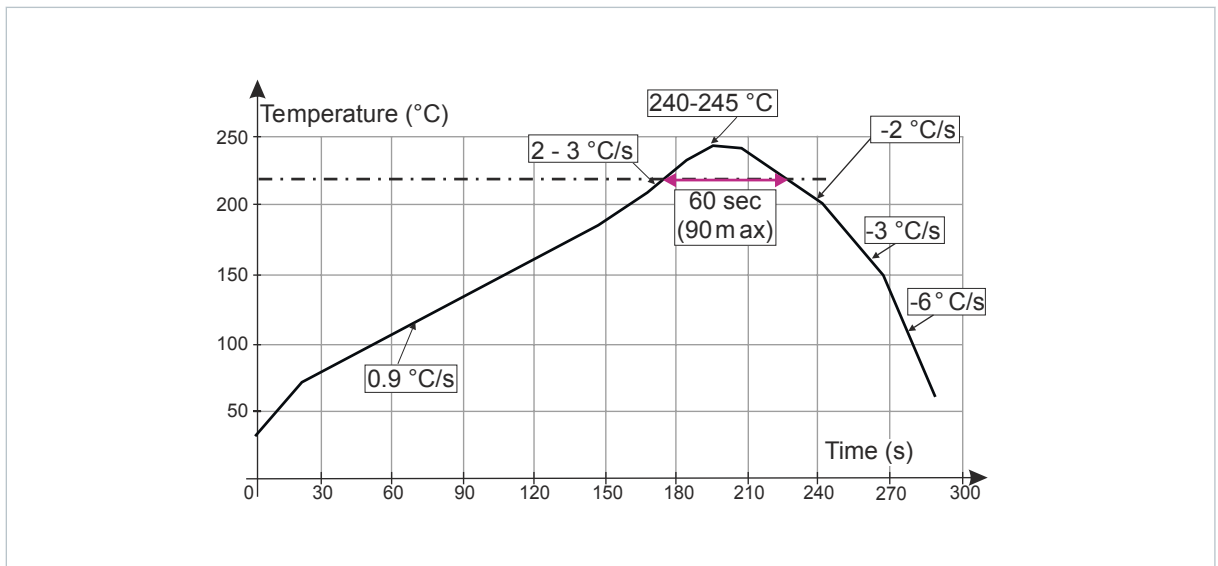
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

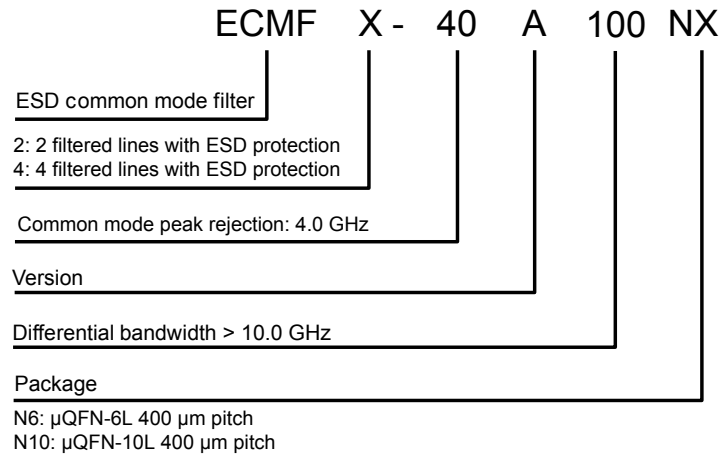
### 3.6 Reflow profile

**Figure 32. ST ECOPACK<sup>®</sup> recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 4 Ordering information

**Figure 33. Ordering information scheme**

**Table 8. Ordering information**

Order code	Marking <sup>(1)</sup>	Package	Weight	Base qty.	Delivery mode
ECMF2-40A100N6	ML	$\mu$ QFN-6L	2.4 mg	3000	Tape and reel
ECMF4-40A100N10	MK	$\mu$ QFN-10L	3.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

## Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Feb-2022	1	Initial release.
19-May-2022	2	Added from Figure 15 to Figure 20.
27-Sep-2022	3	Updated <a href="#">Figure 3</a> .

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved