SDFS008A - D2932, APRIL 1986 - REVISED OCTOBER 1993

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for N-Bits Parity
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

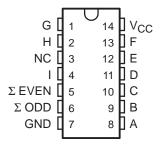
These universal, monolithic, 9-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The SN54F280B is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F280B is characterized for operation from 0°C to 70°C.

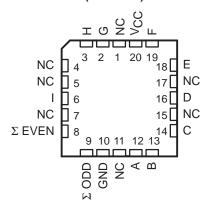
FUNCTION TABLE

NO. OF INPUTS	OUTPUTS					
A THRU I THAT ARE HIGH	Σ EVEN	Σ ODD				
0, 2, 4, 6, 8	Н	L				
1, 3, 5, 7, 9	L	Н				

SN54F280B . . . J PACKAGE SN74F280B . . . D OR N PACKAGE (TOP VIEW)

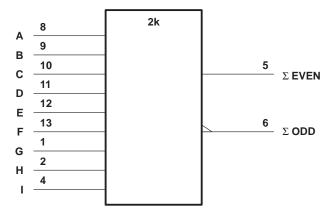


SN54F280B . . . FK PACKAGE (TOP VIEW)



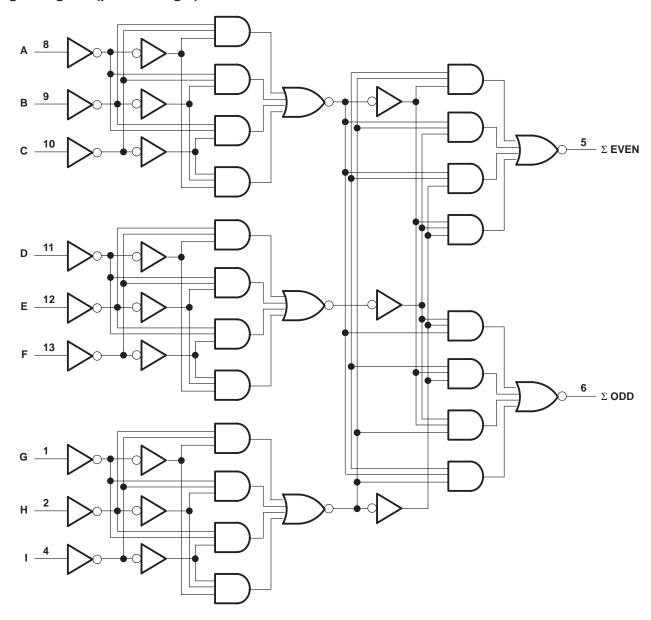
NC - No internal connection

logic symbol†



 \dagger This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	\dots -0.5 V to 7 V
Input voltage range (see Note 1)	\dots -1.2 V to 7 V
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the high state	\dots -0.5 V to V _{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F280B	. −55°C to 125°C
SN74F280B	0°C to 70°C
Storage temperature range	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54F280B			SI	LINUT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
lik	Input clamp current			-18			-18	mA
lOH	High-level output current			- 1			- 1	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEST CONDITIONS			N54F280	В	SI			
PARAMETER	TES	ST CONDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
V	V _{CC} = 4.5 V	I _{OH} = – 1 mA	2.5	3.4		2.5	3.4		V
Voн	$V_{CC} = 4.75 V$,	I _{OH} = – 1 mA				2.7			V
VOL	V _{CC} = 4.5 V	$I_{OL} = 20 \text{ mA}$		0.3	0.5		0.3	0.5	V
lį	$V_{CC} = 0$,	V _I = 7 V			0.1			0.1	mA
lіН	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
I _I L	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V			- 20			- 20	μΑ
I _{OS} §	V _{CC} = 5.5 V,	V _O = 0	-60		-150	-60		-150	mA
Icc	$V_{CC} = 5.5 \text{ V},$	V _I = 0		26	35		26	35	mA

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54F280B, SN74F280B 9-BIT PARITY GENERATORS/CHECKERS

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switching characteristics (see Note 2)

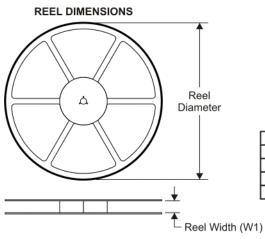
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R _I T _A	C = 5 V = 50 p = 500 s = 25°C	F, Ω,	C R T	L = 50 p L = 5009 L = MIN	Ω, to MAX†		UNIT
			MIN	TYP	MAX	SN54F MIN	MAX	SN74F MIN	MAX	
tPLH			3.2	6.1	9	2.7	13	2.7	10	
t _{PHL}	Any input	Σ EVEN	3.2	6.6	10	2.7	15	2.7	11	ns
t _{PLH}	Any input	ΣODD	3.2	6.1	9	2.7	14	2.7	10	no
^t PHL	Any input	2 000	3.2	6.6	10	2.7	14	2.7	11	ns

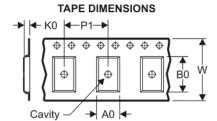
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.





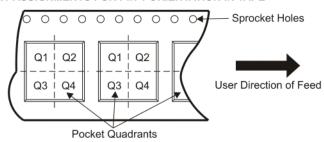
TAPE AND REEL INFORMATION





-		
		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F280BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F280BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F280BDR	SOIC	D	14	2500	346.0	346.0	33.0
SN74F280BNSR	SO	NS	14	2000	346.0	346.0	33.0

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