DLPA200 Digital Micromirror Device Driver

1 Features

- Generates the micromirror clocking pulses required by the DLP® Digital Micromirror Device (DMD)
- Generates specialized voltage levels required for micromirror clocking pulse generation
- Designed for use in multiple DLP chipsets

2 Applications

- Display:
  - Projectors
  - Personal electronics
  - Intelligent and adaptive lighting
  - Augmented reality and information overlay
- Industrial:
  - Direct imaging lithography
  - Additive manufacturing and 3D printers
  - 3D scanners for machine vision and inspection
  - Laser marking and repair systems
  - Computer-to-plate and industrial printers
- Medical:
  - Vascular or hyperspectral imaging
  - 3D Scanners for ear, teeth, and limb measurement
  - Microscopes
  - Ophthalmology

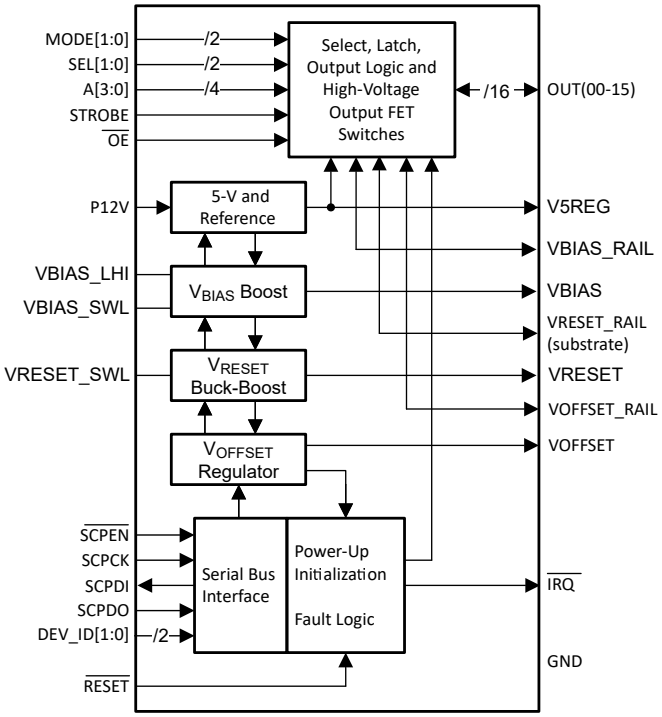
3 Description

The DLPA200 is a DLP® digital micromirror device (DMD) driver that generates the micromirror clocking pulses for certain DMDs in the DLP portfolio. A complete DLP chipset provides developers easier access to the DMD, as well as high-speed micromirror control.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
DLPA200	HTQFP (80)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2022) to Revision G (June 2023)	Page
• Added minimum value to V_{IN} in Section 7.1	6
• Updated F_{SW} values in Section 7.8	9
• Deleted Discharge time constant in Section 7.9	9
• Added Discharge current sink Section 7.9	9
• Updated drawing for proper logic polarity	12
• Updated Table 12-1	20

Changes from Revision E (August 2018) to Revision F (November 2022)	Page
• Changed Min/Typ/Max values for switching frequency F_{SW}	8

5 Device Configurations Table

Table 5-1. Device Configurations

DMD	DMD MICROMIRROR DRIVER	DIGITAL CONTROLLER
DLP9500 DLP 0.95 1080p 2xLVDS Type A DMD	2 ea. DLPA200	DLPC410 (+ DLPR410)
DLP7000 DLP 0.7 XGA 2xLVDS Type A DMD	1 ea. DLPA200	
DLP650LNIR DLP 0.65 WXGA NIR S450 DMD	1 ea. DLPA200	
DLP5500 DLP 0.55 XGA Series 450 DMD	1 ea. DLPA200	DLPC200

6 Pin Configuration and Functions

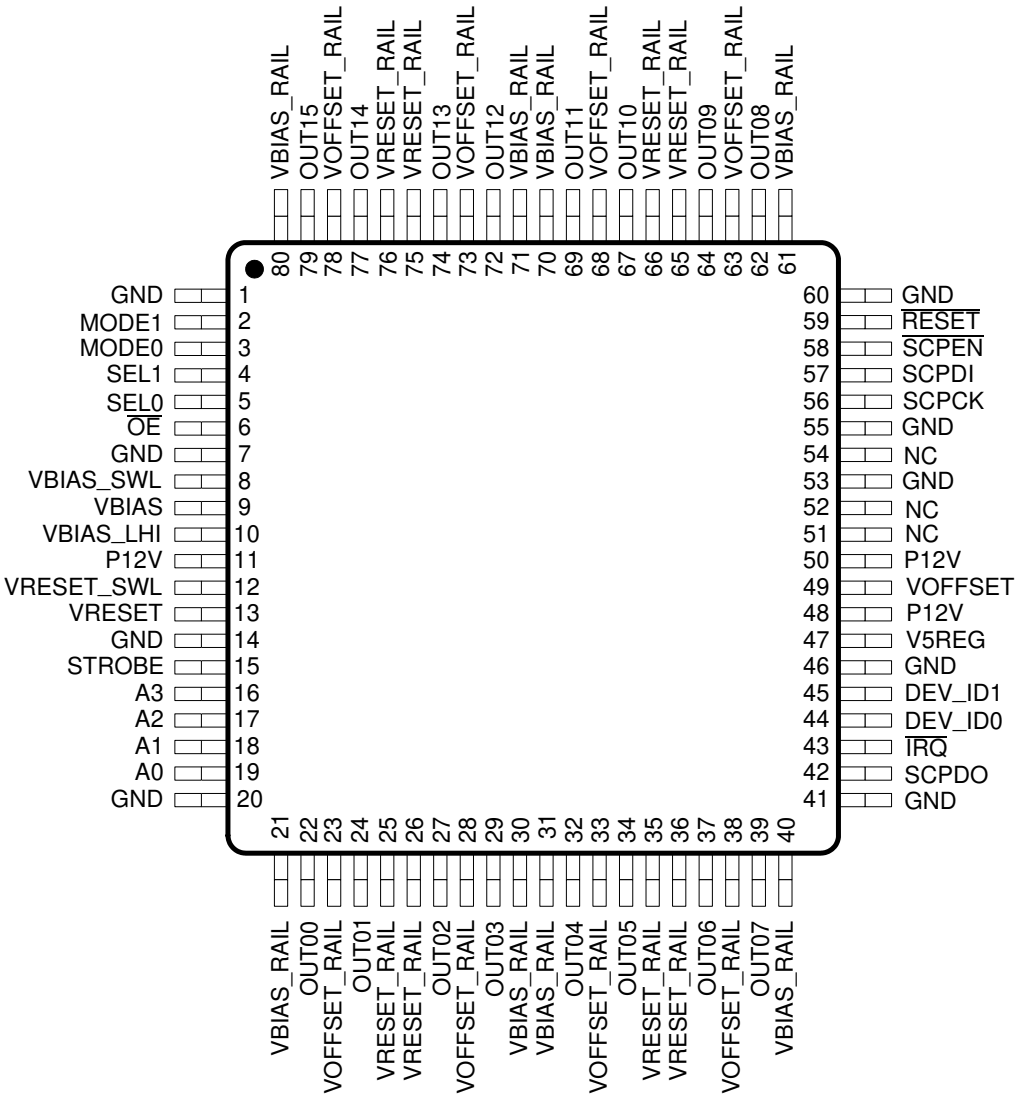


Figure 6-1. PFP Package 80-Pin HTQFP Top View

Table 6-1. Pin Functions

PIN		I/O (INPUT DEFAULT)[1]	DESCRIPTION
NAME	NO.		
OUT00	22	Output	16 micromirror clocking waveform outputs (enabled by $\overline{OE}$ = 0).
OUT01	24	Output	
OUT02	27	Output	
OUT03	29	Output	
OUT04	32	Output	
OUT05	34	Output	
OUT06	37	Output	
OUT07	39	Output	
OUT08	62	Output	
OUT09	64	Output	
OUT10	67	Output	
OUT11	69	Output	
OUT12	72	Output	
OUT13	74	Output	
OUT14	77	Output	
OUT15	79	Output	
A0	19	Input (pull down)	Output Address. Used to select which OUTxx pin is active at a given time.
A1	18	Input (pull down)	
A2	17	Input (pull down)	
A3	16	Input (pull down)	
MODE0	3	Input (pull down)	Mode Select. Used to determine the operating mode of the DLPA200.
MODE1	2	Input (pull down)	
SEL0	5	Input (pull down)	Output Voltage Select. Used to switch the voltage applied to the addressed OUTxx pin.
SEL1	4	Input (pull down)	
STROBE	15	Input (pull down)	A rising edge on STROBE latches in the control signals after a tristate delay.
$\overline{OE}$	6	Input (pull up)	Asynchronous input controls whether the 16 OUTxx pins are active or are in a in high-impedance state. $\overline{OE}$ = 0 : Enabled. $\overline{OE}$ = 1 : High Z.
$\overline{RESET}$	59	Input (pull up)	Resets the DLPA200 internal logic. Active low. Asynchronous.
$\overline{SCPEN}$	58	Input (pull up)	Enables serial bus data transfers. Active low.
SCPDI	57	Input (pull down)	Serial bus data input. Clocked in on the falling edge of SCPCK.
SCPCK	56	Input (pull down)	Serial bus clock. Provided by chipset controller.
SCPDO	42	Output	Serial bus data output (open drain). Clocked out on the rising edge of SCPCK. A 1kΩ pull up resistor to the Chip-Set Controller V_{DD} supply is recommended.
$\overline{IRQ}$	43	Output	Interrupt request output to the chipset Controller. Active low. A 1-kΩ pullup resistor to the Chip-Set Controller V_{DD} supply is recommended.
DEV_ID1	45	Input (pull up)	Serial bus device address: 00 = all; 01 = device 1; 10 = device 2; 11 = device 3.
DEV_ID0	44	Input (pull up)	
VBIAS	9	Output	One of three specialized voltages generated by the DLPA200
VBIAS_LHI	10	Input	Current limiter output for VBIAS supply (also the VBIAS switching inductor input)
VBIAS_SWL	8	Input	Connection point for VBIAS supply switching inductor
VBIAS_RAIL	21, 30, 31, 40, 61, 70, 71, 80	Input	The internally-used VBIAS supply rail. Internally isolated from VBIAS
VRESET	13	Output	One of three specialized voltages which are generated by the DLPA200. The package thermal pad is tied to this voltage level.

Table 6-1. Pin Functions (continued)

PIN		I/O (INPUT DEFAULT)[1]	DESCRIPTION
NAME	NO.		
VRESET_SWL	12	Input	Connection point for VRESET supply switching inductor
VRESET_RAIL[1]	25, 26, 35,36, 65, 66, 75, 76	Input	The internally-used VRESET supply rail. Internally isolated from VRESET.[1]
VOFFSET	49	Output	One of three specialized voltages which are generated by the DLPA200
VOFFSET_RAIL	23, 28, 33, 38, 63, 68, 73, 78	Input	The internally used VOFFSET supply rail. Internally isolated from VOFFSET
GND	1, 7, 14, 20, 41, 46, 53, 55, 60	GND	Common ground
V5REG	47	Output	The 5-volt logic supply output
P12V	11, 48, 50	Input	The main power input to the DLPA200
NC	51, 52, 54	No Connect	No connect

(1) The exposed thermal pad is internally connected to VRESET_RAIL.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
ELECTRICAL					
P12V	Load supply voltage			14	V
VRESET_SWL	Reset supply switching inductor connection point	(VRESET_SWL-VRESET_RAIL)		–1	V
VBIAS_RAIL	Internally-used V_{BIAS} supply rail	(VBIAS_RAIL-VRESET_RAIL)		60	V
VOFFSET_RAIL	Internally-used V_{OFFSET} supply rail	(VOFFSET_RAIL-VRESET_RAIL)		40.5	V
V_{IN}	Logic inputs		–0.3	7	V
V_{OUT}	Open drain logic outputs			7	V
ENVIRONMENTAL					
$T_{J(max)}$	Maximum junction temperature			125	°C
T_A	Operating temperature		0	75	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Section 7.1* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM)(2)	±2000	V
		Charged device model (CDM)(3)	800	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

at T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)(2)

POWER			MIN	NOM	MAX	UNIT
I_{P12V1}	P12V supply current(1)	Global shadow at 50 kHz, OUT load = 39 Ω and 390 pF, V5REG = 30 mA, V_{BIAS} = 26 V at 5 mA, V_{OFFSET} = 10V at 30 mA, V_{RESET} = –26 V		200		mA
I_{P12V2}		Outputs disabled and no external loads, V_{BIAS} = 19 V, V_{OFFSET} = 4.5 V, V_{RESET} = –19 V			22	mA
T_{JTSDR}	Thermal shutdown temperature	With device temperature rising	145	160	175	°C
		Hysteresis	5	10	15	°C
	Delta between thermal shutdown and thermal warning		5	10	15	°C
T_{JTWR}	Thermal warning temperature	With device temperature rising	125	140	155	°C
		Hysteresis	5	10	15	°C

(1) During power up the inrush power supply current can be as high as 1 A for a momentary period of time.
(2) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.

7.4 Thermal Information

THERMAL METRIC(1)		DLPA200 PFP (HTQFP) 80 PINS	UNIT
R_{c-j}	Thermal resistance, V_{BIAS} = 26 V, V_{RESET} = -26 V, V_{OFFSET} = 10 V, Output load = 390 pF and 39R on each output, Phase by one with global mode, Channel repetition frequency = 50 kHz, Additional external loads: I_{BIAS} = 5 mA, I_{OFFSET} = 30 mA, I_{5REG} = 30 mA	3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

7.5 Electrical Characteristics Control Logic

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level logic input voltage				0.8	V
V_{IH}	High-level logic input voltage		1.97			V
I_{IH}	High-level logic input current	V_{IN} = 5 V, input with pulldown. See terminal functions table.		40	50	µA
I_{IL}	Low-level logic input current	V_{IN} = 0 V, input with pullup. See terminal functions table.	–50	–40		µA
I_{IH}	High-level logic input leakage current	V_{IN} = 0 V, input with pulldown	–1		1	µA
I_{IL}	Low-level logic input leakage current	V_{IN} = 5 V, input with pullup	–1		1	µA
V_{OL}	Open drain logic outputs	I = 4 mA			0.4	V
I_{OL}	Logic output leakage current	V = 3.3 V			1	µA

7.6 5-V Linear Regulator

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{5REG}	Output voltage	Average voltage, I_{OUT} = 4 mA to 50 mA		4.75	5	5.25	V
I_{IL}	Output current: internal logic			4		20	mA
I_{IE}	Output current: external circuitry			0		30	mA
I_{CL5}	Current limit			80			mA
V_{UV5}	Undervoltage threshold	I_{OUT} = 50 mA	V5REG voltage increasing, P12V = 5.4 V		4.1		V
			V5REG voltage falling, P12V = 5.2 V		3.9		
V_{RIP}	Output ripple voltage(1)					200	mVpk-pk
V_{OS5}	Voltage overshoot at start up					2	%V5REG
t_{ss}	Power up	Measured between 10 to 90% of V5REG				1	ms

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

7.7 Bias Voltage Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I_{DL}	Output current: DMD load		0		5	mA
I_{CLFB}	Current limit flag	Corresponding current on output at P12V = 10.8 V	30			mA
I_{CLB}	Current limit	Measured on input	330	376	460	mA
V_{BIAS}	Output voltage		25.5	26	26.5	V
V_{UVB}	V_{BIAS} undervoltage threshold	Bias voltage falling	50		92	%VBIAS
V_{UVLHI}	VBIAS_LHI undervoltage threshold	VBIAS_LHI voltage increasing		8		V
		VBIAS_LHI voltage falling		6.5		V
R_{DS}	Boost switch $R_{DS(on)}$	T_J = 25°C		2		Ω
V_{RIP}	Output ripple voltage(1)				200	mVpk-pk
F_{SW}	Switching frequency		1.1	1.3	1.5	MHz
V_{OSB}	Voltage overshoot at start up				2	%VBIAS
t_{ss}	Power up	C_{OUT} = 3.3 µF, measured between 10 to 90% of target V_{BIAS}			1	ms
t_{dis}	Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

7.8 Reset Voltage Buck-Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω , repetition frequency = 50 kHz			3	mA
I_{CLFR}	Current limit flag	Corresponding current on output at P12V = 10.8 V	25			mA
I_{CLR}	Current limit	Measured on input	400		800	mA
V_{RESET}	Output voltage		–25.5	–26	–26.5	V
V_{UVR}	Undervoltage threshold	Reset voltage falling	50		92	%VRESET
R_{DS}	Buck-boost switch $R_{DS(on)}$	T_J = 25°C		8		Ω
V_{RIP}	Output ripple voltage(1)				200	mVpk-pk
F_{SW}	Switching frequency		1.1	1.3	1.5	MHz
V_{OSR}	Voltage overshoot at start up				2	%VRESET
t_{ss}	Power up	C_{OUT} = 3.3 µF, Measured between 10 to 90% of target V_{RESET}			1	ms
t_{dis}	Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

7.9 V_{OFFSET}/DMDVCC2 Regulator

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		12.2	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I_{DL}	Output current: DMDVCC2		0		30	mA
I_{CLO}	Current limit		100			mA
V_{OFFSET}	Output Voltage	DLP9500, DLP5500, DLP650LNIR	8.25	8.5	8.75	V
		DLP7000	7.25	7.5	7.75	
V_{UVO}	Undervoltage threshold	V_{OFFSET} voltage falling	50		92	%VOFFSET
V_{RIP}	Output ripple voltage(1)				100	mVpk-pk
V_{OSO}	Voltage overshoot at start-up				2	%VOFFSET
t_{ss}	Power up	C_{OUT} = 4.7 µF, Measured between 10 to 90% of target V_{OFFSET}			1	ms
I_{dis}	Discharge current sink		400			mA

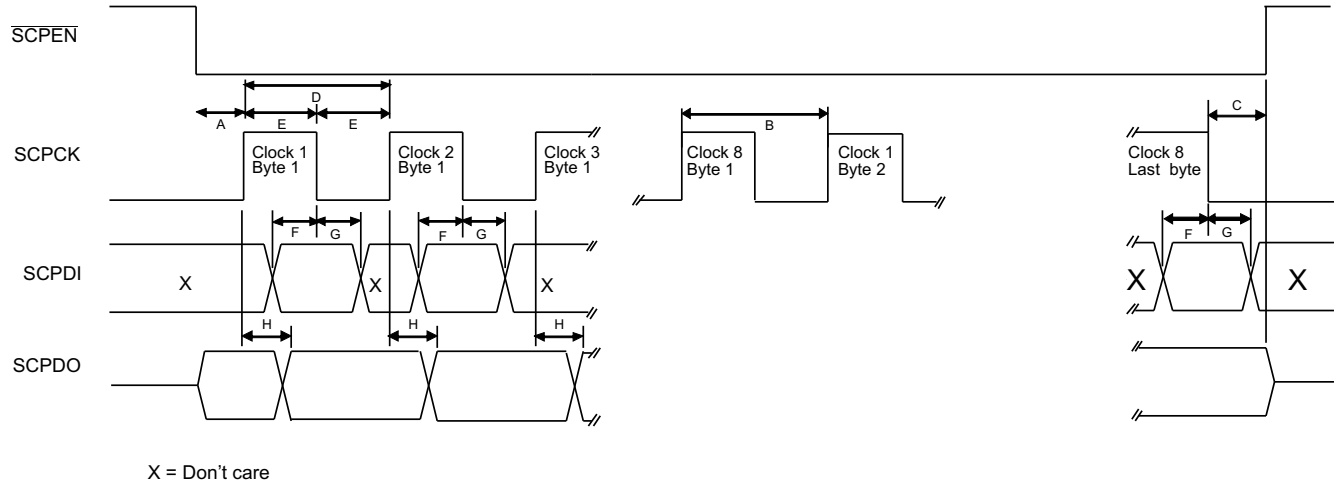
(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

7.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL COMMUNICATION PORT INTERFACE						
A(1)	Setup $\overline{SCPEN}$ low to SCPCK	Reference to rising edge of SCPCK	360			ns
B(1)	Byte to byte delay	Nominally 1 SCPCK cycle, rising edge to rising edge	1.9			µs
C(1)	Setup SCPDI to $\overline{SCPEN}$ high	Last byte to secondary disable	360			ns
D(1)	SCPCK frequency(2)		0		526	kHz
	SCPCK period		1.9	2		µs
E(1)	SCPCK high or low time		300			ns
F(1)	SCPDI set-up time	Reference to falling edge of SCPCK	300			ns
G(1)	SCPDI hold time	Reference from falling edge of SCPCK	300			ns
H(1)	SCPDO propagation delay	Reference from rising edge of SCPCK			300	ns
	$\overline{SCPEN}$, SCPCK, SCPDI, $\overline{RESET}$ filter (pulse reject)		150			ns
OUTPUT MICROMIRROR CLOCKING PULSES						
F_{PREP}	Phased reset repetition frequency each output pin (non-overlapping)				50	kHz
F_{GREP}	Global reset repetition frequency all output pins				50	kHz
I_{RLK}	V_{RESET} output leakage current	$\overline{OE}$ = 1, VRESET_RAIL = -28.5V		-1	-10	µA
I_{BLK}	V_{BIAS} output leakage current	$\overline{OE}$ = 1, VBIAS_RAIL = 28.5V		1	10	µA
I_{OLK}	V_{OFFSET} output leakage current	$\overline{OE}$ = 1, VOFFSET_RAIL = 10.25V		1	10	µA
OUTPUT MICROMIRROR CLOCKING PULSE CONTROLS						
t_{SPW}	STROBE pulse width		10			ns
t_{SP}	STROBE period		20			ns
t_{OHZ}	Output time to high impedance	$\overline{OE}$ Pin = High			100	ns
t_{OEN}	Output enable time from high impedance	$\overline{OE}$ Pin = Low			100	ns
t_{SUS}	Set-up time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t_{HOS}	Hold time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t_{PBR}	Propagation time	From STROBE to V_{BIAS}/V_{RESET} edge 50% point.	80		200	ns
t_{PRO}		From STROBE to V_{RESET}/V_{OFFSET} edge 50% point.	80		200	ns
t_{POB}		From STROBE to V_{OFFSET}/V_{BIAS} edge 50% point.	80		200	ns
t_{DEL}	Edge-to-edge propagation delta	Maximum difference between the slowest and fastest propagation times for any given reset output.			40	ns
t_{CHCH}	Output channel-to-channel propagation delta	Maximum difference between the slowest and fastest propagation times for any two outputs for any given edge.			20	ns

(1) See Figure 7-1
(2) There is no minimum speed for the serial port. It can be written to statically for diagnostic purposes.



X = Don't care

Figure 7-1. Serial Interface Timing

8 Detailed Description

8.1 Overview

Reliable function and operation of the DLPA200 requires that it be used in conjunction with the other components of a given DLP chipset. It is typical for the DMD controller to operate the DMD micromirror driver. For more information on the chipset components, see the appropriate DMD or DMD Controller Data Sheet (Table 12-1).

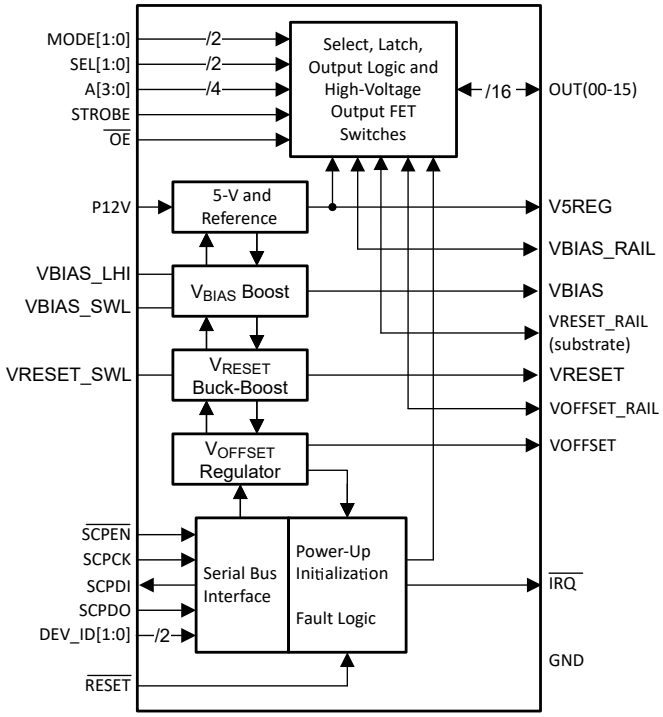
The DLPA200 consists of three functional blocks: A High-Voltage Power Supply function, a DMD Micromirror Clock Generation function, and a Serial Communication function.

The High-Voltage Power Supply function generates three specialized voltage levels: V_{BIAS} (19 to 28 V), V_{RESET} (–19 to –28 V), and V_{OFFSET} (4.5 to 10 V).

The Micromirror Clock Generation function uses the three voltages generated by the High-Voltage Power Supply function to create the sixteen micromirror clock pluses (output the OUTx pins of the DLPA200).

The Serial Communication function allows the chipset Controller to control the generation of V_{BIAS}, V_{RESET}, and V_{OFFSET}; control the generation of the micromirror clock pulses; status the general operation of the DLPA200.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 5-V Linear Regulator

The 5-V linear regulator supplies the 5-V requirement of the DLPA200 internal logic.

Figure 8-1 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA200 modules. See Section 9.1.1 for recommended component values.

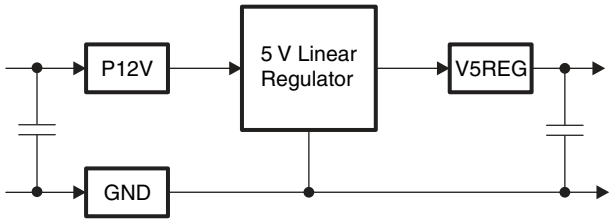


Figure 8-1. 5-Volt Linear Regulator Block Diagram

8.3.2 Bias Voltage Boost Converter

The bias voltage converter is a switching supply that operates at 1.5 MHz. The bias switching device switches 180° out-of-phase with the reset switching device.

The converter supplies the internal bias voltage for the high voltage FET switches and the external V_{BIAS} for the DMD Pond of Mirrors. The V_{BIAS} voltage level can be different for different generations of DMDs. The V_{BIAS} voltage level is configured by the DLP Controller chip over the Serial Communication Port (SCP). Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 8-2 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA200 modules. See Section 9.1.1 for recommended component values.

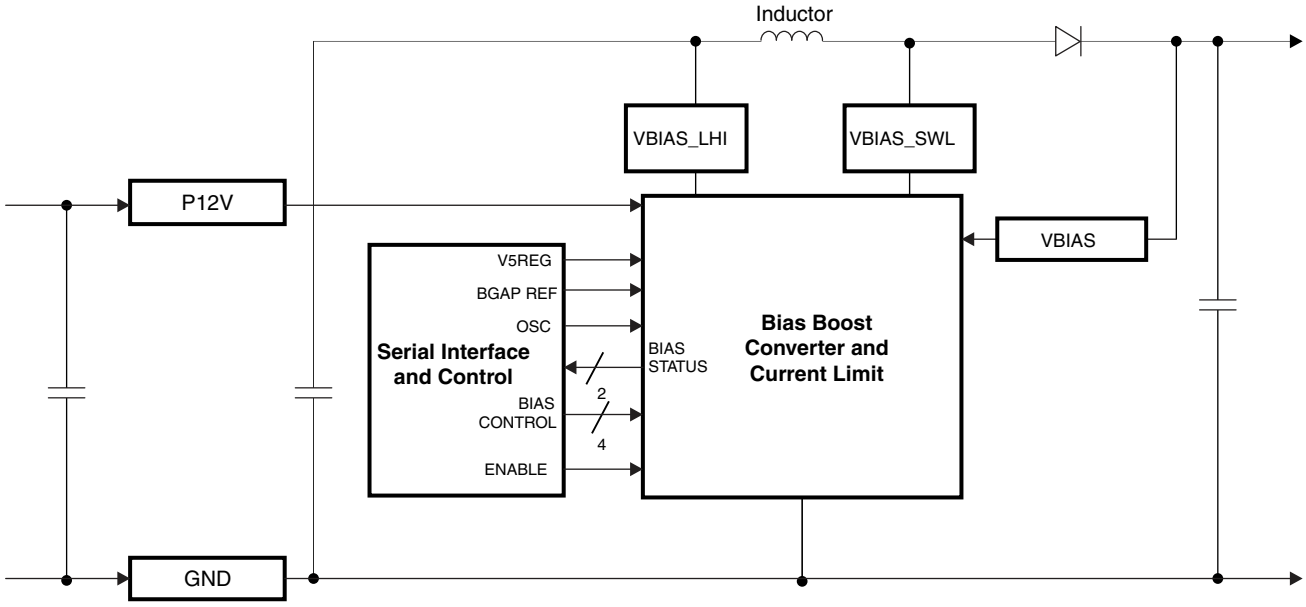


Figure 8-2. Bias Voltage Boost Converter Block Diagram

8.3.3 Reset Voltage Buck-Boost Converter

The reset voltage buck-boost converter is a switching supply that operates at 1.5 MHz. The reset switching device switches 180° out-of-phase with the bias switching device.

The converter supplies the internal reset voltage levels for the high voltage FET switches. The V_{RESET} voltage level can be different for different generations of DMDs. The V_{RESET} voltage level is configured by the DLP controller chip over the Serial Communication Port. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 8-3 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA200 modules. See Section 9.1.1 for recommended component values.

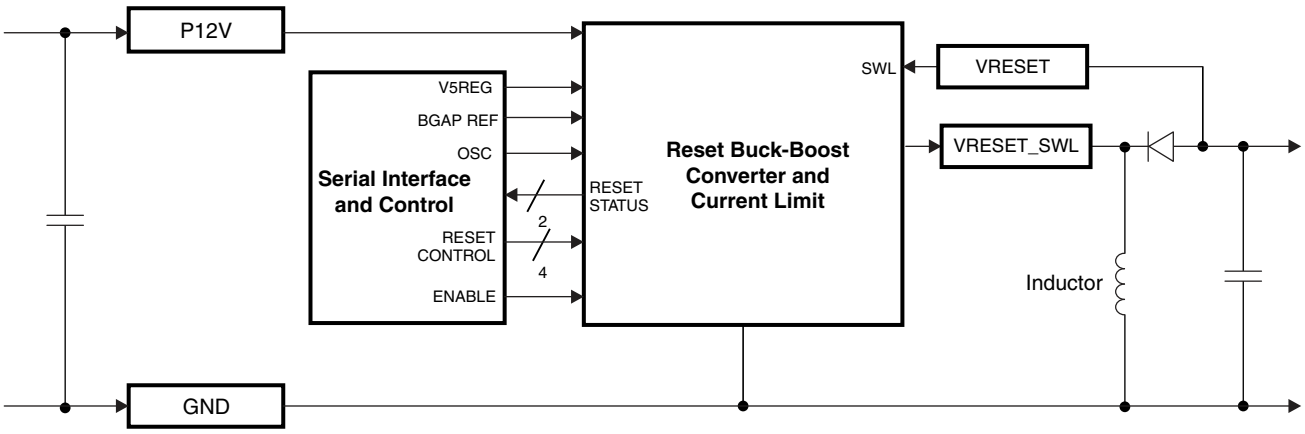


Figure 8-3. Reset Voltage Buck-Boost Converter Block Diagram

8.3.4 V_{OFFSET}/DMDVCC2 Regulator

The V_{OFFSET}/DMDVCC2 regulator supplies the internal V_{OFFSET} voltage for the high voltage FET switches and the external DMDVCC2 for the DMD. The V_{OFFSET} voltage level can be different for different generations of DMDs. The V_{OFFSET} voltage level is configured by the DLP Controller chip over the Serial Communication Port. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides 2 status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 8-4 shows the block diagram of this module. The input decoupling capacitors are shared with other DLPA200 modules. See Section 9.1.1 for recommended component values.

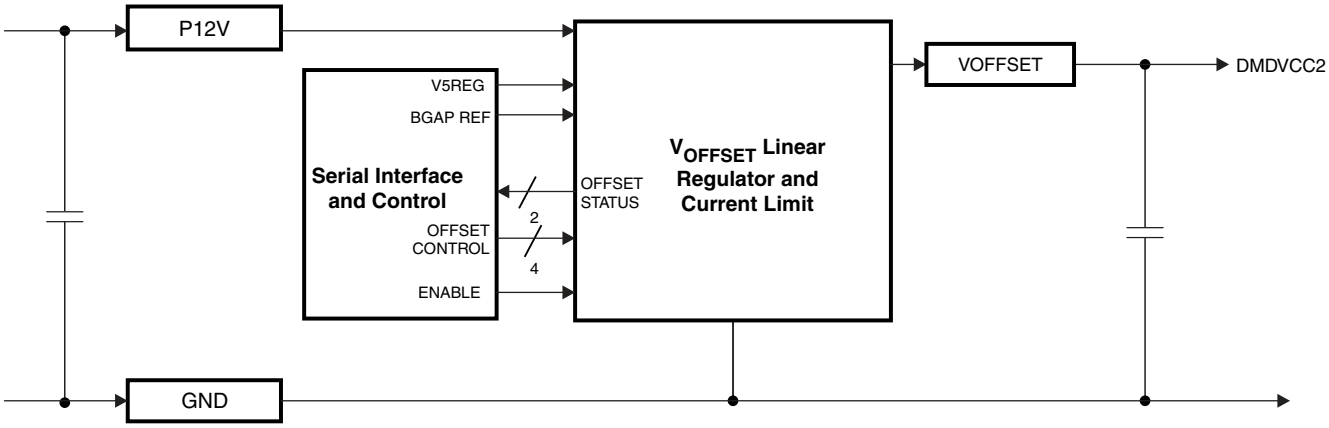


Figure 8-4. Offset Voltage Boost Convertor Block Diagram

8.3.5 Serial Communications Port (SCP)

The SCP is a full duplex, synchronous, character-oriented (byte) port that allows exchange of data between the primary ASIC or FPGA, and one or more secondary DLPA200s (and/or other DLP devices).

Table 8-1. Serial Communications Port Signal Definitions

SIGNAL	I/O	FROM/TO	TYPE	DESCRIPTION
SCPCK	I	SCP bus primary to secondary	LVTTL compatible	SCP bus serial transfer clock. The host processor (primary) generates this clock.
$\overline{\text{SCPEN}}$	I	SCP bus primary to secondary	LVTTL compatible	SCP bus access enable (low true). When high, secondary will reset to idle state, and SCPDO output will tri-state. Pulling $\overline{\text{SCPEN}}$ low initiates a read or write access. $\overline{\text{SCPEN}}$ must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull $\overline{\text{SCPEN}}$ high at any point.
SCPDI	I	SCP bus primary to secondary	LVTTL compatible	SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK.
SCPDO	O	SCP bus secondary to primary	LVTTL, open drain w/tri-state	SCP bus serial data output. Data bits must clocked out on the rising edge of SCPCK. A 1-kΩ pullup resistor to the 3.3 volt ASIC supply is required.
$\overline{\text{IRQ}}$	O	SCP bus secondary to primary	LVTTL, open drain	Not part of the SCP bus definition. Asynchronous interrupt signal from secondary to request service from primary. A 1-kΩ pullup resistor to the 3.3-V ASIC supply is required.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Component Selection Guidelines

Table 9-1. 5-V Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
P12V filter capacitor	10 to 33 µF, 20 VDC, 1Ω max ESR	Tantalum or ceramic	Positive Terminal: P12V, pin 11 (locate near pin 11)	Negative Terminal: Ground
P12V bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	P12V, pin 11 (locate near pin 11)	Ground
V5REG filter capacitor	0.1(1) to 1.0 µF, 10 VDC, 2.5Ω max ESR	Tantalum or ceramic	Positive Terminal: V5REG, pin 47 (locate near pin 47)	Negative Terminal: Ground
V5REG bypass capacitor	0.1 µF(1), 16 VDC, 0.1Ω max ESR	Ceramic	V5REG, pin 47 (locate near pin 47)	Ground

(1) To ensure stability of the linear regulator, use a capacitance with a value not less than 0.1 µF.

Table 9-2. Bias Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
LHI filter capacitor	10 µF, 20 VDC, 1-Ω max ESR	Tantalum or ceramic	Positive Terminal: VBIAS_LHI, pin 10 (locate near pin 10)	Negative Terminal: Ground
LHI bypass capacitor	0.1 µF, 50 VDC, 0.1-Ω max ESR	Ceramic	VBIAS_LHI, pin 10 (locate near pin 10)	Ground
VBIAS filter capacitor	1 to 10 µF, 35 VDC, 1-Ω max ESR; (3.3 µF nominal value)	Tantalum or ceramic	Positive Terminal: VBIAS, pin 9 (locate near pin 9)	Negative Terminal: Ground
VBIAS bypass capacitor	0.1 µF, 50 VDC, 0.1-Ω max ESR	Ceramic	VBIAS, pin 9 (locate near pin 9)	Ground
VBIAS_RAIL bypass capacitors (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground
Resistor jumper (optional)	0-Ω normally (1-Ω for testing(1))		VBIAS, pin 9	VBIAS_RAIL, pins 21 or 80
Inductor	22 µH, 0.5 A, 160 mΩ ESR	Coil Craft DT1608C-223 (or equivalent)	VBIAS_LHI, pin 10	VBIAS_SWL, pin 8
Schottky diode	0.5 A, 40 V (minimum)	OnSemi MBR0540T1G or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent)	Anode: VBIAS_SWL, pin 8	Cathode: VBIAS, pin 9

(1) Allows for VBIAS current measurement.

Table 9-3. Reset Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VRESET filter capacitor	1 to 10 µF, 35 VDC, 1Ω max ESR; (3.3 µF nominal value)	Tantalum or ceramic	Negative Terminal: VRESET, pin 13 (locate near pin 13)	Positive Terminal: Ground
VRESET bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VRESET, pin 13 (locate near pin 13)	Ground
VRESET_RAIL bypass capacitors (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VRESET_RAIL, pins 35 and 66 (locate near pins 35 and 66)	Ground
Resistor jumper (optional)	0-Ω normally (1Ω for testing(1))		VRESET, pin 13	VRESET_RAIL, pins 25 or 76
Inductor	22 µH, 0.5A, 160 mΩ	Coil Craft DT1608C-223 (or equivalent)	VRESET_SWL, pin 12	Ground
Schottky diode	0.5 A (minimum), 60 V	STMicroelectronics STPS0560Z or Infineon/ International Rectifier 10MQ060N (or equivalent)	Cathode: VRESET_SWL, pin 12	Anode: VRESET, pin 13

(1) Allows for VRESET current measurement.

Table 9-4. Offset Voltage Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VOFFSET/VCC2 filter capacitors (2 required)	1(1) to 4.7(2) µF, 35 VDC, 1Ω max ESR	Tantalum or ceramic	Positive Terminal: VOFFSET, pin 49 (1st Cap near pin 49) Positive Terminal: DMDVCC2 pins (2nd Cap at DMD)	Negative Terminal: Ground at DLPA200 Negative Terminal: VSS (Ground) at DMD
VOFFSET/VCC2 bypass capacitors (5 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VOFFSET, pin 49 (locate 1 near pin 49) DMD DMDVCC2 pins (locate 4 near DMD pins)	Ground at DLPA200 Ground at DMD
VOFFSET_RAIL bypass capacitor (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VOFFSET_RAIL, pins 28 and 73 (locate near pins 28 and 73)	Ground
Resistor jumper (optional)	0-Ω normal (1Ω for testing(3))		VOFFSET, pin 49	VOFFSET_RAIL, pins 38 or 63
Resistor jumper (optional)	0-ohm normal (1Ω for testing(4))		VOFFSET, pin 49	DMDVCC2 pins

(1) To ensure stability of the linear regulator, the absolute minimum output capacitance must not be less than 1.0 µF.
(2) Recommended value is 3.3 µF each. Different values are acceptable, provided that the sum of the two is 6.8 µF maximum.
(3) Allows for V_{OFFSET} current measurement
(4) Allows for DMDVCC2 current measurement

Table 9-5. Pullup Resistors

COMPONENT	VALUE (kΩ)	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
Resistor	1		SCPDO, pin 42	Chipset controller 3.3-V V_{DD}
Resistor	1		$\overline{IRQ}$, pin 43	Chipset Controller 3.3-V V_{DD}
Resistor (optional)	1		$\overline{OE}$, pin 6	Chipset Controller 3.3-V V_{DD}

10 Power Supply Recommendations

10.1 Power Supply Rail Guidelines

Table 9-1 through Table 9-5 provides discrete component selection guidelines.

- Ensure that the P12V filter and bypass capacitors are distributed and connected to pin 11 and pin 48 and pin 50. Place these capacitors as close to their respective pins as possible and if necessary, place on the bottom layer.
- The V5REG filter and bypass capacitors must be placed near and connected to pin 47.
- It is best to route the VBIAS_RAIL etch runs in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. Ensure that the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Locate the bypass capacitors near and connected to pin 30 and pin 71 to provide bypassing on both sides.
- The VBIAS_LHI filter and bypass capacitors must be placed near and connected to pin 10.
- The VBIAS filter and bypass capacitors must be placed near and connected to pin 9.
- VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS_RAIL at or between pins 21 and 80.
- Route the VRESET_RAIL etch runs in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Bypass capacitors must be placed near and connected to pins 35 and 66 to provide bypassing on both sides.
- The VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-Ω resistor) to VRESET_RAIL at or between pin 25 and pin 76.
- Route the VOFFSET_RAIL etch runs in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Place the bypass capacitors near and connected to pin 28 and pin 73 to provide bypassing on both sides.
- The VOFFSET filter and bypass capacitors must be placed near and connected to pin 49.
- VOFFSET pin 49 must also be connected (optionally with a 0-Ω resistor) to VOFFSET_RAIL at or between pin 38 and pin 63.

Note

Aluminum electrolytic capacitors may not be suitable for the DLPA200 application. At the switching frequencies used in the DLPA200 (up to 1.5 MHz), aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails, which could cause the device to shut down or perform in an unreliable manner.

11 Layout

11.1 Layout Guidelines

CAUTION

Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DLPA200.

CAUTION

Thermal pads must be tied to VRESET_RAIL. Do not connect to ground.

Provide suitable Kelvin connections for the switching regulator feedback pins: V_{BIAS} (pin 9) and V_{RESET} (pin 13).

Make the PCB traces that connect the switching devices: VBIAS_SWL (pin 8) and VRESET_SWL (pin 12) as short and wide as possible to minimize leakage inductances. Make the PCB traces that connect the switching converter components (inductors, flywheel diodes and filtering capacitors) as short and wide as possible. Ensure that the electrical loops that these components form are as small and compact as possible, with the ground referenced components forming a star connection.

Due to the fast switching transitions appearing on the sixteen reset OUTx pins, it is recommended to keep these traces as short as possible. Also, to minimize potential cross-talk between outputs, it is advisable to maintain as much clearance between each of the output traces.

11.1.1 Grounding Guidelines

Ensure that the PWB has an internal ground plane that extends under the DLPA200. All nine ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

11.2 Thermal Considerations

Thermally bond or solder the DLPA200 package to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 mm × 10 mm centered under the device. The metal bottom of the package is tied internally to the substrate at the VRESET_RAIL voltage level. Therefore, the thermal pad on the board must be isolated from any other extraneous circuit or ground and no circuit vias are allowed inside the pad area. Thermal pads are required on both sides of the PWB. Connect the thermal pads together through an array of 5 × 5 thermal vias, 0.5 mm in diameter.

Thermal pads and the thermal vias are connected to VRESET_RAIL and must be isolated from ground, or any other circuit.

Locate an internal P12V plane directly underneath the top layer and have an isolated area under the DLPA200. This isolated area must be a minimum of 20 cm^2 and connect to the thermal pad of the DLPA200 through the thermal vias. The potential of the isolated area will also be at VRESET_RAIL. The internal ground plane must extend under the DLPA200 to help carry the heat away. Please refer to the PowerPAD Thermally Enhanced Package application report (SLMA002) for details on thermally efficient package design considerations.

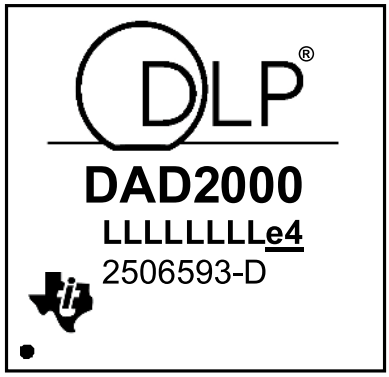
Be careful to place the DLPA200 device away from local PWB hotspots. Heat generated from adjacent components may impact the DLPA200 thermal characteristics.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The device marking consists of the fields shown in Figure 12-1.



PART MARKING CODES

LLLLLLLL = Lot trace code or date code

e4 = Pb-Free NiPdAu terminal finish

● = Pin 1 designator

2506593 = TI internal part number

D = revision letter

Figure 12-1. Device Marking (Device Top View)

DLPA200PFP is functionally equivalent to 2506593-0005N.

12.2 Documentation Support

12.2.1 Related Documentation

Table 12-1. Links to Related Documentation

Document	TI Literature Number
PowerPAD™ Thermally Enhanced Package Application Report	SLMA002

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPA200PFP	ACTIVE	HTQFP	PFP	80	5	TBD	Call TI	Call TI	0 to 75		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

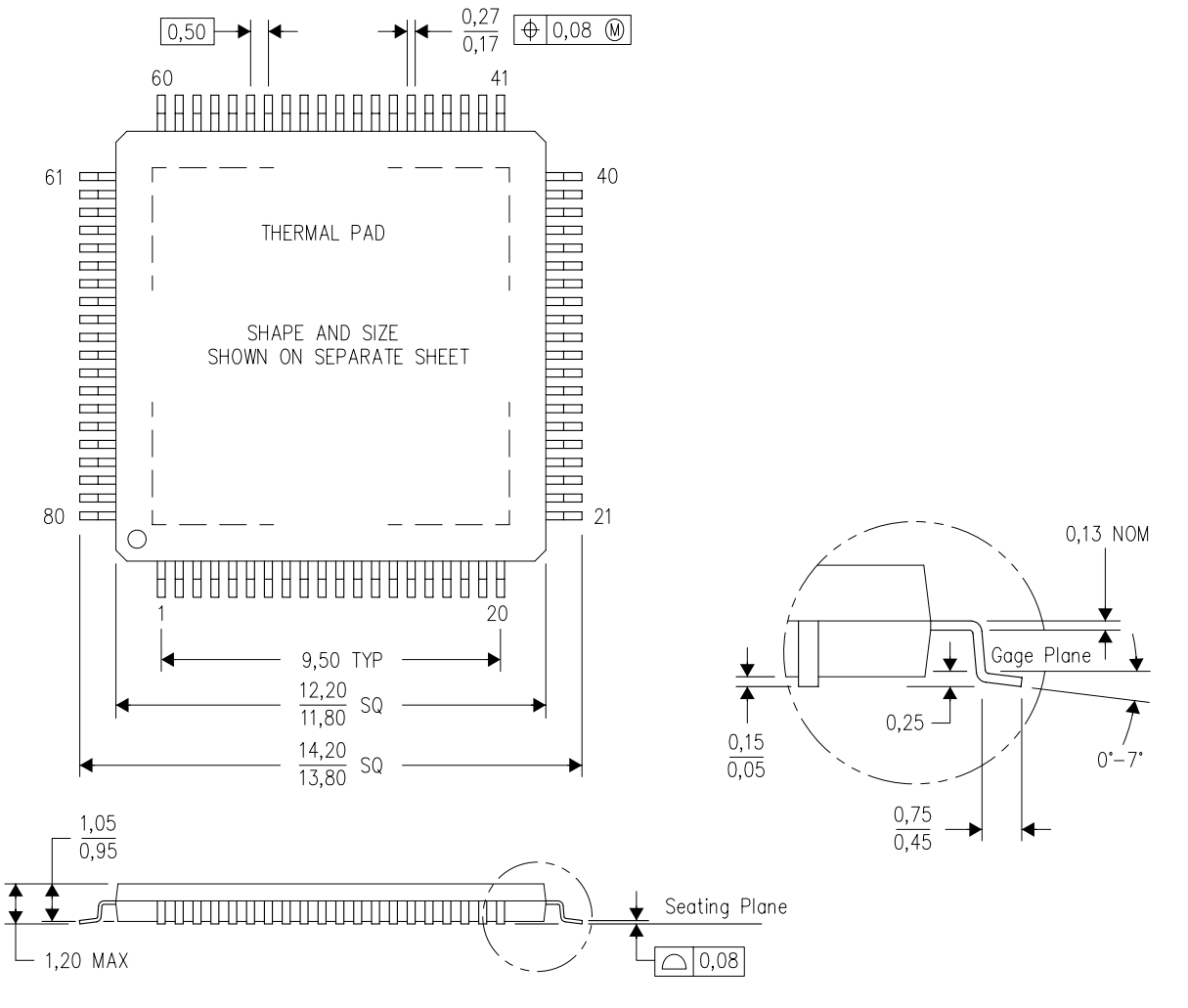
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

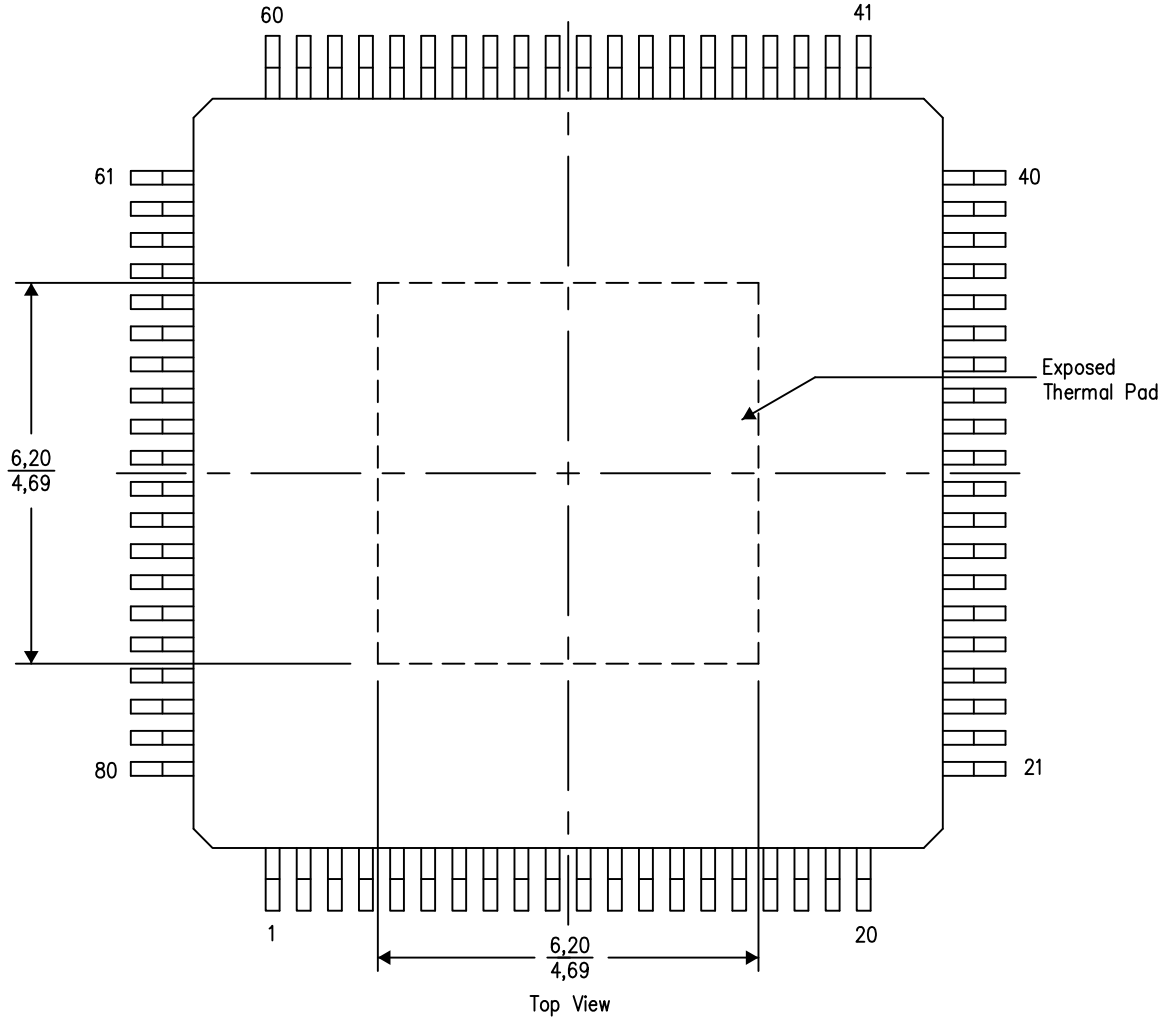
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

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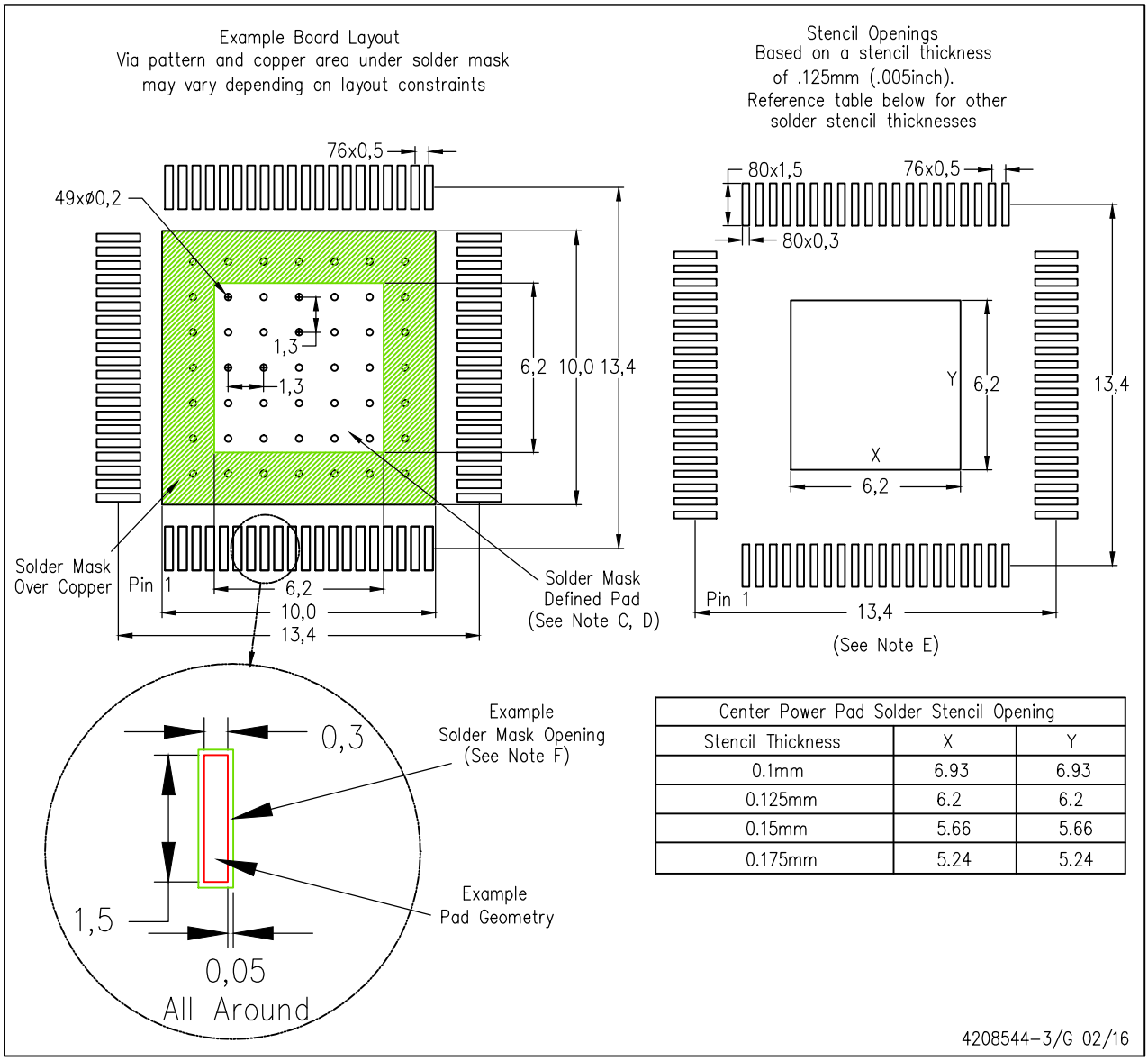
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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