TEXAS INSTRUMENTS

TPS78833EVM

LDO Regulator Evaluation Module

User's Guide

January 2002 *Power Management Products Low Power*

SLVU059

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DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7–13.5 V and the output current range of 0 mA to150 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the TPS78833EVM LDO regulator evaluation module. Each EVM contains an SLVP191 test board with a TPS78833DBV low dropout linear regulator as well as supporting passive components. The SLVP191 test board provides a convenient method of evaluating the performance of the TPS788xx linear regulator family as well as other SOT–23 packaged linear regulators with the same pinout.

How to Use This Manual

- Chapter 1—Introduction
- Chapter 2—EVM Test Setup
- Chapter 3—Test Results

Related Documentation From Texas Instruments

- TPS788xx data sheet (literature number SLVS382)

Contents

Figures

Tables

Chapter 1

Introduction

This user's guide describes the TPS78833EVM LDO regulator evaluation module (SLVP191). Each EVM contains an SLVP191 test board with a TPS78833DBV low dropout linear regulator as well as supporting passive components.

Topic **Page**

1.1 TPS788xx Family of LDO Regulators

The TPS788xx family of LDO regulators consists of small SOT–23 packaged regulators capable of delivering 150 mA of output current. The SR pin of the part can be used to control the output voltage slew rate and therefore the in-rush current of the device. In-rush current control is critical for many USB applications. Other features of the part include:

- $V_{I(max)}$ = 13.5 V
- Low 17-µA quiescent current across entire load range
- Less than 1-µA quiescent current in standby mode
- Low dropout voltage (typically 150 mV at 150 mA)
- Over current and thermal protection

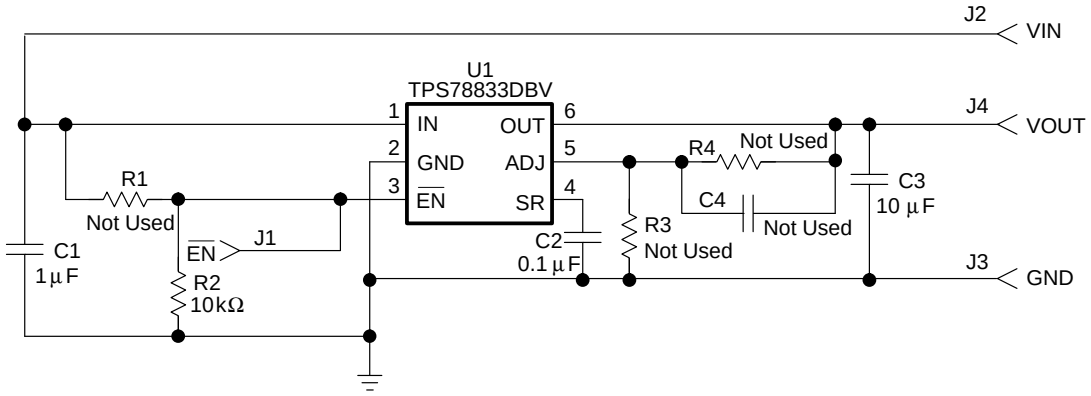
1.2 EVM Design Strategy

The purpose of this EVM is to facilitate evaluation of the TPS788xx family of LDO regulators. Each EVM contains an SLVP191 test board with a TPS78833DBV low dropout linear regulator as well as supporting passive components. Also, the board's small size and side clips facilitate attaching it to other PCB's as a power module.

1.3 Schematic

Figure 1–1 shows the SLVP191 PCB schematic diagram, which is used in the TPS78833EVM.

Figure 1–1. TPS78833EVM Schematic Diagram



1.4 Bill of Materials

Table 1–2 lists materials required for the TPS78833 EVMs.

Table 1–1. TPS78833EVM Bill of Materials

Qty	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, Ceramic, 1.0-µF, 6.3 V, 10%	603	Murata	GRM39X7R105K6.3
1	C2	Capacitor, Ceramic, 0.1-µF, 16 V, 10%	603	Murata	GRM39X7R104K016D
1	C3	Capacitor, Tantalum, 10-µF, 10 V, 20%	B Case	VISHAY	293D106X0010B2T
	C4	Not used	603		
1	J1	Clip, Surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA-D36W-0FC
1	J2	Clip, Surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA-D36W-0FC
1	J3	Clip, Surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DAD36W-0FC
1	J4	Clip, Surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DAD36W-0FC
	R1	Not used	603	Std	Std
1	R2	Resistor, Chip, 10.0 kΩ, 1/16 W, 1%	603	Std	Std
	R3	Not used	603	Std	Std
	R4	Not used	603	Std	Std
1	U1	IC, High PSRR, low noise LDO, 3.3 V, 100 mA	SOT23–5	TI	TPS78833DBV
1		PCB, 0.705 In × 0.570 In × 0.031		Any	SLVP191

1.5 Board Layout

Figures 1–2 and 1-3 show the board layout for the TPS78833EVM.

Figure 1–2. Top Layer

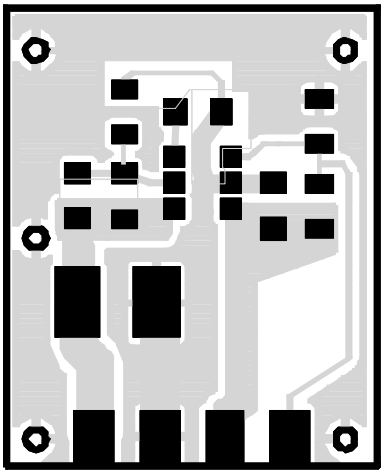


Figure 1–3. Bottom Layer

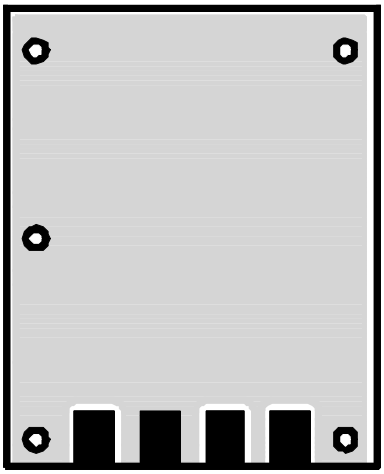
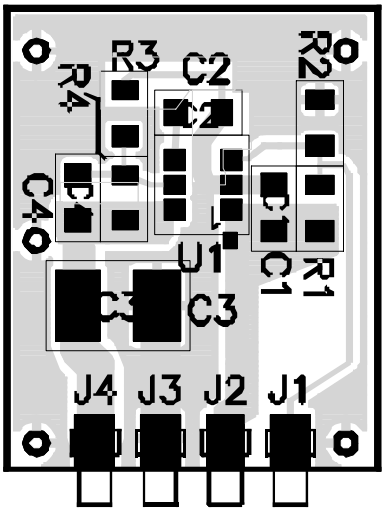


Figure 1–4. Assembly Drawing—Top

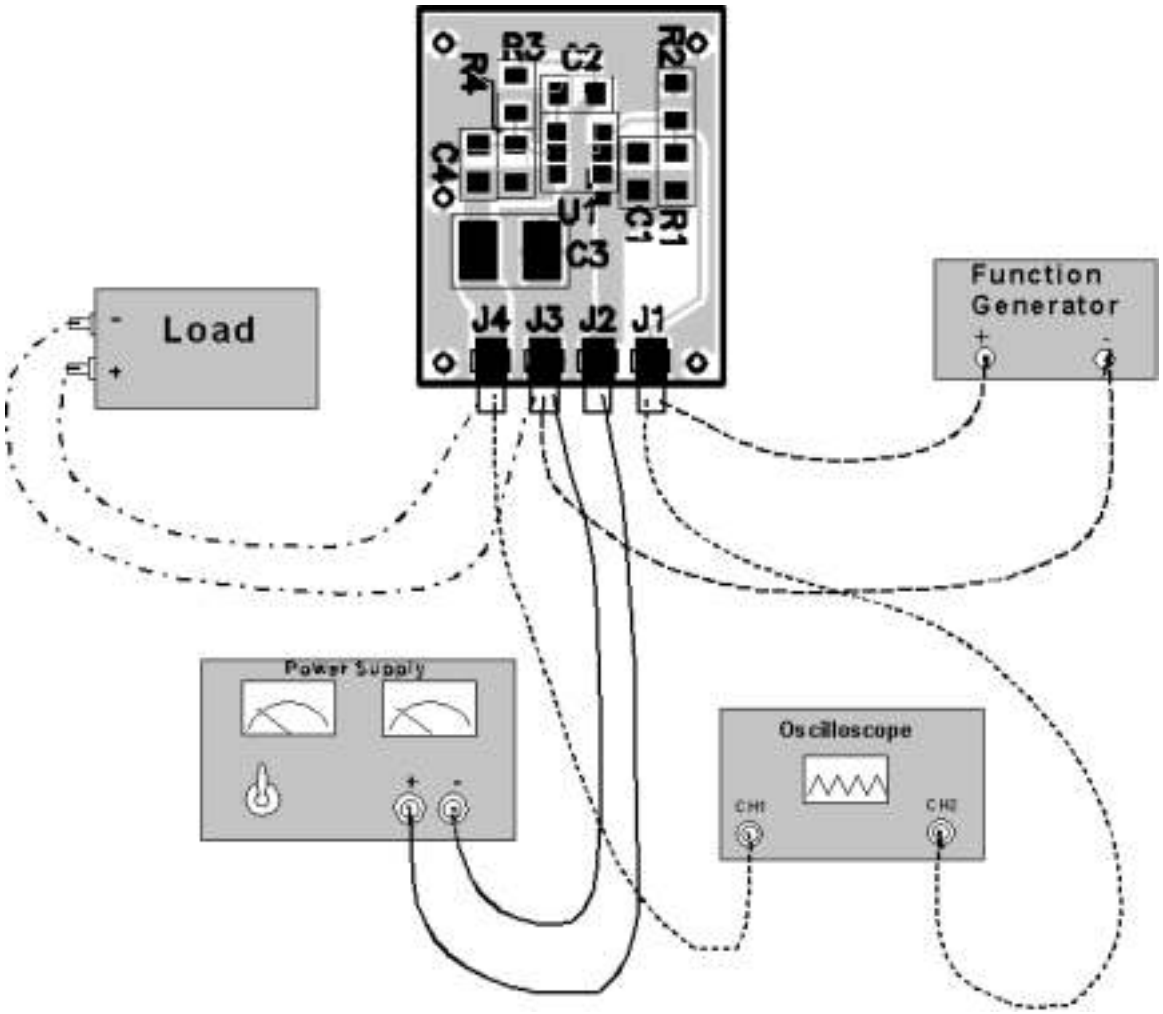


Chapter 2

EVM Test Setup

This chapter provides recommended test equipment and procedure for performing evaluations using the TPS78833EVM. Figure 2–1 shows the test setup.

Figure 2–1. Recommended TPS78833EVM Test Setup



The settings for the test equipment shown in Figure 2–1 are described below:

- Power supply set to 5-V and 1-A current limit connected to IN (J2) and GND (J3).
- Function generator set to 1 Hz, 25% duty cycle, 0-V to 5-V amplitude square wave (may require setting of 2.5-V square wave and 2.5-V dc offset) with positive side connected to EN (J1) and negative to GND (J4)
- Oscilloscope with the time scale set to 10 ms/div, channel 1 connected to OUT (J4), and channel 2 connected to EN (J1). Set the oscilloscope to trigger off of the falling edge of channel 2 of the oscilloscope.
- Appropriately sized resistance for desired output current between OUT (J4) and GND (J3).

Powering up the device and function generator will result in an oscilloscope plot similar to the one in Chapter 3.

Chapter 3

Test Results

This chapter gives laboratory test results of the TPS78833EVM obtained for the recommended test procedures in Chapter 2.

Figure 3–1 shows start up of the TPS78833 device with different capacitors on the SR pin.

Figure 3–1. Output Voltage, Enable Voltage vs Time (Start-Up)