



# PSMN4R1-30YLC

N-channel 30 V 4.35mΩ logic level MOSFET in LPAK using NextPower technology

12 February 2013

Product data sheet

## 1. General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

## 3. Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

## 4. Quick reference data

Table 1. Quick reference data

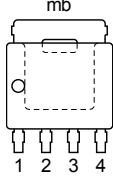
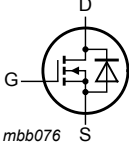
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 1</a>	-	-	92	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	67	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a>	-	4.75	5.7	mΩ
		$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a>	-	3.65	4.35	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 20\text{ A}; V_{DS} = 15\text{ V};$ <a href="#">Fig. 14; Fig. 15</a>	-	3.5	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}$ ; $I_D = 20 \text{ A}$ ; $V_{DS} = 15 \text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	11	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R1-30YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R1-30YLC	4C130L

## 8. Limiting values

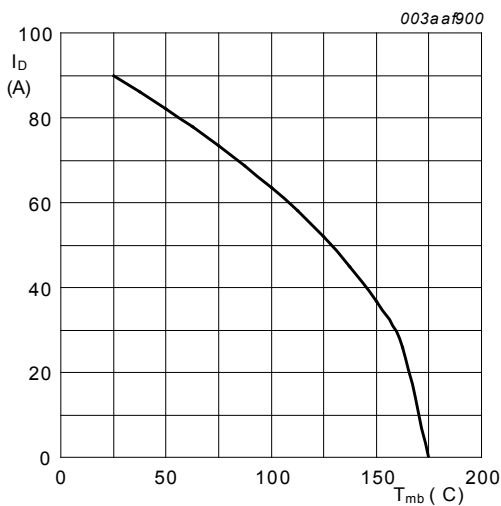
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ °C}$ ; <a href="#">Fig. 1</a>	-	92	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ °C}$ ; <a href="#">Fig. 1</a>	-	65	A

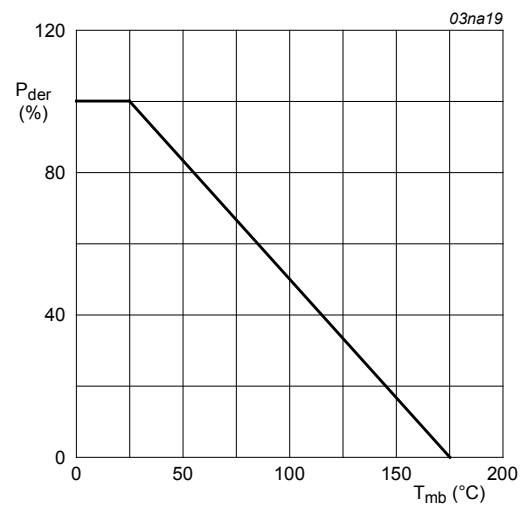
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Symbol	Parameter	Conditions	Min	Max	Unit
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 4</a>	-	367	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	67	W
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
$V_{ESD}$	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	270	-	V
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	61	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	367	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; $I_D = 92 \text{ A}$ ; $V_{sup} \leq 30 \text{ V}$ ; $R_{GS} = 50 \text{ } \Omega$ ; unclamped; <a href="#">Fig. 3</a>	-	21	mJ



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 10V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

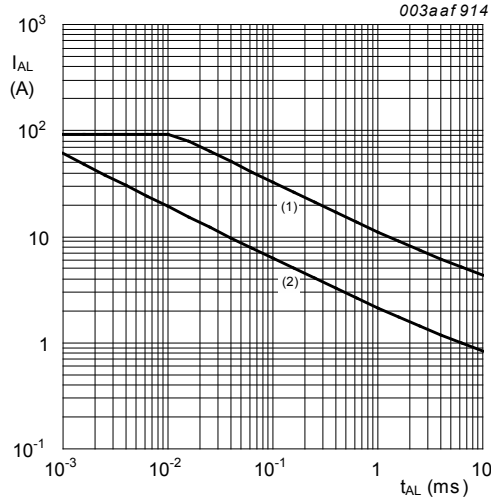


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (TIT)} = 25^{\circ}C$ ; (2)  $T_{j (TIT)} = 100^{\circ}C$

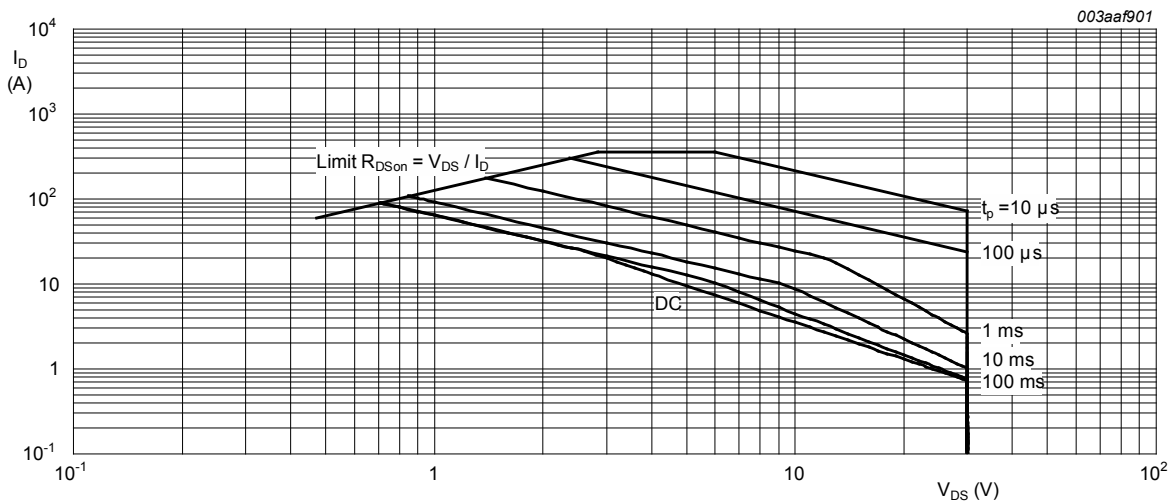


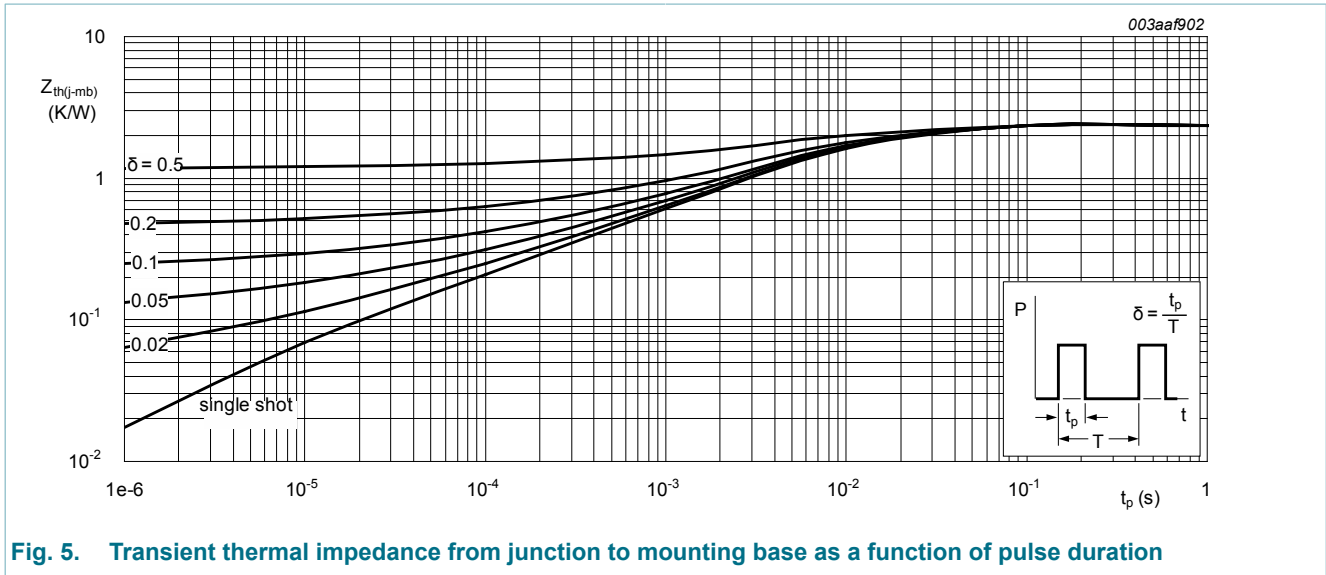
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.05	2.24	K/W



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	1.05	1.58	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	-	2.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	4.75	5.7	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 20 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	9.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	3.65	4.35	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	7.25	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.9	3.8	Ω

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	23	-	nC
		I <sub>D</sub> = 20 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	11	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	20	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	3.5	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	2.3	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	1.2	-	nC
Q <sub>GD</sub>	gate-drain charge		-	3.5	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 15 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	2.66	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	1502	-	pF
C <sub>oss</sub>	output capacitance		-	316	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	106	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; R <sub>L</sub> = 0.6 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 4.7 Ω	-	16	-	ns
t <sub>r</sub>	rise time		-	19	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	24	-	ns
t <sub>f</sub>	fall time		-	10	-	ns
Q <sub>oss</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 15 V; f = 1 MHz; T <sub>j</sub> = 25 °C	-	8	-	nC
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.8	1.1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 15 V	-	23	-	ns
Q <sub>r</sub>	recovered charge		-	15	-	nC
t <sub>a</sub>	reverse recovery rise time	V <sub>GS</sub> = 0 V; I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>DS</sub> = 15 V; <a href="#">Fig. 18</a>	-	13.5	-	ns
t <sub>b</sub>	reverse recovery fall time		-	9.5	-	ns

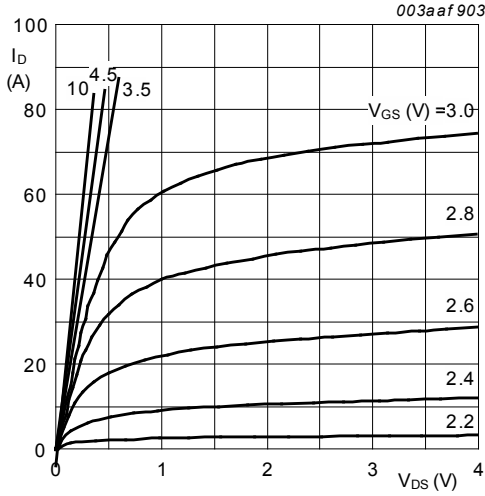


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

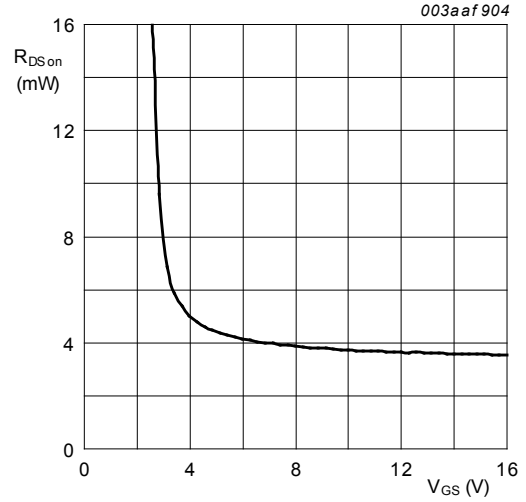


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 20\text{A}$

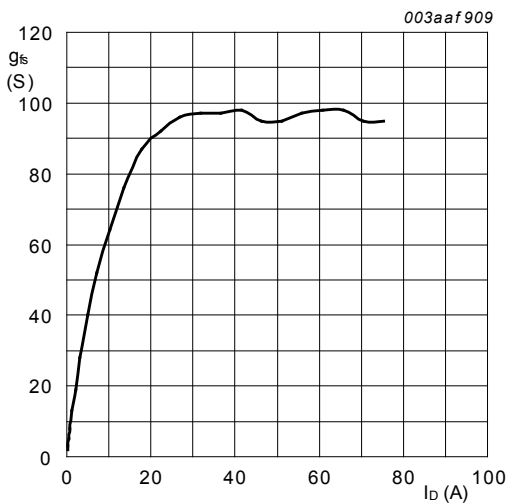


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

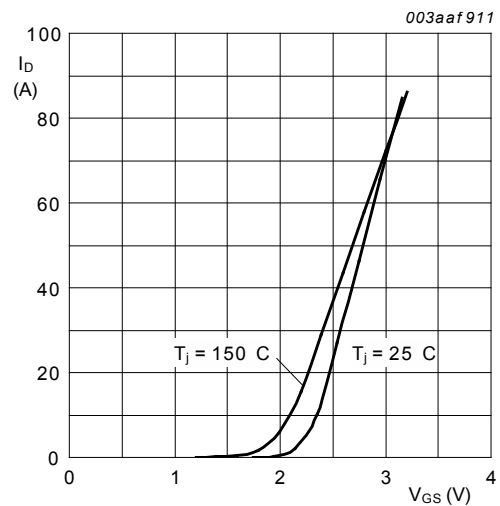


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

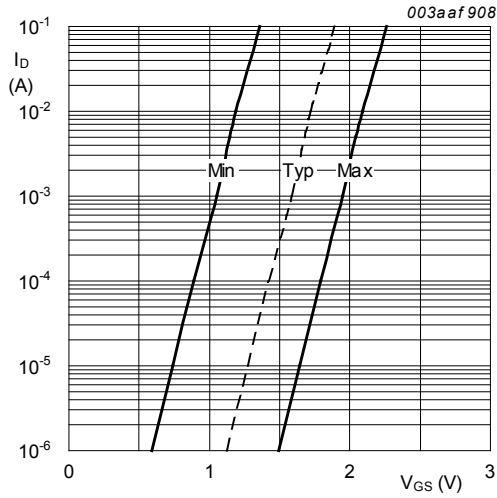


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

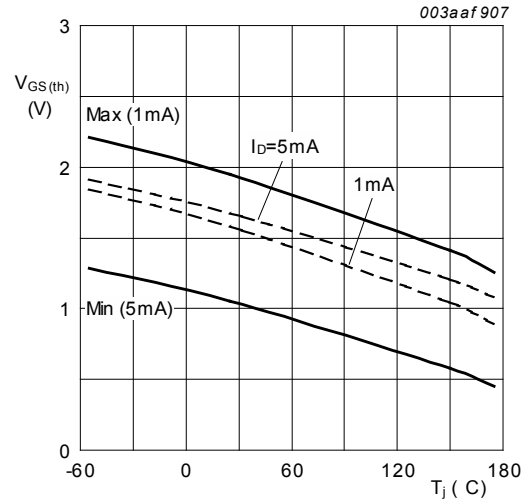


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$V_{DS} = V_{GS}$$

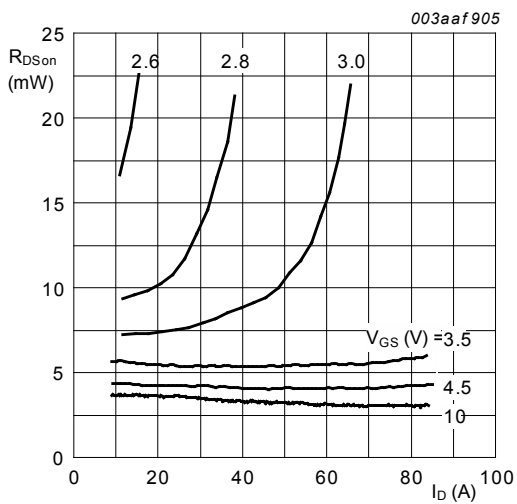


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

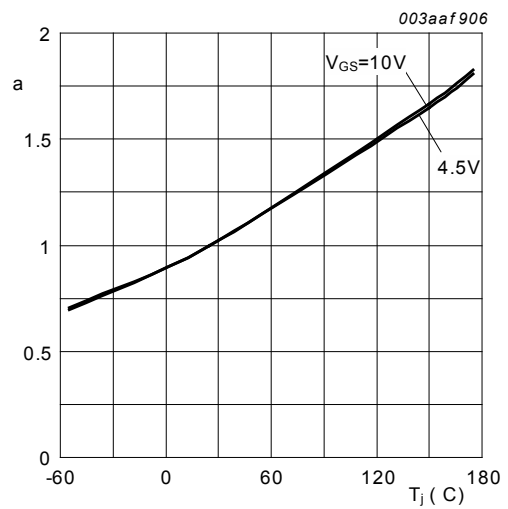


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



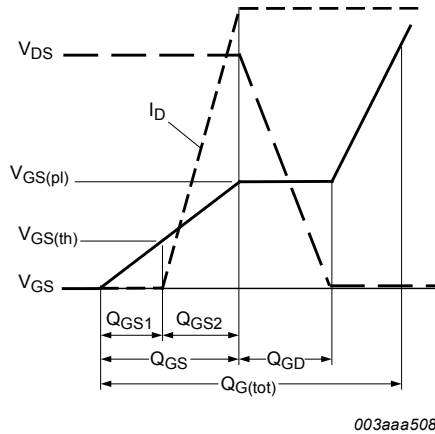


Fig. 14. Gate charge waveform definitions

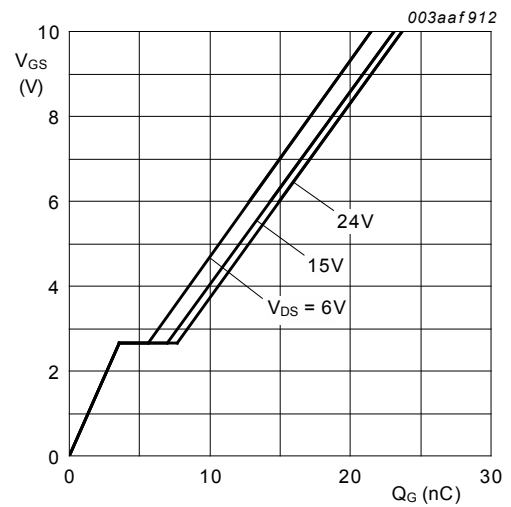


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 20 A$

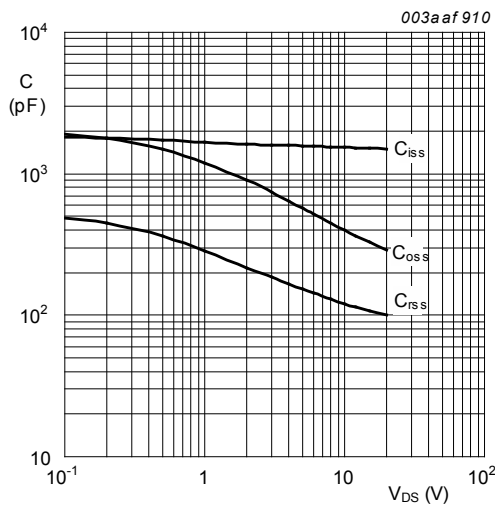


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0 V; f = 1 MHz$

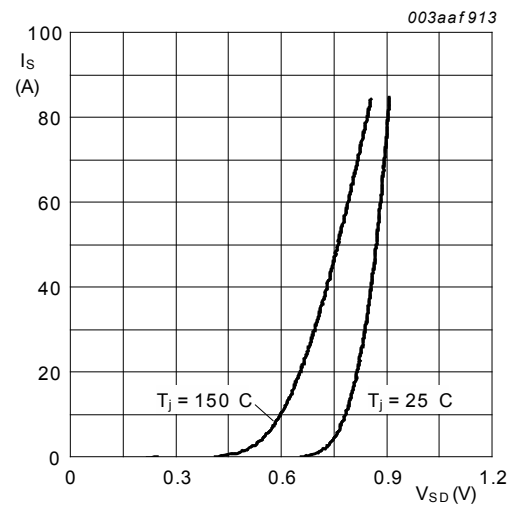


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0 V$

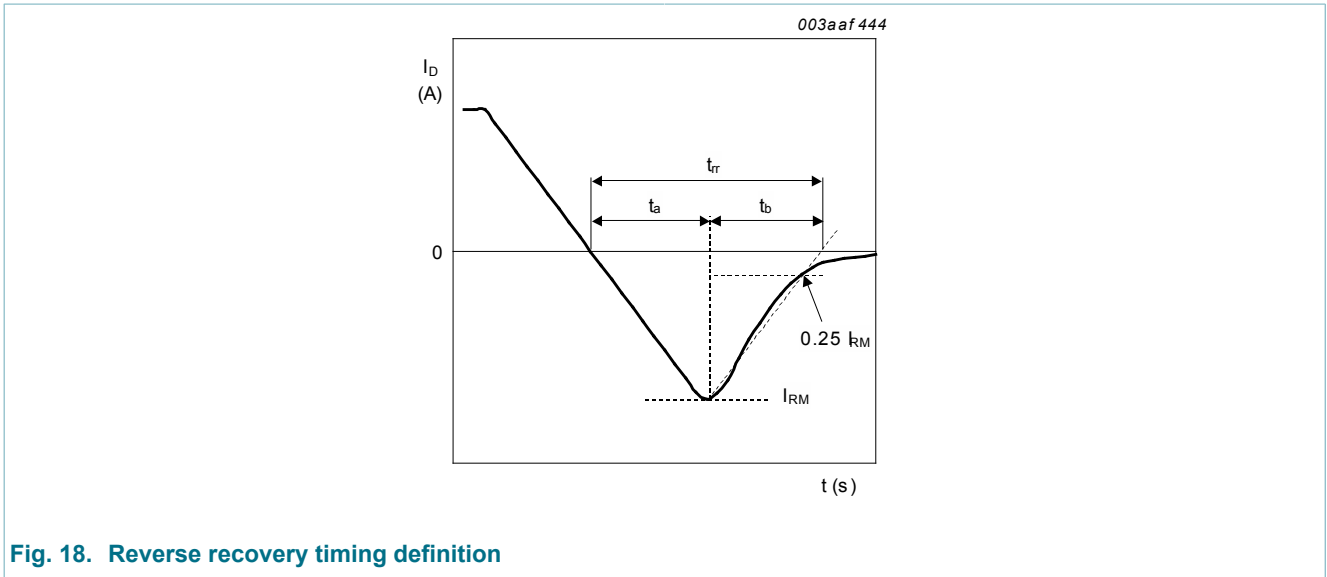


Fig. 18. Reverse recovery timing definition

### 11. Package outline

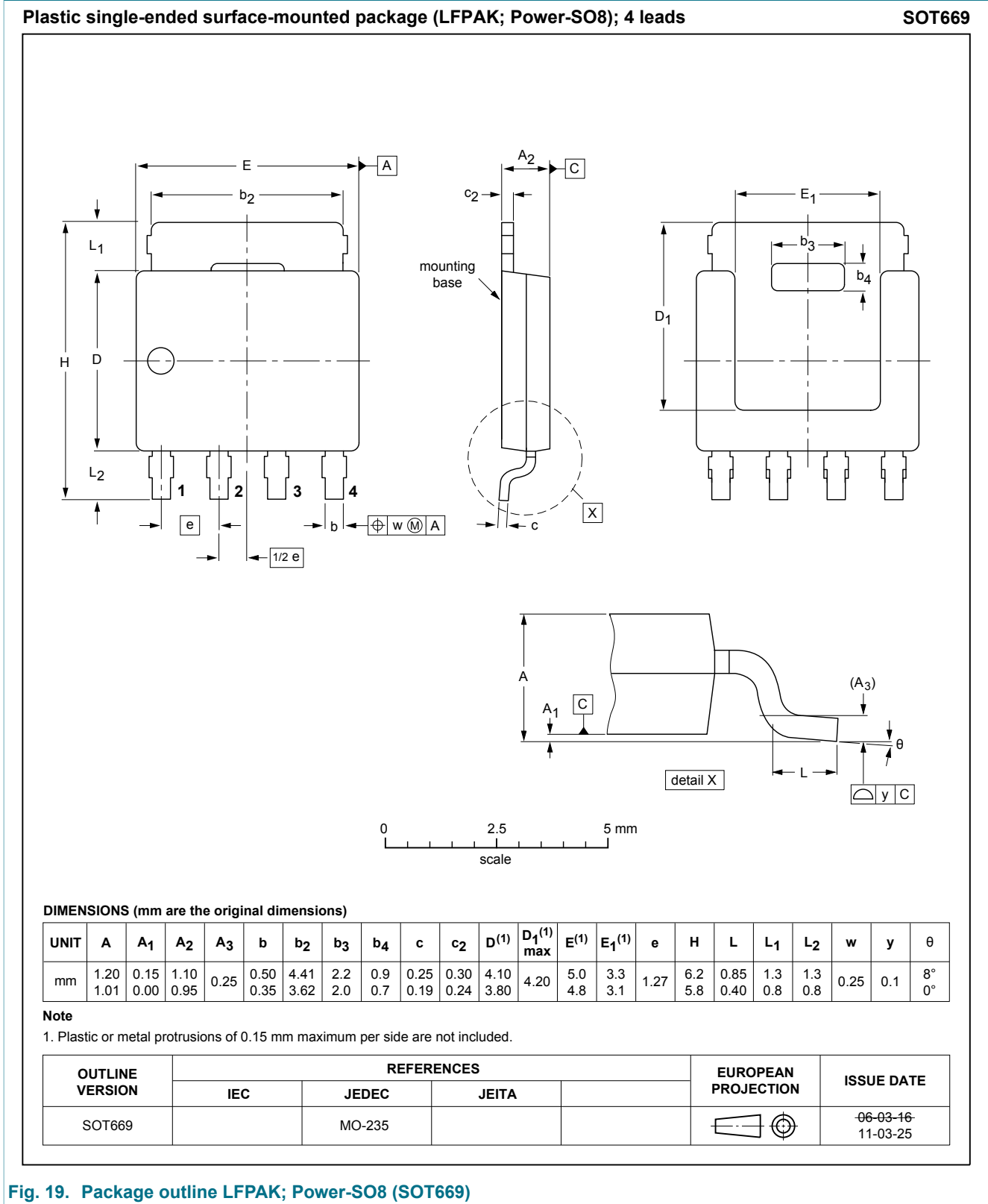


Fig. 19. Package outline LPAK; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## 13. Contents

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